

***Low-Voltage Logic
LVT, LVC, ALVC and LV Families***

Data Book

IMPORTANT NOTICE

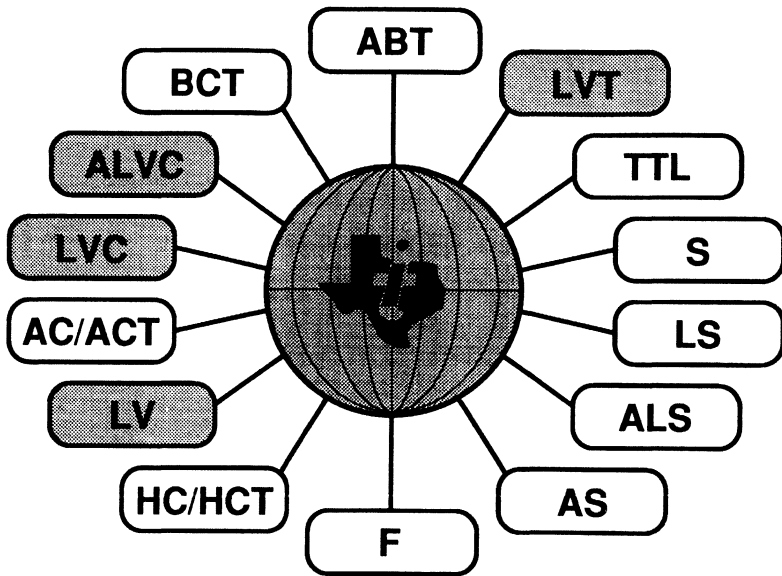
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Digital Logic Spectrum



**GTL (LVT1661x and GTL16821)
device nomenclature change**

Old Part Number	New Part Number
SN74LVT16611	SN74GTL16611
SN74LVT16615	SN74GTL16615
SN74GTL16821	SN74GTL16921



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INTRODUCTION

The 3.3-V era has arrived! The combination of continuous advancement in semiconductor wafer fabrication technologies and the proliferation of battery-powered computing devices has changed the system design methodologies of the past, and indeed our entire industry. This new era will bring an entirely new set of possibilities for computing, hand-held instruments and telecom equipments. Products that will run faster, consume less power, and use fewer total system components than ever before. Products that will be smaller and lighter, yet maintain interface compatibility with existing industry standard bus architectures. Products that will in turn bring on the next era in the computer industry.

Welcome to the 1993 Texas Instruments Low-Voltage Logic Data Book. A single family of 3.3-V logic products could not possibly cover the diverse needs of all of the end equipment segments. Products ranging from hand-held point-of-sale terminals, notebook and laptop personal computers, low-power environmentally conscious desktop computers and peripherals, and high-performance RISC and CISC workstation platforms as well as telecom central and end equipment will all share the need for low-voltage technology, but will each have radically different price, performance, and feature requirements for the logic they will employ. As a response to these diverse needs, Texas Instruments has developed four independent logic families:

- Low-Voltage HCMOS (LV)
- Low-Voltage CMOS (LVC)
- Low-Voltage Technology (LVT)
- Advanced Low-Voltage CMOS (ALVC)

These products span four generations of CMOS and BiCMOS process technologies and years of fine-pitch packaging and innovative circuit developments to deliver a set of products for each of these end-equipment segments. In addition to popular octal and Widebus™ bus-interface circuits, two of the families also include SSI and MSI logic functions to help streamline design and facilitate time to market. Finally, voltage translators are also provided to bridge the gap between the 5-V and 3.3-V worlds.

Some of the information in this data book is in product preview form. For more information on these products including availability dates, pricing, and final timing specifications, please contact your local Texas Instruments field sales representative, authorized distributor, or write directly to

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INTRODUCTION

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

OPERATING CONDITIONS AND CHARACTERISTICS (IN SEQUENCE BY LETTER SYMBOLS)

- C_i** **Input capacitance**
The internal capacitance at an input of the device.
- C_o** **Output capacitance**
The internal capacitance at an output of the device.
- C_{pd}** **Power dissipation capacitance**
Used to determine the no-load dynamic power dissipation per logic function (see individual circuit pages):
 $P_D = C_{pd} V_{CC}^2 f + I_{CC} V_{CC}$.
- f_{max}** **Maximum clock frequency**
The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.
- I_{CC}** **Supply current**
The current into* the V_{CC} supply terminal of an integrated circuit.
- ΔI_{CC}** **Supply current change**
The increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.
- I_{CEX}** **Output high leakage current**
The maximum leakage current into the collector of the pulldown output transistor when the output is high and the output forcing condition V_O = 5.5 V.
- I_{I(hold)}** **Input hold current**
Input current that holds the input at the previous state when the driving device goes to a high-impedance state.
- I_{IH}** **High-level input current**
The current into* an input when a high-level voltage is applied to that input.
- I_{IL}** **Low-level input current**
The current into* an input when a low-level voltage is applied to that input.
- I_{OFF}** **Input/output power-off leakage current**
The maximum leakage current into/out of the input/output transistors when forcing the input/output to 4.5 V and V_{CC} = 0 V.
- I_{OH}** **High-level output current**
The current into* an output with input conditions applied that, according to the product specification, will establish a high level at the output.
- I_{OL}** **Low-level output current**
The current into* an output with input conditions applied that, according to the product specification, will establish a low level at the output.

*Current out of a terminal is given as a negative value.

GLOSSARY SYMBOLS, TERMS, AND DEFINITIONS

I_{OZ}	Off-state (high-impedance-state) output current (of a 3-state output) The current flowing into* an output having 3-state capability with input conditions established that, according to the product specification, will establish the high-impedance state at the output.
t_a	Access time The time interval between the application of a specified input pulse and the availability of valid signals at an output.
t_{dis}	Disable time (of a 3-state or open-collector output) The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from either of the defined active levels (high or low) to a high-impedance (off) state. NOTE: For 3-state outputs, $t_{dis} = t_{PHZ}$ or t_{PLZ} . Open-collector outputs will change only if they are low at the time of disabling so $t_{dis} = t_{PLH}$.
t_{en}	Enable time (of a 3-state or open-collector output) The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from a high-impedance (off) state to either of the defined active levels (high or low). NOTE: In the case of memories, this is the access time from an enable input (e.g., \overline{OE}). For 3-state outputs, $t_{en} = t_{PZH}$ or t_{PZL} . Open-collector outputs will change only if they are responding to data that would cause the output to go low so, for them $t_{en} = t_{PHL}$.
t_h	Hold time The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal. NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed. 2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is guaranteed.
t_{pd}	Propagation delay time The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level. ($t_{pd} = t_{PHL}$ or t_{PLH}).
t_{PHL}	Propagation delay time, high-to-low level output The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.
t_{PHZ}	Disable time (of a 3-state output) from high level The time interval between the specified reference points on the input and the output voltage waveforms with the 3-state output changing from the defined high level to a high-impedance (off) state.
t_{PLH}	Propagation delay time, low-to-high level output The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.
t_{PLZ}	Disable time (of a 3-state output) from low level The time interval between the specified reference points on the input and the output voltage waveforms with the 3-state output changing from the defined low level to a high-impedance (off) state.

t_{PZH}	Enable time (of a 3-state output) to high level The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from a high-impedance (off) state to the defined high level.
t_{PZL}	Enable time (of a 3-state output) to low level The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from a high-impedance (off) state to the defined low level.
t_{su}	Setup time The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal. NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed. 2. The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.
t_w	Pulse duration (width) The time interval between specified reference points on the leading and trailing edges of the pulse waveform.
V_{IH}	High-level input voltage An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables. NOTE: A minimum is specified that is the least-positive value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.
V_{IL}	Low-level input voltage An input voltage within the less positive (more negative) of the two ranges of values used to represent the binary variables. NOTE: A maximum is specified that is the most-positive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.
V_{OH}	High-level output voltage The voltage at an output terminal with input conditions applied that, according to product specification, will establish a high level at the output.
V_{OL}	Low-level output voltage The voltage at an output terminal with input conditions applied that, according to product specification, will establish a low level at the output.
V_{T+}	Positive-going threshold level The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, V _{T-} .
V_{T-}	Negative-going threshold level The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V _{T+} .

EXPLANATION OF FUNCTION TABLES

Among the most complex function tables are those of the shift registers. These embody most of the symbols used in any of the function tables, plus more. Below is the function table of a 4-bit bidirectional universal shift register, e.g., type SN74194.

CLEAR	MODE		CLOCK	INPUTS				OUTPUTS						
	S1	S0		SERIAL		PARALLEL				Q _A	Q _B	Q _C	Q _D	
				LEFT	RIGHT	A	B	C	D					
L	X	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}
H	H	H	↑	X	X	a	b	c	d		a	b	c	d
H	L	H	↑	X	H	H	H	H	H	H	H	Q _{An}	Q _{Bn}	Q _{Cn}
H	L	H	↑	X	L	L	L	L	L	L	L	Q _{An}	Q _{Bn}	Q _{Cn}
H	H	L	↑	H	X	X	X	X	X	X	Q _{Bn}	Q _{Cn}	Q _{Dn}	H
H	H	L	↑	L	X	X	X	X	X	X	Q _{Bn}	Q _{Cn}	Q _{Dn}	L
H	L	L	X	X	X	X	X	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}

The first line of the table represents a synchronous clearing of the register and says that if clear is low, all four outputs will be reset low regardless of the other inputs. In the following lines, clear is inactive (high) and so has no effect.

The second line shows that so long as the clock input remains low (while clear is high), no other input has any effect and the outputs maintain the levels they assumed before the steady-state combination of clear high and clock low was established. Since on other lines of the table only the rising transition of the clock is shown to be active, the second line implicitly shows that no further change in the outputs will occur while the clock remains high or on the high-to-low transition of the clock.

The third line of the table represents synchronous parallel loading of the register and says that if S1 and S0 are both high then, without regard to the serial input, the data entered at A will be at output Q_A, data entered at B will be at Q_B, and so forth, following a low-to-high clock transition.

The fourth and fifth lines represent the loading of high- and low-level data, respectively, from the shift-right serial input and the shifting of previously entered data one bit; data previously at Q_A is now at Q_B, the previous levels of Q_B and Q_C are now at Q_C and Q_D, respectively, and the data previously at Q_D is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is low and S0 is high and the levels at inputs A through D have no effect.



The sixth and seventh lines represent the loading of high- and low-level data, respectively, from the shift-left serial input and the shifting of previously entered data one bit; data previously at Q_B is now at Q_A, the previous levels of Q_C and Q_D are now at Q_B and Q_C, respectively, and the data previously at Q_A is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is high and S0 is low and the levels at inputs A through D have no effect.

The last line shows that as long as both inputs are low, no other input has any effect and, as in the second line, the outputs maintain the levels they assumed before the steady-state combination of clear high and both mode inputs low was established.



The function table functional tests do not reflect all possible combinations or sequential modes.

EXPLANATION OF FUNCTION TABLES

The following symbols are used in function tables on TI data sheets:

H	=	high level (steady state)
L	=	low level (steady state)
↑	=	transition from low to high level
↓	=	transition from high to low level
→	=	value/level or resulting value/level is routed to indicated destination
↶	=	value/level is re-entered
X	=	irrelevant (any input, including transitions)
Z	=	off (high-impedance) state of a 3-state output
a . . . h	=	the level of steady-state inputs A through H respectively
Q_0	=	level of Q before the indicated steady-state input conditions were established
\bar{Q}_0	=	complement of Q_0 or level of \bar{Q} before the indicated steady-state input conditions were established
Q_n	=	level of Q before the most recent active transition indicated by ↓ or ↑
	=	one high-level pulse
	=	one low-level pulse
Toggle	=	each output changes to the complement of its previous level on each active transition indicated by ↓ or ↑

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

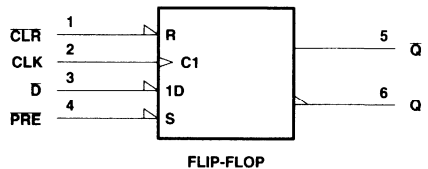
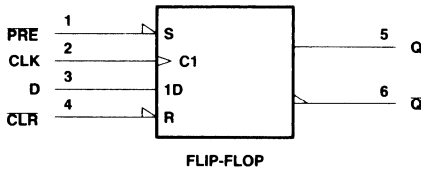
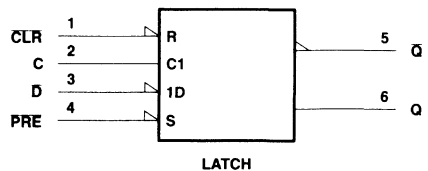
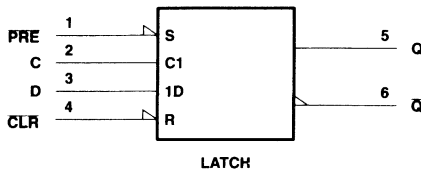
If, in the input columns, a row contains H, L, and/or X together with ↑ and/or ↓, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q_0 , or \bar{Q}_0), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as a pulse,  or , the pulse follows the indicated input transition and persists for an interval dependent on the circuit.)

D FLIP-FLOP AND LATCH SIGNAL CONVENTIONS

It is normal TI practice to name the outputs and other inputs of a D-type flip-flop or latch and to draw its logic symbol based on the assumption of true data (D) inputs. Outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called \bar{Q} . An input that causes a Q output to go high or a \bar{Q} output to go low is called preset (PRE). An input that causes a \bar{Q} output to go high or a Q output to go low is called clear (CLR). Bars are used over these pin names (PRE and CLR) if they are active low.

The devices on several data sheets are second-source designs, and the pin name conventions used by the original manufacturers have been retained. That makes it necessary to designate the inputs and outputs of the inverting circuits \bar{D} and \bar{Q} .

In some applications, it may be advantageous to redesignate the data input from D to \bar{D} or vice versa. In that case, all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbols. Arbitrary pin numbers are shown.



The figures show that when Q and \bar{Q} exchange names, the preset and clear pins also exchange names. The polarity indicators (\triangle) on PRE and CLR remain, as these inputs are still active-low, but the presence or absence of the polarity indicator changes at D (or \bar{D}), Q, and \bar{Q} . Pin 5 (Q or \bar{Q}) is still in phase with the data input (D or \bar{D}); their active levels change together.

In digital system design, consideration must be given to thermal management of components. The small size of the small-outline package makes this even more critical. Figure 1 shows the thermal resistance of these packages for various rates of air flow.

The thermal resistances in Figure 1 can be used to approximate typical and maximum virtual junction temperatures for the EPIC™ ACL family. In general, the junction temperature for any device can be calculated using Equation 1.

$$T_J = R_{\theta JA} \times P_T + T_A \tag{1}$$

where:

- T_J = virtual junction temperature
- R_{θJA} = thermal resistance, junction to free air
- P_T = total power dissipation of the device
- T_A = free-air temperature

The total power consumption can be determined from Equation 2 for an AC device and Equation 3 for an ACT device.

$$P_T = V_{CC} \times I_{CC} + (C_{pd} \times V_{CC}^2 \times f_i) + \Sigma(C_L \times V_{CC}^2 \times f_o) \tag{2}$$

$$P_T = V_{CC} \times [I_{CC} + (N \times \Delta I_{CC} \times DC)] + (C_{pd} \times V_{CC}^2 \times f_i) + \Sigma(C_L \times V_{CC}^2 \times f_o) \tag{3}$$

where:

- V_{CC} = supply voltage (5 V for typical, 5.5 V for maximum) (see Note 1)
- I_{CC} = quiescent supply current (specified on device data sheet)
- C_{pd} = power dissipation capacitance (from the device data sheet)
- f_i = input frequency
- C_L = output load capacitance
- f_o = output frequency
- N = number of inputs driven by a TTL device
- DC = duty cycle
- ΔI_{CC} = increase in supply current (specified on device data sheet)

NOTE 1: In system applications, I_{CC} can be minimized by keeping input voltage levels less than 1 V for V_{IL} and greater than V_{CC} - 1 V for V_{IH} and input rise and fall times less than 15 ns.

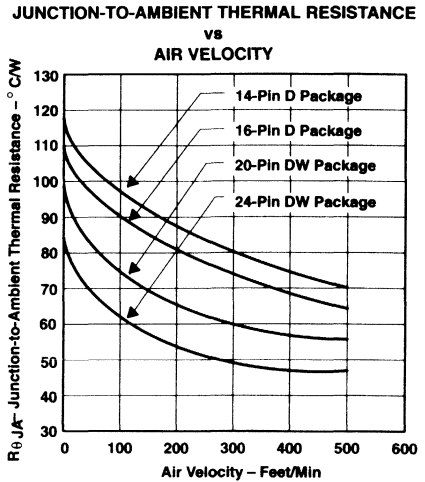


Figure 1

THERMAL INFORMATION

DERATING CURVES FOR 210-MIL SHRINK SMALL-OUTLINE PACKAGE (DB)

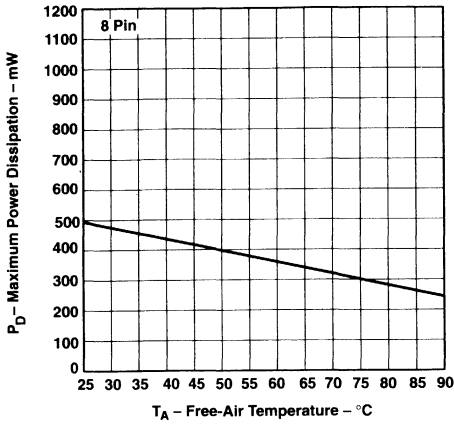


Figure 2

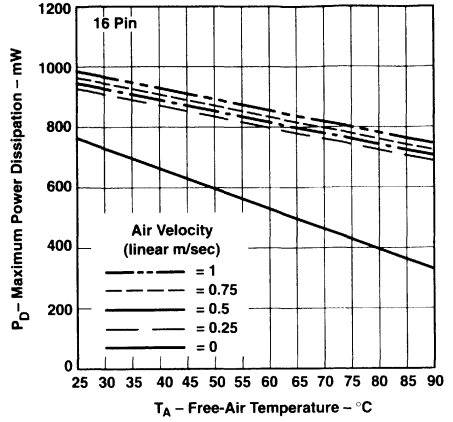


Figure 3

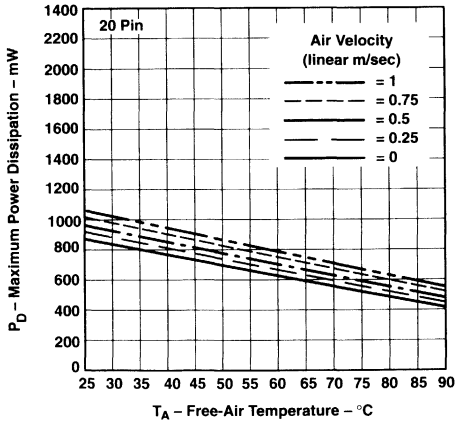


Figure 4

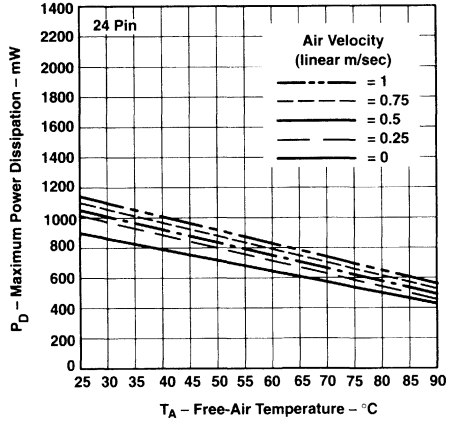


Figure 5

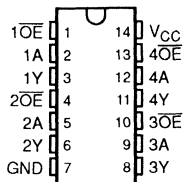
General Information	1
LVT Octals and Widebus™	2
LVC MSI, Octals and Widebus™	3
ALVC Widebus™	4
LV MSI and Octals	5
GTL Widebus™	6
CBT Bus Switches and 5-V/3-V Volt. Translators	7
Application Notes	8
LVT Characterization Information	9
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SN54LVT125, SN74LVT125 3.3-V ABT QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS

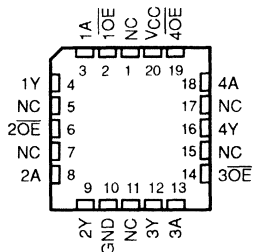
SCBS133A – MAY 1992 – REVISED MARCH 1993

- State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Package Options Include Plastic Small-Outline (SOIC), Shrink Small-Outline (SSOP), and Thin Shrink Small-Outline (TSSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs

SN54LVT125 ... J PACKAGE
SN74LVT125 ... DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVT125 ... FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These bus buffers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The LVT125 features independent line drivers with 3-state outputs. Each output is in the high-impedance state when the associated output-enable (\overline{OE}) input is high.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVT125 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT125 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVT125 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
\overline{OE}	A	Y
L	H	H
L	L	L
H	X	Z

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

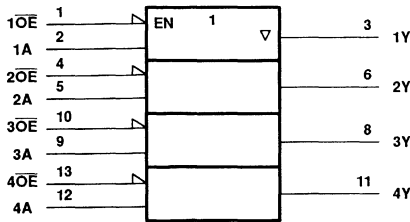


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SN54LVT125, SN74LVT125
3.3-V ABT QUADRUPLE BUS BUFFERS
WITH 3-STATE OUTPUTS

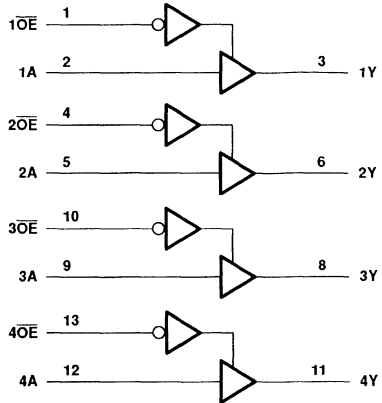
SCBS133A – MAY 1992 – REVISED MARCH 1993

logic symbol



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for the DB, DW, J, and PW packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1)	-0.5 V to 7 V
Current into any output in the low state, I_{OL} : SN54LVT125	96 mA
SN74LVT125	128 mA
Current into any output in the high state, I_{OH} (see Note 2): SN54LVT125	48 mA
SN74LVT125	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DB package	0.6 W
DW package	0.85 W
PW package	0.5 W
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp current ratings are observed.
 2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

SN54LVT125, SN74LVT125 3.3-V ABT QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS

SCBS133A – MAY 1992 – REVISED MARCH 1993

recommended operating conditions

		SN54LVT125		SN74LVT125		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage		5.5		5.5	V
I _{OH}	High-level output current		-24		-32	mA
I _{OL}	Low-level output current		24		32	mA
I _{OL} †	Low-level output current		48		64	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
T _A	Operating free-air temperature	-55	125	-40	85	°C

† Current duty cycle ≤ 50%, f ≥ 1 kHz

SN54LVT125, SN74LVT125

3.3-V ABT QUADRUPLE BUS BUFFERS

WITH 3-STATE OUTPUTS

SCBS133A – MAY 1992 – REVISED MARCH 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54LVT125		SN74LVT125		UNIT		
			MIN	TYP†	MAX	MIN		TYP†	MAX
V_{IK}	$V_{CC} = 2.7 \text{ V}$,	$I_I = -18 \text{ mA}$			-1.2		-1.2	V	
V_{OH}	$V_{CC} = \text{MIN to MAX}^\ddagger$,	$I_{OH} = -100 \mu\text{A}$	$V_{CC} - 0.2$		$V_{CC} - 0.2$			V	
	$V_{CC} = 2.7 \text{ V}$,	$I_{OH} = -8 \text{ mA}$	2.4		2.4				
	$V_{CC} = 3 \text{ V}$,	$I_{OH} = -24 \text{ mA}$	2						
	$V_{CC} = 3 \text{ V}$,	$I_{OH} = -32 \text{ mA}$			2				
V_{OL}	$V_{CC} = 2.7 \text{ V}$,	$I_{OL} = 100 \mu\text{A}$			0.2		0.2	V	
	$V_{CC} = 2.7 \text{ V}$,	$I_{OL} = 24 \text{ mA}$			0.5		0.5		
	$V_{CC} = 3 \text{ V}$,	$I_{OL} = 16 \text{ mA}$			0.4		0.4		
	$V_{CC} = 3 \text{ V}$,	$I_{OL} = 32 \text{ mA}$			0.5		0.5		
	$V_{CC} = 3 \text{ V}$,	$I_{OL} = 48 \text{ mA}$			0.55				
	$V_{CC} = 3 \text{ V}$,	$I_{OL} = 64 \text{ mA}$					0.55		
I_I	$V_{CC} = 0 \text{ or MAX}^\ddagger$,	$V_I = 5.5 \text{ V}$			10		10	μA	
	$V_{CC} = 3.6 \text{ V}$,	$V_I = V_{CC} \text{ or GND}$	Control pins		± 1		± 1		
	$V_{CC} = 3.6 \text{ V}$,	$V_I = V_{CC}$	Data pins		1		1		
	$V_{CC} = 3.6 \text{ V}$,	$V_I = 0$			-5		-5		
I_{off}	$V_{CC} = 0$,	$V_I \text{ or } V_O = 0 \text{ to } 4.5 \text{ V}$					± 100	μA	
$I_I(\text{hold})$	$V_{CC} = 3 \text{ V}$	$V_I = 0.8 \text{ V}$	Data inputs		75		75	μA	
		$V_I = 2 \text{ V}$			-75		-75		
I_{OZH}	$V_{CC} = 3.6 \text{ V}$,	$V_O = 3 \text{ V}$			5		5	μA	
I_{OZL}	$V_{CC} = 3.6 \text{ V}$,	$V_O = 0.5 \text{ V}$			-5		-5	μA	
I_{CC}	$V_{CC} = 3.6 \text{ V}$,	$V_I = V_{CC} \text{ or GND}$	$I_O = 0$	Outputs high	0.12	0.19	0.12	0.19	mA
				Outputs low	4.5	7	4.5	7	
				Outputs disabled	0.12	0.19	0.12	0.19	
ΔI_{CC}^\S	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$, One input at $V_{CC} - 0.6 \text{ V}$, Other inputs at $V_{CC} \text{ or GND}$				0.3		0.2	mA	
C_i	$V_I = 3 \text{ V or } 0$				4		4	pF	
C_o	$V_O = 3 \text{ V or } 0$				8		8	pF	

† All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT125			SN74LVT125			UNIT	
			$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CC} = 2.7 \text{ V}$	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CC} = 2.7 \text{ V}$		
			MIN	MAX	MAX	MIN	TYP†	MAX		
t_{PLH}	A	Y	1	4.2	4.7	1	2.7	4	4.5	ns
t_{PHL}			1	4.1	5.1	1	2.9	3.9	4.9	
t_{PZH}	\overline{OE}	Y	1	4.9	6.2	1	3.4	4.7	6	ns
t_{PZL}			1.1	4.9	6.7	1.1	3.4	4.7	6.5	
t_{PHZ}	\overline{OE}	Y	1.8	5.3	5.9	1.8	3.7	5.1	5.7	ns
t_{PLZ}			1.3	4.7	4.2	1.3	2.6	4.5	4	

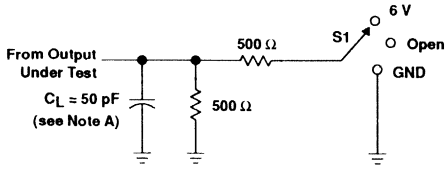
PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



SN54LVT125, SN74LVT125 3.3-V ABT QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS

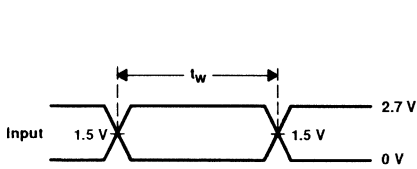
SCBS133A – MAY 1992 – REVISED MARCH 1993

PARAMETER MEASUREMENT INFORMATION

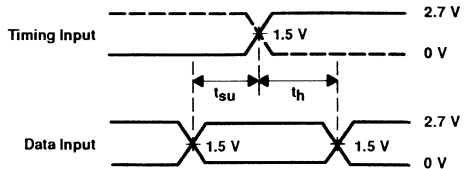


LOAD CIRCUIT FOR OUTPUTS

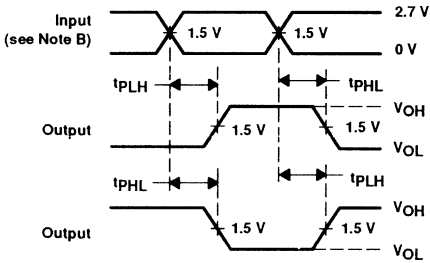
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



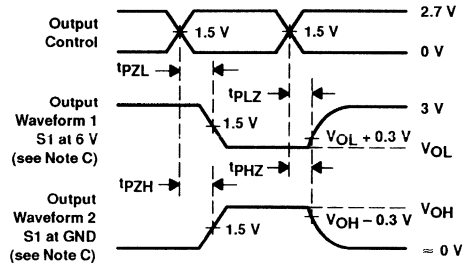
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SN54LVT240, SN74LVT240 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS143B – SEPTEMBER 1992 – REVISED JUNE 1993

- State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Package Options Include Plastic Small-Outline (SOIC), Shrink Small-Outline (SSOP), and Thin Shrink Small-Outline (TSSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs

description

These octal buffers and line drivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

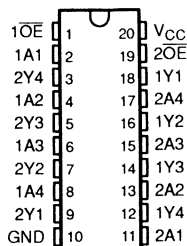
The LVT240 is organized as two 4-bit buffer/line drivers with separate output-enable ($\overline{\text{OE}}$) inputs. When $\overline{\text{OE}}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{\text{OE}}$ is high, the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

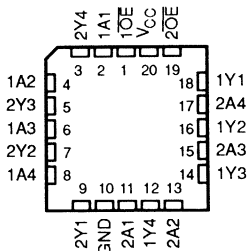
The SN74LVT240 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT240 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVT240 is characterized for operation from -40°C to 85°C .

SN54LVT240 ... J PACKAGE
SN74LVT240 ... DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVT240 ... FK PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{\text{OE}}$	A	Y
L	H	L
L	L	H
H	X	Z

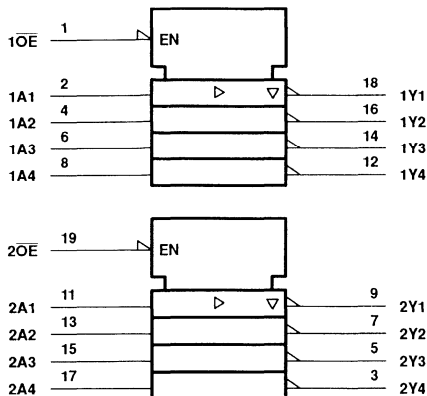
SN54LVT240, SN74LVT240

3.3-V ABT OCTAL BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

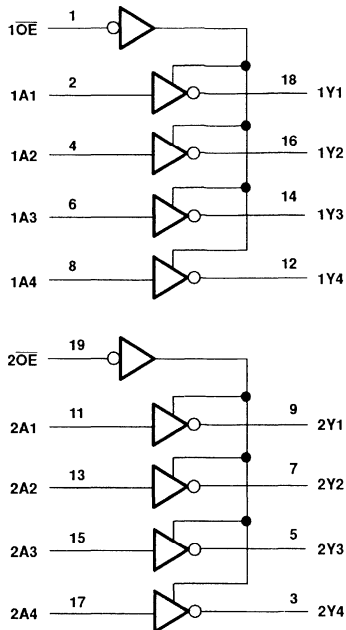
SCBS143B – SEPTEMBER 1992 – REVISED JUNE 1993

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1)	-0.5 V to 7 V
Current into any output in the low state, I_O : SN54LVT240	96 mA
SN74LVT240	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT240	48 mA
SN74LVT240	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DB package	0.65 W
DW package	0.85 W
PW package	0.6 W
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

SN54LVT240, SN74LVT240
3.3-V ABT OCTAL BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

SCBS143B - SEPTEMBER 1992 - REVISED JUNE 1993

recommended operating conditions

		SN54LVT240		SN74LVT240		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage		5.5		5.5	V
I _{OH}	High-level output current		-24		-32	mA
I _{OL}	Low-level output current		24		32	mA
I _{OL} †	Low-level output current		48		64	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
T _A	Operating free-air temperature	-55	125	-40	85	°C

† Current duty cycle ≤ 50%, f ≥ 1 kHz

SN54LVT240, SN74LVT240

3.3-V ABT OCTAL BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

SCBS143B - SEPTEMBER 1992 - REVISED JUNE 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54LVT240		SN74LVT240		UNIT
			MIN	TYP†	MAX	MIN	
V_{IK}	$V_{CC} = 2.7\text{ V}$, $I_I = -18\text{ mA}$		-1.2		-1.2		V
V_{OH}	$V_{CC} = \text{MIN to MAX}^\ddagger$, $I_{OH} = -100\ \mu\text{A}$		$V_{CC} - 0.2$		$V_{CC} - 0.2$		V
	$V_{CC} = 2.7\text{ V}$, $I_{OH} = -8\text{ mA}$		2.4		2.4		
	$V_{CC} = 3\text{ V}$, $I_{OH} = -24\text{ mA}$		2				
	$V_{CC} = 3\text{ V}$, $I_{OH} = -32\text{ mA}$				2		
V_{OL}	$V_{CC} = 2.7\text{ V}$, $I_{OL} = 100\ \mu\text{A}$		0.2		0.2		V
	$V_{CC} = 2.7\text{ V}$, $I_{OL} = 24\text{ mA}$		0.5		0.5		
	$V_{CC} = 3\text{ V}$, $I_{OL} = 16\text{ mA}$		0.4		0.4		
	$V_{CC} = 3\text{ V}$, $I_{OL} = 32\text{ mA}$		0.5		0.5		
	$V_{CC} = 3\text{ V}$, $I_{OL} = 48\text{ mA}$		0.55				
	$V_{CC} = 3\text{ V}$, $I_{OL} = 64\text{ mA}$				0.55		
I_I	$V_{CC} = 0\text{ or MAX}^\ddagger$, $V_I = 5.5\text{ V}$		10		10		μA
	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}\text{ or GND}$		Control pins		± 1		
	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}$		Data pins		1		
	$V_{CC} = 3.6\text{ V}$, $V_I = 0$				-5		
I_{off}	$V_{CC} = 0$, $V_I\text{ or }V_O = 0\text{ to }4.5\text{ V}$				± 100		μA
$I_I(\text{hold})$	$V_{CC} = 3\text{ V}$		75		75		μA
	$V_I = 0.8\text{ V}$		-75		-75		
	$V_I = 2\text{ V}$		A inputs				
I_{OZH}	$V_{CC} = 3.6\text{ V}$, $V_O = 3\text{ V}$		5		5		μA
I_{OZL}	$V_{CC} = 3.6\text{ V}$, $V_O = 0.5\text{ V}$		-5		-5		μA
I_{CC}	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}\text{ or GND}$, $I_O = 0$		Outputs high		0.12 0.19		mA
			Outputs low		8.6 12		
			Outputs disabled		0.12 0.19		
ΔI_{CC}^\S	$V_{CC} = 3\text{ V to }3.6\text{ V}$, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at $V_{CC}\text{ or GND}$		0.2		0.2		mA
C_i	$V_I = 3\text{ V or }0$		4		4		pF
C_o	$V_O = 3\text{ V or }0$		8		8		pF

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT240			SN74LVT240			UNIT	
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		
			MIN	MAX	MAX	MIN	TYP†	MAX		
t_{PLH}	A	Y	1	4.5	5.4	1	2.5	4.3	5.2	ns
t_{PHL}			1	4.5	5.2	1	2.5	4.3	5	
t_{PZH}	$\overline{\text{OE}}$	Y	1	5.4	6.5	1	2.7	5.2	6.3	ns
t_{PZL}			1	5.4	7.4	1	3.1	5.2	6.7	
t_{PHZ}	$\overline{\text{OE}}$	Y	2	5.8	6.5	2	3.9	5.6	6.3	ns
t_{PLZ}			1.6	5.3	5.8	1.6	3.2	5.1	5.6	

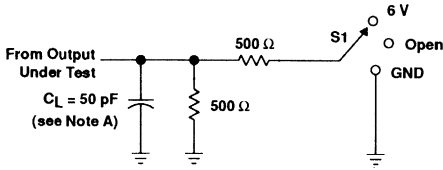
PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



SN54LVT240, SN74LVT240
3.3-V ABT OCTAL BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

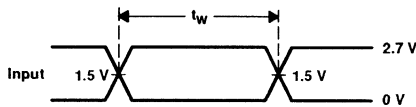
SCBS143B - SEPTEMBER 1992 - REVISED JUNE 1993

PARAMETER MEASUREMENT INFORMATION

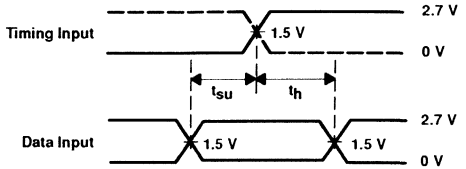


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

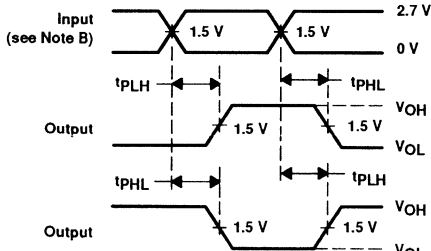
LOAD CIRCUIT FOR OUTPUTS



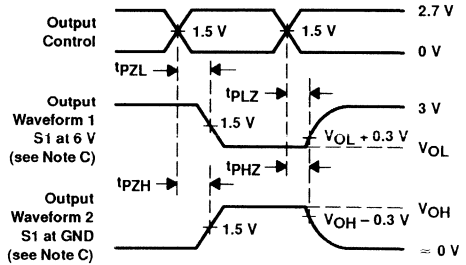
**VOLTAGE WAVEFORMS
PULSE DURATION**



**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

- NOTES:
- C_L includes probe and jig capacitance.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SN54LVTZ240, SN74LVTZ240 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SEPTEMBER 1993 – REVISED OCTOBER 1993

- State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- High-Impedance State During Power Up and Power Down
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Package Options Include Plastic Small-Outline (SOIC), Shrink Small-Outline (SSOP), and Thin Shrink Small-Outline (TSSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs

description

These octal buffers and line drivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

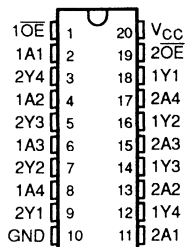
The LVTZ240 is organized as two 4-bit line drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

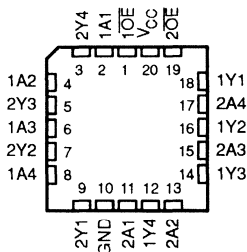
The SN74LVTZ240 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVTZ240 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVTZ240 is characterized for operation from -40°C to 85°C .

SN54LVTZ240 ... J PACKAGE
SN74LVTZ240 ... DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVTZ240 ... FK PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
\overline{OE}	A	Y
L	H	L
L	L	H
H	X	Z

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



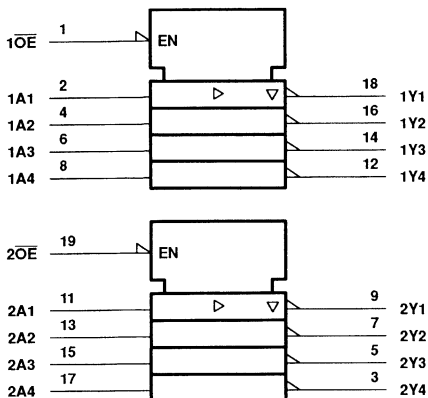
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SN54LVTZ240, SN74LVTZ240

3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

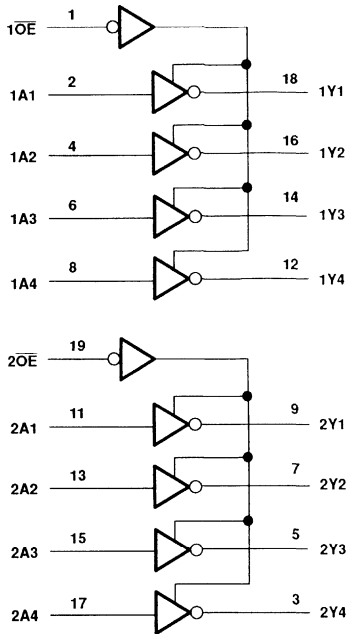
SEPTEMBER 1993 – REVISED OCTOBER 1993

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	−0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	−0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1)	−0.5 V to 7 V
Current into any output in the low state, I_{OL} : SN54LVTZ240	96 mA
SN74LVTZ240	128 mA
Current into any output in the high state, I_{OH} (see Note 2): SN54LVTZ240	48 mA
SN74LVTZ240	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	−50 mA
Output clamp current, I_{OK} ($V_O < 0$)	−50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DB package	0.5 W
DW package	0.85 W
PW package	0.5 W
Storage temperature range	−65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

SN54LVTZ240, SN74LVTZ240
3.3-V ABT OCTAL BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

SEPTEMBER 1993 – REVISED OCTOBER 1993

recommended operating conditions

		SN54LVTZ240		SN74LVTZ240		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8	0.8		V
V _I	Input voltage		5.5	5.5		V
I _{OH}	High-level output current		-24	-32		mA
I _{OL}	Low-level output current		24	32		mA
I _{OL} †	Low-level output current		48	64		mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
Δt/ΔV _{CC}	Power-up ramp rate	200		200		μs/V
T _A	Operating free-air temperature	-55	125	-40	85	°C

† Current duty cycle ≤ 50%, f ≥ 1 kHz

SN54LVTZ240, SN74LVTZ240
3.3-V ABT OCTAL BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

SEPTEMBER 1993 – REVISED OCTOBER 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54LVTZ240		SN74LVTZ240		UNIT	
			MIN	TYP†	MAX	MIN		TYP†
V_{IK}	$V_{CC} = 2.7\text{ V}$, $I_I = -18\text{ mA}$				-1.2		V	
V_{OH}	$V_{CC} = \text{MIN to MAX}^\ddagger$, $I_{OH} = -100\ \mu\text{A}$		$V_{CC} - 0.2$		$V_{CC} - 0.2$		V	
	$V_{CC} = 2.7\text{ V}$, $I_{OH} = -8\text{ mA}$		2.4		2.4			
	$V_{CC} = 3\text{ V}$, $I_{OH} = -24\text{ mA}$		2					
	$V_{CC} = 3\text{ V}$, $I_{OH} = -32\text{ mA}$				2			
V_{OL}	$V_{CC} = 2.7\text{ V}$, $I_{OL} = 100\ \mu\text{A}$				0.2		V	
	$V_{CC} = 2.7\text{ V}$, $I_{OL} = 24\text{ mA}$				0.5			
	$V_{CC} = 3\text{ V}$, $I_{OL} = 16\text{ mA}$				0.4			
	$V_{CC} = 3\text{ V}$, $I_{OL} = 32\text{ mA}$				0.5			
	$V_{CC} = 3\text{ V}$, $I_{OL} = 48\text{ mA}$				0.55			
	$V_{CC} = 3\text{ V}$, $I_{OL} = 64\text{ mA}$				0.55			
I_I	$V_{CC} = 0\text{ or MAX}^\ddagger$, $V_I = 5.5\text{ V}$				10		μA	
	$V_{CC} = 0\text{ to }3.6\text{ V}$, $V_I = V_{CC}\text{ or GND}$		Control pins		± 1			
	$V_{CC} = 0\text{ to }3.6\text{ V}$, $V_I = V_{CC}$		Data pins		1			
	$V_{CC} = 0\text{ to }3.6\text{ V}$, $V_I = 0$				-5			
I_{off}	$V_{CC} = 0\text{ V}$, $V_I\text{ or }V_O = 0\text{ to }4.5\text{ V}$				± 100		μA	
I_{OZPU}^\S	$V_{CC} = 0\text{ V to }1.5$, $V_O = 0.5\text{ to }3\text{ V}$, $\overline{OE} = 0.8\text{ V}$				± 50		μA	
I_{OZPD}^\S	$V_{CC} = 1.5\text{ V to }0$, $V_O = 0.5\text{ to }3\text{ V}$, $\overline{OE} = 0.8\text{ V}$				± 50		μA	
$I_I(\text{hold})$	$V_{CC} = 3\text{ V}$	$V_I = 0.8\text{ V}$	A inputs	75		75		μA
		$V_I = 2\text{ V}$		-75		-75		
I_{OZH}	$V_{CC} = 1.5\text{ V to }3.6\text{ V}$, $V_O = 3\text{ V}$				5		μA	
I_{OZL}	$V_{CC} = 1.5\text{ V to }3.6\text{ V}$, $V_O = 0.5\text{ V}$				-5		μA	
I_{CC}	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}\text{ or GND}$	$I_O = 0$	Outputs high		0.12 0.5		0.12 0.225	
			Outputs low		8.6 14		8.6 12	
			Outputs disabled		0.12 0.5		0.12 0.225	
ΔI_{CC}^\S	$V_{CC} = 3\text{ V to }3.6\text{ V}$, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at $V_{CC}\text{ or GND}$				0.3		0.2	
C_i	$V_I = 3\text{ V or }0$				4		4	
C_o	$V_O = 3\text{ V or }0$				8		8	

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

¶ This parameter is guaranteed by characterization.

SN54LVTZ240, SN74LVTZ240
3.3-V ABT OCTAL BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

SEPTEMBER 1993 – REVISED OCTOBER 1993

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

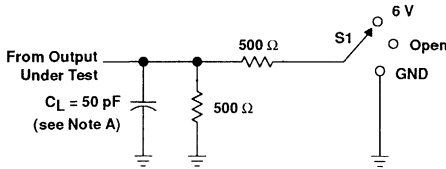
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTZ240			SN74LVTZ240				UNIT
			$V_{CC} = 3.3 V \pm 0.3 V$		$V_{CC} = 2.7 V$	$V_{CC} = 3.3 V \pm 0.3 V$		$V_{CC} = 2.7 V$		
			MIN	MAX	MAX	MIN	TYP†	MAX	MAX	
t_{PLH}	A	Y	1	4.5	5.4	1	2.5	4.3	5.2	ns
t_{PHL}			1	4.5	5.2	1	2.5	4.3	5	
t_{PZH}	\overline{OE}	Y	1	5.4	6.5	1	2.7	5.2	6.3	ns
t_{PZL}			1	5.4	7.4	1	3.1	5.2	6.7	
t_{PHZ}	\overline{OE}	Y	2	5.8	6.5	2	3.9	5.6	6.3	ns
t_{PLZ}			1.6	5.3	5.8	1.6	3.2	5.1	5.6	

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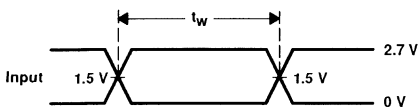
SN54LVT240, SN74LVT240
3.3-V ABT OCTAL BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS
 SEPTEMBER 1993 – REVISED OCTOBER 1993

PARAMETER MEASUREMENT INFORMATION

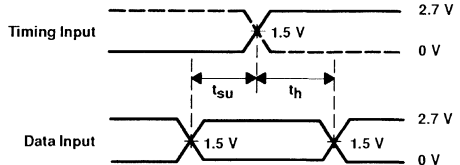


LOAD CIRCUIT FOR OUTPUTS

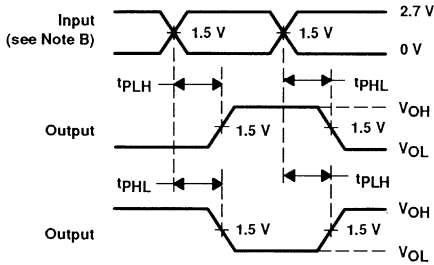
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



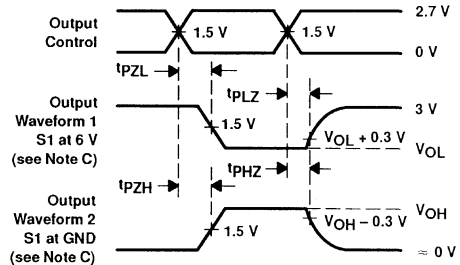
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SN54LVT244A, SN74LVT244A 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS135A - AUGUST 1992 - REVISED SEPTEMBER 1993

- State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Package Options Include Plastic Small-Outline (SOIC), Shrink Small-Outline (SSOP), and Thin Shrink Small-Outline (TSSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs

description

These octal buffers and line drivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

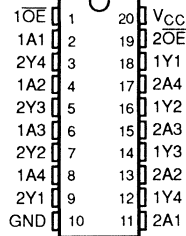
The 'LVT244A is organized as two 4-bit line drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

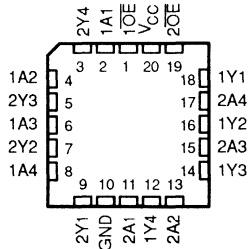
The SN74LVT244A is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT244A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVT244A is characterized for operation from -40°C to 85°C .

SN54LVT244A ... J PACKAGE
SN74LVT244A ... DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVT244A ... FK PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each buffer)

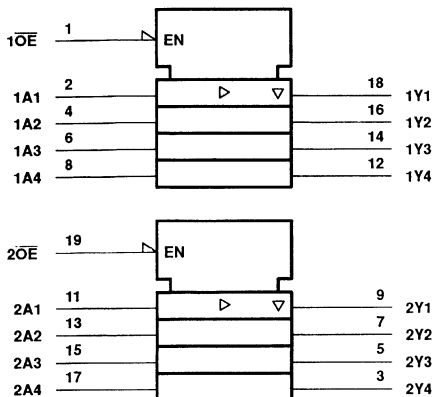
INPUTS		OUTPUT
\overline{OE}	A	Y
L	H	H
L	L	L
H	X	Z

SN54LVT244A, SN74LVT244A

3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

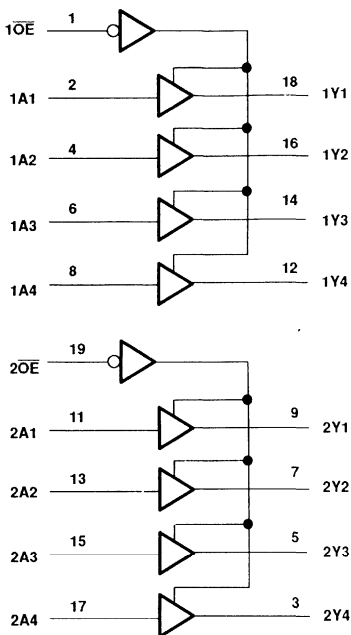
SCBS135A - AUGUST 1992 - REVISED SEPTEMBER 1993

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1)	-0.5 V to 7 V
Current into any output in the low state, I_O : SN54LVT244A	96 mA
SN74LVT244A	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT244A	48 mA
SN74LVT244A	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DB package	0.65 W
DW package	0.85 W
PW package	0.6 W
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp current ratings are observed.
 2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

SN54LVT244A, SN74LVT244A

3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS135A – AUGUST 1992 – REVISED SEPTEMBER 1993

recommended operating conditions

		SN54LVT244A		SN74LVT244A		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage		5.5		5.5	V
I _{OH}	High-level output current		-24		-32	mA
I _{OL}	Low-level output current		24		32	mA
I _{OL} †	Low-level output current		48		64	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled			10	ns/V
T _A	Operating free-air temperature	-55	125	-40	85	°C

† Current duty cycle ≤ 50%, f ≥ 1 kHz

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



SN54LVT244A, SN74LVT244A

3.3-V ABT OCTAL BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

SCBS135A – AUGUST 1992 – REVISED SEPTEMBER 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54LVT244A		SN74LVT244A		UNIT		
			MIN	TYP†	MAX	MIN		TYP†	MAX
V_{IK}	$V_{CC} = 2.7\text{ V}$, $I_I = -18\text{ mA}$		-1.2		-1.2		V		
V_{OH}	$V_{CC} = \text{MIN to MAX}^\ddagger$, $I_{OH} = -100\ \mu\text{A}$		$V_{CC} - 0.2$		$V_{CC} - 0.2$		V		
	$V_{CC} = 2.7\text{ V}$, $I_{OH} = -8\text{ mA}$		2.4		2.4				
	$V_{CC} = 3\text{ V}$, $I_{OH} = -24\text{ mA}$		2						
	$V_{CC} = 3\text{ V}$, $I_{OH} = -32\text{ mA}$				2				
V_{OL}	$V_{CC} = 2.7\text{ V}$, $I_{OL} = 100\ \mu\text{A}$				0.2		V		
	$V_{CC} = 2.7\text{ V}$, $I_{OL} = 24\text{ mA}$				0.5				
	$V_{CC} = 3\text{ V}$, $I_{OL} = 16\text{ mA}$				0.4				
	$V_{CC} = 3\text{ V}$, $I_{OL} = 32\text{ mA}$				0.5				
	$V_{CC} = 3\text{ V}$, $I_{OL} = 48\text{ mA}$				0.55				
	$V_{CC} = 3\text{ V}$, $I_{OL} = 64\text{ mA}$				0.55				
I_I	$V_{CC} = 0\text{ or MAX}^\ddagger$, $V_I = 5.5\text{ V}$				10		μA		
	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}\text{ or GND}$		Control pins		± 1				
	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}$		Data pins		1				
	$V_{CC} = 3.6\text{ V}$, $V_I = 0$				-5				
I_{off}	$V_{CC} = 0$, $V_I\text{ or }V_O = 0\text{ to }4.5\text{ V}$				± 100		μA		
$I_I(\text{hold})$	$V_{CC} = 3\text{ V}$	$V_I = 0.8\text{ V}$	A inputs		75		μA		
		$V_I = 2\text{ V}$			-75				
I_{OZH}	$V_{CC} = 3.6\text{ V}$, $V_O = 3\text{ V}$		5		5		μA		
I_{OZL}	$V_{CC} = 3.6\text{ V}$, $V_O = 0.5\text{ V}$		-5		-5		μA		
I_{CC}	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}\text{ or GND}$		$I_O = 0$, Outputs high		0.12	0.5	0.12	0.19	mA
			Outputs low		8.6	14	8.6	12	
			Outputs disabled		0.12	0.5	0.12	0.19	
ΔI_{CC}^\S	$V_{CC} = 3\text{ V to }3.6\text{ V}$, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at $V_{CC}\text{ or GND}$		0.3		0.2		mA		
C_i	$V_I = 3\text{ V or }0$		4		4		pF		
C_o	$V_O = 3\text{ V or }0$		8		8		pF		

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT244A			SN74LVT244A			UNIT	
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		
			MIN	MAX	MAX	MIN	TYP†	MAX		MAX
t_{PLH}	A	Y	0.5	4.7	5.2	1	2.5	4.1	5	ns
t_{PHL}			0.5	4.4	5.4	1	2.5	4.1	5.2	
t_{PZH}	\overline{OE}	Y	0.8	5.4	6.5	1	2.7	5.2	6.3	ns
t_{PZL}			0.8	5.4	7.6	1.1	3.1	5.2	6.7	
t_{PHZ}	\overline{OE}	Y	1.5	6.2	6.9	1.9	3.9	5.6	6.3	ns
t_{PLZ}			1.2	5.5	6	1.8	3.2	5.1	5.6	

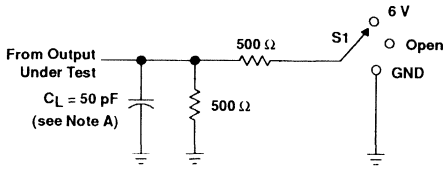
PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



SN54LVT244A, SN74LVT244A
3.3-V ABT OCTAL BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

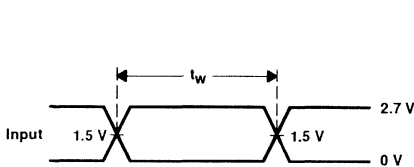
SCBS135A – AUGUST 1992 – REVISED SEPTEMBER 1993

PARAMETER MEASUREMENT INFORMATION

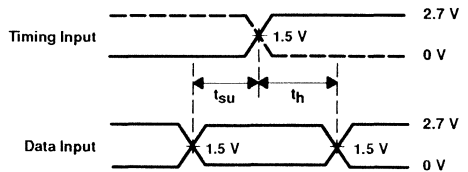


LOAD CIRCUIT FOR OUTPUTS

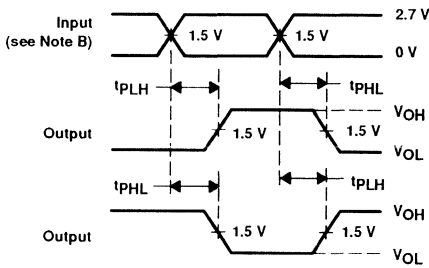
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



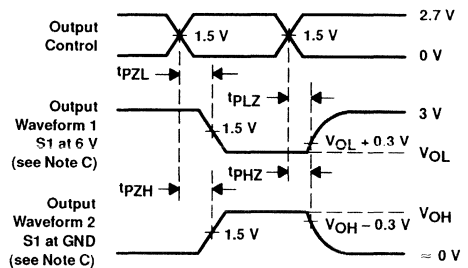
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SN54LVTZ244, SN74LVTZ244 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SEPTEMBER 1993

- State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- High-Impedance State During Power Up and Power Down
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Package Options Include Plastic Small-Outline (SOIC), Shrink Small-Outline (SSOP), and Thin Shrink Small-Outline (TSSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs

description

These octal buffers and line drivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVTZ244 is organized as two 4-bit line drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

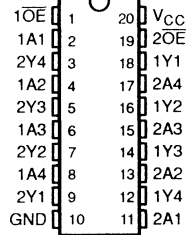
The SN74LVTZ244 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVTZ244 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVTZ244 is characterized for operation from -40°C to 85°C .

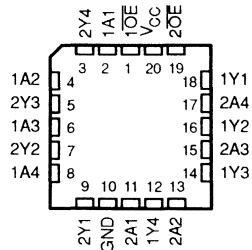
FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
\overline{OE}	A	Y
L	H	H
L	L	L
H	X	Z

SN54LVTZ244 . . . J PACKAGE
SN74LVTZ244 . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVTZ244 . . . FK PACKAGE
(TOP VIEW)



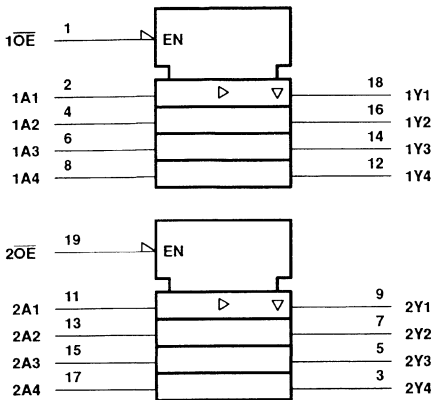
SN54LVTZ244, SN74LVTZ244

3.3-V ABT OCTAL BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

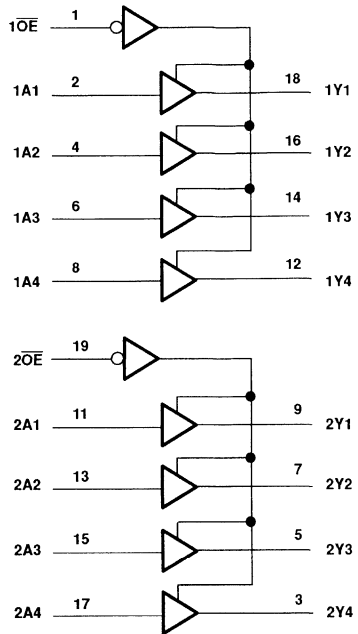
SEPTEMBER 1993

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1)	-0.5 V to 7 V
Current into any output in the low state, I_O : SN54LVTZ244	96 mA
SN74LVTZ244	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTZ244	48 mA
SN74LVTZ244	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DB package	0.5 W
DW package	0.85 W
PW package	0.5 W
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

SN54LVTZ244, SN74LVTZ244
3.3-V ABT OCTAL BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS
 SEPTEMBER 1993

recommended operating conditions

		SN54LVTZ244		SN74LVTZ244		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage		5.5		5.5	V
I _{OH}	High-level output current		-24		-32	mA
I _{OL}	Low-level output current		24		32	mA
I _{OL} †	Low-level output current		48		64	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
Δt/ΔV _{CC}	Power-up ramp rate	200		200		μs/V
T _A	Operating free-air temperature	-55	125	-40	85	°C

† Current duty cycle ≤ 50%, f ≥ 1 kHz

SN54LVTZ244, SN74LVTZ244

3.3-V ABT OCTAL BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

SEPTEMBER 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54LVTZ244		SN74LVTZ244		UNIT		
			MIN	TYP†	MAX	MIN		TYP†	MAX
V_{IK}	$V_{CC} = 2.7 V$,	$I_I = -18 mA$			-1.2		-1.2	V	
V_{OH}	$V_{CC} = \text{MIN to MAX}^\ddagger$,	$I_{OH} = -100 \mu A$	$V_{CC} - 0.2$		$V_{CC} - 0.2$			V	
	$V_{CC} = 2.7 V$,	$I_{OH} = -8 mA$	2.4		2.4				
	$V_{CC} = 3 V$,	$I_{OH} = -24 mA$	2						
	$V_{CC} = 3 V$,	$I_{OH} = -32 mA$			2				
V_{OL}	$V_{CC} = 2.7 V$,	$I_{OL} = 100 \mu A$		0.2		0.2	V		
	$V_{CC} = 2.7 V$,	$I_{OL} = 24 mA$		0.5		0.5			
	$V_{CC} = 3 V$,	$I_{OL} = 16 mA$		0.4		0.4			
	$V_{CC} = 3 V$,	$I_{OL} = 32 mA$		0.5		0.5			
	$V_{CC} = 3 V$,	$I_{OL} = 48 mA$		0.55					
	$V_{CC} = 3 V$,	$I_{OL} = 64 mA$				0.55			
I_I	$V_{CC} = 0 \text{ or } \text{MAX}^\ddagger$,	$V_I = 5.5 V$		10		10	μA		
	$V_{CC} = 0 \text{ to } 3.6 V$,	$V_I = V_{CC} \text{ or } \text{GND}$	Control pins	± 1		± 1			
	$V_{CC} = 0 \text{ to } 3.6 V$,	$V_I = V_{CC}$	Data pins	1		1			
	$V_{CC} = 0 \text{ to } 3.6 V$,	$V_I = 0$		-5		-5			
I_{off}	$V_{CC} = 0 V$,	$V_I \text{ or } V_O = 0 \text{ to } 4.5 V$				± 100	μA		
I_{OZPU}^\S	$V_{CC} = 0 V \text{ to } 1.5 V$,	$V_O = 0.5 \text{ to } 3 V$,	$\overline{OE} = 0.8 V$			± 50	μA		
I_{OZPD}^\S	$V_{CC} = 1.5 V \text{ to } 0$,	$V_O = 0.5 \text{ to } 3 V$,	$\overline{OE} = 0.8 V$			± 50	μA		
$I_I(\text{hold})$	$V_{CC} = 3 V$	$V_I = 0.8 V$	A inputs	75		75	μA		
		$V_I = 2 V$		-75		-75			
I_{OZH}	$V_{CC} = 1.5 V \text{ to } 3.6 V$,	$V_O = 3 V$		5		5	μA		
I_{OZL}	$V_{CC} = 1.5 V \text{ to } 3.6 V$,	$V_O = 0.5 V$		-5		-5	μA		
I_{CC}	$V_{CC} = 3.6 V$,	$I_O = 0$,	$V_I = V_{CC} \text{ or } \text{GND}$	Outputs high	0.12	0.5	0.12	0.225	mA
				Outputs low	8.6	14	8.6	12	
				Outputs disabled	0.12	0.5	0.12	0.225	
ΔI_{CC}^\S	$V_{CC} = 3 V \text{ to } 3.6 V$,	One input at $V_{CC} - 0.6 V$,		0.3		0.2	mA		
C_i	$V_I = 3 V \text{ or } 0$			4		4	pF		
C_o	$V_O = 3 V \text{ or } 0$			8		8	pF		

† All typical values are at $V_{CC} = 3.3 V$, $T_A = 25^\circ C$.

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

¶ This parameter is guaranteed by characterization.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



SN54LVTZ244, SN74LVTZ244
3.3-V ABT OCTAL BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS
SEPTEMBER 1993

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$
(unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTZ244			SN74LVTZ244				UNIT
			$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CC} = 2.7 \text{ V}$	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CC} = 2.7 \text{ V}$		
			MIN	MAX	MAX	MIN	TYP†	MAX	MAX	
t_{PLH}	A	Y	1	4.7	5.2	1	2.5	4.1	5	ns
t_{PHL}			1	4.4	5.4	1	2.5	4.1	5.2	
t_{PZH}	\overline{OE}	Y	1	5.4	6.5	1	2.7	5.2	6.3	ns
t_{PZL}			1.1	5.4	7.6	1.1	3.1	5.2	6.7	
t_{PHZ}	\overline{OE}	Y	1.9	6.2	6.9	1.9	3.9	5.6	6.3	ns
t_{PLZ}			1.8	5.5	6	1.8	3.2	5.1	5.6	

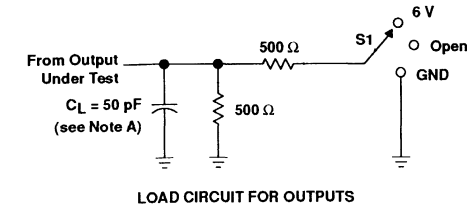
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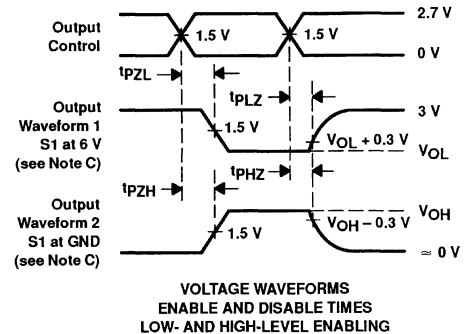
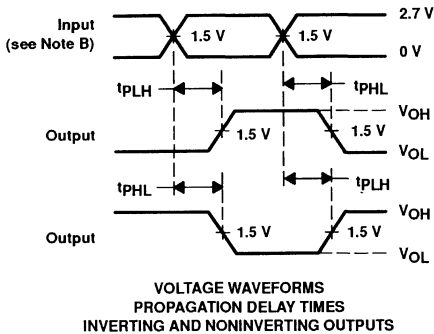
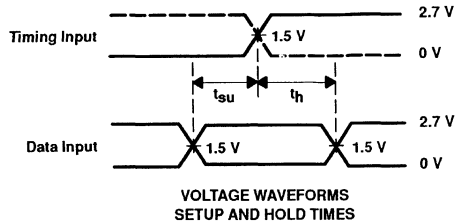
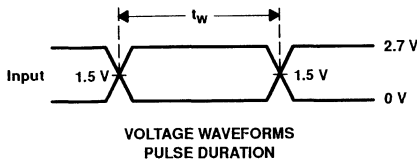
SN54LVTZ244, SN74LVTZ244
3.3-V ABT OCTAL BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

SEPTEMBER 1993

PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SN54LVT245, SN74LVT245 3.3-V ABT OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS130B – D4504, MAY 1992 – REVISED AUGUST 1993

- State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Package Options Include Plastic Small-Outline (SOIC), Shrink Small-Outline (SSOP), and Thin Shrink Small-Outline (TSSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs

description

These octal bus transceivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVT245 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so the buses are effectively isolated.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

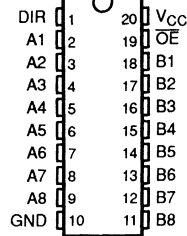
The SN74LVT245 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT245 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVT245 is characterized for operation from -40°C to 85°C .

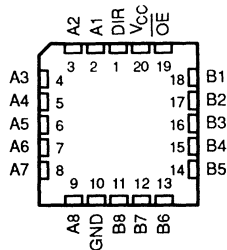
FUNCTION TABLE

INPUTS		OPERATION
\overline{OE}	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

SN54LVT245 ... J PACKAGE
SN74LVT245 ... DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVT245 ... FK PACKAGE
(TOP VIEW)

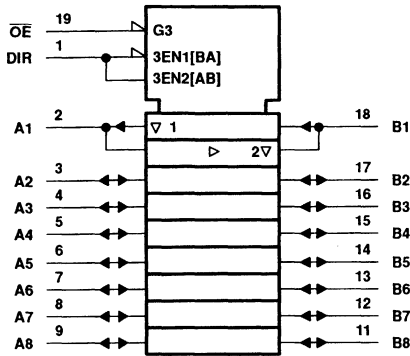


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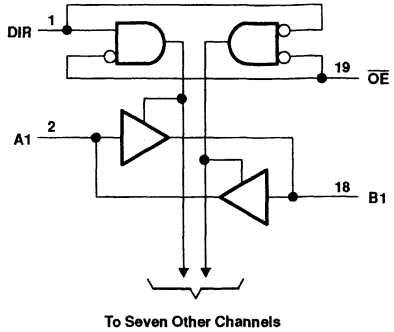
SN54LVT245, SN74LVT245 3.3-V ABT OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS130B – D4504, MAY 1992 – REVISED AUGUST 1993

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1)	-0.5 V to 7 V
Current into any output in the low state, I_O : SN54LVT245	96 mA
SN74LVT245	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT245	48 mA
SN74LVT245	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DB package	0.65 W
DW package	0.85 W
PW package	0.6 W
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

SN54LVT245, SN74LVT245

3.3-V ABT OCTAL BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

SCBS130B – D4504, MAY 1992 – REVISED AUGUST 1993

recommended operating conditions

		SN54LVT245		SN74LVT245		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage		5.5		5.5	V
I _{OH}	High-level output current		-24		-32	mA
I _{OL}	Low-level output current		24		32	mA
I _{OL} †	Low-level output current		48		64	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
T _A	Operating free-air temperature	-55	125	-40	85	°C

† Current duty cycle ≤ 50%, f ≥ 1 kHz

SN54LVT245, SN74LVT245

3.3-V ABT OCTAL BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

SCBS130B – D4504, MAY 1992 – REVISED AUGUST 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54LVT245			SN74LVT245			UNIT	
			MIN	TYP†	MAX	MIN	TYP†	MAX		
V_{IK}	$V_{CC} = 2.7\text{ V}$, $I_I = -18\text{ mA}$				-1.2			-1.2	V	
V_{OH}	$V_{CC} = \text{MIN to MAX}^\ddagger$, $I_{OH} = -100\text{ }\mu\text{A}$		$V_{CC} - 0.2$			$V_{CC} - 0.2$			V	
	$V_{CC} = 2.7\text{ V}$, $I_{OH} = -8\text{ mA}$		2.4			2.4				
	$V_{CC} = 3\text{ V}$, $I_{OH} = -24\text{ mA}$		2							
	$V_{CC} = 3\text{ V}$, $I_{OH} = -32\text{ mA}$					2				
V_{OL}	$V_{CC} = 2.7\text{ V}$, $I_{OL} = 100\text{ }\mu\text{A}$					0.2			V	
	$V_{CC} = 2.7\text{ V}$, $I_{OL} = 24\text{ mA}$					0.5				
	$V_{CC} = 3\text{ V}$, $I_{OL} = 16\text{ mA}$					0.4				
	$V_{CC} = 3\text{ V}$, $I_{OL} = 32\text{ mA}$					0.5				
	$V_{CC} = 3\text{ V}$, $I_{OL} = 48\text{ mA}$					0.55				
	$V_{CC} = 3\text{ V}$, $I_{OL} = 64\text{ mA}$					0.55				
I_I	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}$ or GND		Control pins				± 1			μA
	$V_{CC} = 0$ or MAX^\ddagger , $V_I = 5.5\text{ V}$						10			
	$V_{CC} = 3.6\text{ V}$, $V_I = 5.5\text{ V}$		A or B ports§				100			
	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}$						5			
	$V_{CC} = 3.6\text{ V}$, $V_I = 0$						-10			
I_{off}	$V_{CC} = 0$, V_I or $V_O = 0$ to 4.5 V					± 100			μA	
$I_I(\text{hold})$	$V_{CC} = 3\text{ V}$		A or B ports	$V_I = 0.8\text{ V}$		75		75		μA
				$V_I = 2\text{ V}$		-75		-75		
I_{OZH}	$V_{CC} = 3.6\text{ V}$, $V_O = 3\text{ V}$					1			μA	
I_{OZL}	$V_{CC} = 3.6\text{ V}$, $V_O = 0.5\text{ V}$					-1			μA	
I_{CC}	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}$ or GND, $I_O = 0$		Outputs high	0.13 0.5		0.13 0.19		mA		
			Outputs low	8.8 14		8.8 12				
			Outputs disabled	0.13 0.5		0.13 0.19				
$\Delta I_{CC}\P$	$V_{CC} = 3\text{ V}$ to 3.6 V , One input at $V_{CC} - 0.6\text{ V}$, Other inputs at V_{CC} or GND					0.3		0.2		mA
C_i	$V_I = 3\text{ V}$ or 0					4		4		pF
C_{iO}	$V_O = 3\text{ V}$ or 0					10		10		pF

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ Unused pins at V_{CC} or GND

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

SN54LVT245, SN74LVT245
3.3-V ABT OCTAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

SCBS130B – D4504, MAY 1992 – REVISED AUGUST 1993

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

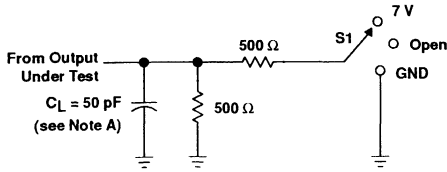
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT245			SN74LVT245				UNIT
			$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CC} = 2.7 \text{ V}$	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CC} = 2.7 \text{ V}$		
			MIN	MAX	MAX	MIN	TYP†	MAX	MAX	
t_{PLH}	A or B	B or A	0.5	4.4	5.2	1	2.4	4	4.7	ns
t_{PHL}			0.5	4.2	4.8	1	2.4	4	4.6	
t_{PZH}	\overline{OE}	A or B	0.8	5.9	7.3	1.1	3.4	5.5	7.1	ns
t_{PZL}			1	5.9	7.2	1.5	3.6	5.5	6.5	
t_{PHZ}	\overline{OE}	A or B	1.5	6.5	7.2	2.2	4.3	5.9	6.5	ns
t_{PLZ}			1.5	6.1	6.5	2	3.5	4.8	4.8	

† All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.

SN54LVT245, SN74LVT245 3.3-V ABT OCTAL BUS TRANSCIEVERS WITH 3-STATE OUTPUTS

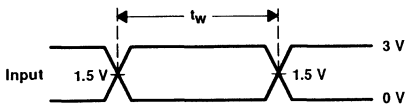
SCBS130B - D4504, MAY 1992 - REVISED AUGUST 1993

PARAMETER MEASUREMENT INFORMATION

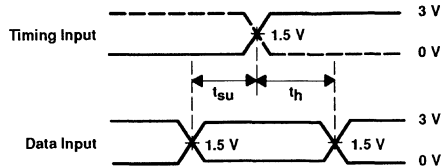


LOAD CIRCUIT FOR OUTPUTS

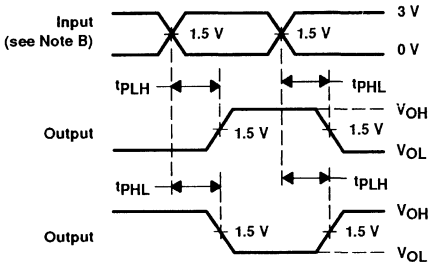
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



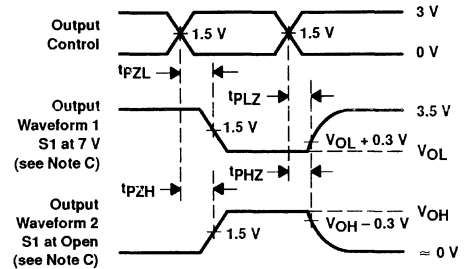
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SN54LVTZ245, SN74LVTZ245 3.3-V ABT OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

NOVEMBER 1993

- State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- High-Impedance State During Power Up and Power Down
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Package Options Include Plastic Small-Outline (SOIC), Shrink Small-Outline (SSOP), and Thin Shrink Small-Outline (TSSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs

description

These octal bus transceivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The LVTZ245 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so the buses are effectively isolated.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

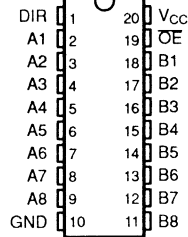
The SN74LVTZ245 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVTZ245 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVTZ245 is characterized for operation from -40°C to 85°C .

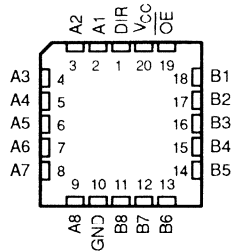
FUNCTION TABLE

INPUTS		OPERATION
\overline{OE}	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

SN54LVTZ245 . . . J PACKAGE
SN74LVTZ245 . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVTZ245 . . . FK PACKAGE
(TOP VIEW)

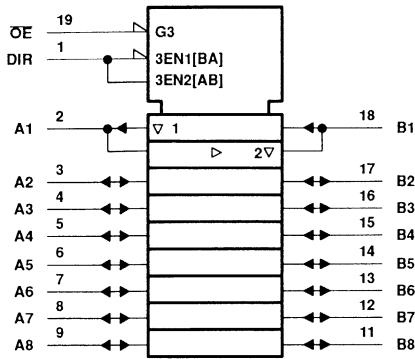


PRODUCT PREVIEW

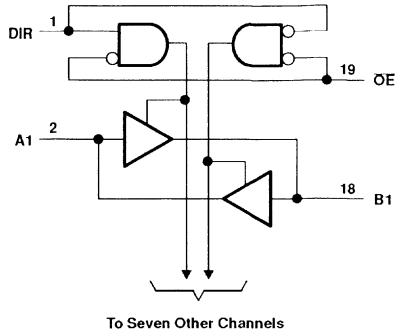
SN54LVTZ245, SN74LVTZ245
3.3-V ABT OCTAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

NOVEMBER 1993

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1)	-0.5 V to 7 V
Current into any output in the low state, I_{OL} : SN54LVTZ245	96 mA
SN74LVTZ245	128 mA
Current into any output in the high state, I_{OH} (see Note 2): SN54LVTZ245	48 mA
SN74LVTZ245	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DB package	0.65 W
DW package	0.85 W
PW package	0.6 W
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

PRODUCT PREVIEW

SN54LVTZ245, SN74LVTZ245
3.3-V ABT OCTAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

NOVEMBER 1993

recommended operating conditions

		SN54LVTZ245		SN74LVTZ245		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current		-24		-32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μ s/V
T_A	Operating free-air temperature	-55	125	-40	85	$^{\circ}$ C

PRODUCT PREVIEW

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



SN54LVTZ245, SN74LVTZ245
3.3-V ABT OCTAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

NOVEMBER 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54LVTZ245			SN74LVTZ245			UNIT	
			MIN	TYP†	MAX	MIN	TYP†	MAX		
V_{IK}	$V_{CC} = 2.7\text{ V}$, $I_I = -18\text{ mA}$		-1.2			-1.2			V	
V_{OH}	$V_{CC} = \text{MIN to MAX}^\ddagger$, $I_{OH} = -100\ \mu\text{A}$		$V_{CC} - 0.2$			$V_{CC} - 0.2$			V	
	$V_{CC} = 2.7\text{ V}$, $I_{OH} = -8\text{ mA}$		2.4			2.4				
	$V_{CC} = 3\text{ V}$, $I_{OH} = -24\text{ mA}$		2							
	$V_{CC} = 3\text{ V}$, $I_{OH} = -32\text{ mA}$					2				
V_{OL}	$V_{CC} = 2.7\text{ V}$, $I_{OL} = 100\ \mu\text{A}$					0.2			V	
	$V_{CC} = 2.7\text{ V}$, $I_{OL} = 24\text{ mA}$					0.5				
	$V_{CC} = 3\text{ V}$, $I_{OL} = 16\text{ mA}$					0.4				
	$V_{CC} = 3\text{ V}$, $I_{OL} = 32\text{ mA}$					0.5				
	$V_{CC} = 3\text{ V}$, $I_{OL} = 48\text{ mA}$					0.55				
	$V_{CC} = 3\text{ V}$, $I_{OL} = 64\text{ mA}$					0.55				
I_I	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}\text{ or GND}$		Control pins			± 1		± 1		μA
	$V_{CC} = 0\text{ or MAX}^\ddagger$, $V_I = 5.5\text{ V}$					10		10		
	$V_{CC} = 3.6\text{ V}$, $V_I = 5.5\text{ V}$		A or B ports §			100		20		
	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}$					5		5		
	$V_{CC} = 3.6\text{ V}$, $V_I = 0$				-10		-10			
I_{off}	$V_{CC} = 0$, $V_I\text{ or }V_O = 0\text{ to }4.5\text{ V}$						± 100		μA	
I_{OZPD}^f	$V_{CC} = 0\text{ V to }1.5\text{ V}$, $V_O = 0.5\text{ V to }3\text{ V}$, $\overline{OE} = 0.8\text{ V}$						± 50		μA	
I_{OZPD}^f	$V_{CC} = 1.5\text{ V to }0$, $V_O = 0.5\text{ V to }3\text{ V}$, $\overline{OE} = 0.8\text{ V}$						± 50		μA	
$I_{I(\text{hold})}$	$V_{CC} = 3\text{ V}$		$V_I = 0.8\text{ V}$		A or B ports	75		75		μA
			$V_I = 2\text{ V}$			-75		-75		
I_{OZH}	$V_{CC} = 3.6\text{ V}$, $V_O = 3\text{ V}$				1		1		μA	
I_{OZL}	$V_{CC} = 3.6\text{ V}$, $V_O = 0.5\text{ V}$				-1		-1		μA	
I_{CC}	$V_{CC} = 3.6\text{ V}$, $I_O = 0$, $V_I = V_{CC}\text{ or GND}$		Outputs high		0.13	0.5	0.13	0.19	mA	
			Outputs low		8.8	14	8.8	12		
			Outputs disabled		0.13	0.5	0.13	0.19		
ΔI_{CC}^\natural	$V_{CC} = 3\text{ V to }3.6\text{ V}$, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at $V_{CC}\text{ or GND}$				0.3		0.2		mA	
C_i	$V_I = 3\text{ V or }0$				4		4		pF	
C_{io}	$V_O = 3\text{ V or }0$				10		10		pF	

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ Unused pins at $V_{CC}\text{ or GND}$

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}\text{ or GND}$.

‡ This parameter is guaranteed by characterization.

PRODUCT PREVIEW

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



SN54LVTZ245, SN74LVTZ245
3.3-V ABT OCTAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS
NOVEMBER 1993

switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTZ245			SN74LVTZ245				UNIT
			$V_{CC} = 3.3 V \pm 0.3 V$		$V_{CC} = 2.7 V$	$V_{CC} = 3.3 V \pm 0.3 V$		$V_{CC} = 2.7 V$		
			MIN	MAX	MAX	MIN	TYP†	MAX	MAX	
t_{PLH}	A or B	B or A	1	4.6	5.3	1	2.5	4	5.2	ns
t_{PHL}			1	4.1	5.7	1	2.5	4	5.5	
t_{PZH}	OE	A or B	1.1	6.1	7.2	1.1	3.3	5.9	7.1	ns
t_{PZL}			1.5	6.6	8	1.5	3.8	6.5	7.9	
t_{PHZ}	OE	A or B	2.2	6.2	7	2.2	4.3	5.9	6.5	ns
t_{PLZ}			2	6.3	5.9	2	3.9	5.5	5.6	

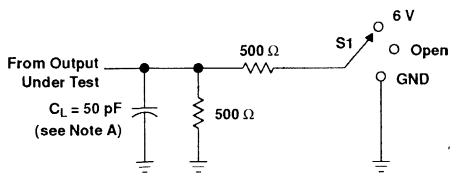
† All typical values are at $V_{CC} = 3.3 V$, $T_A = 25^\circ C$.

PRODUCT PREVIEW

SN54LVTZ245, SN74LVTZ245
3.3-V ABT OCTAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

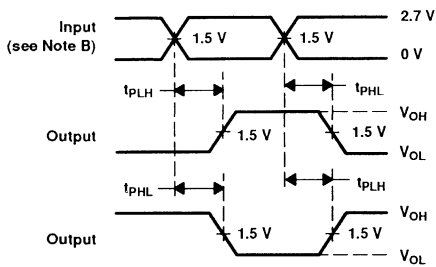
NOVEMBER 1993

PARAMETER MEASUREMENT INFORMATION

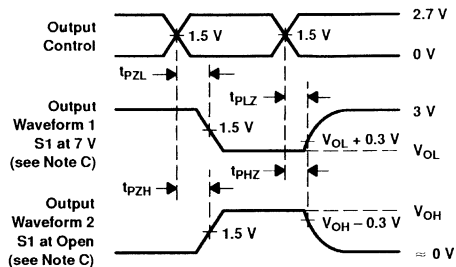


LOAD CIRCUIT FOR OUTPUTS

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
 PROPAGATION DELAY TIMES
 INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
 ENABLE AND DISABLE TIMES
 LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

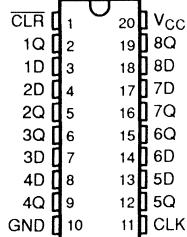
PRODUCT PREVIEW

SN54LVT273, SN74LVT273 3.3-V ABT OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

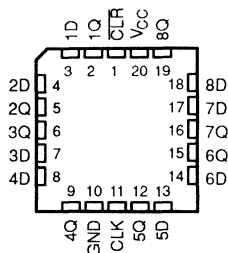
SCBS136B - MAY 1992 - REVISED MARCH 1993

- State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- Buffered Clock and Direct Clear Inputs
- Individual Data Input to Each Flip-Flop
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Package Options Include Plastic Small-Outline (SOIC), Shrink Small-Outline (SSOP), and Thin Shrink Small-Outline (TSSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs

SN54LVT273 ... J PACKAGE
SN74LVT273 ... DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVT273 ... FK PACKAGE
(TOP VIEW)



description

These octal D-type flip-flops are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVT273 is a positive-edge-triggered flip-flop with a direct clear input. Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock (CLK) input is at either the high or low level, the D-input signal has no effect at the output.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVT273 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT273 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVT273 is characterized for operation from -40°C to 85°C .

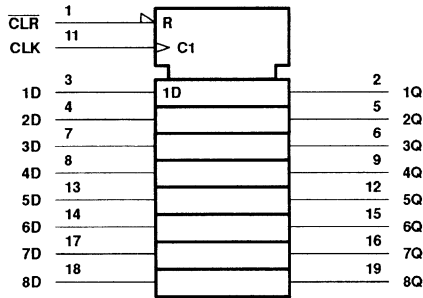
SN54LVT273, SN74LVT273
3.3-V ABT OCTAL D-TYPE FLIP-FLOPS
WITH CLEAR

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FUNCTION TABLE
 (each flip-flop)

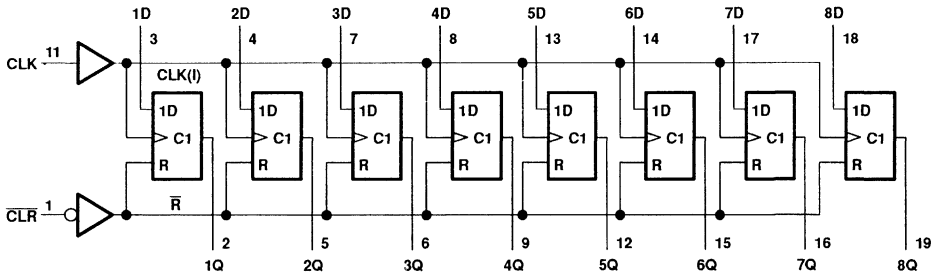
INPUTS			OUTPUT
CLR	CLK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	H or L	X	Q ₀

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN54LVT273, SN74LVT273
3.3-V ABT OCTAL D-TYPE FLIP-FLOPS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Current into any output in the low state, I_O : SN54LVT273	96 mA
SN74LVT273	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT273	48 mA
SN74LVT273	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DB package	0.65 W
DW package	0.85 W
PW package	0.6 W
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp current ratings are observed.
 2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions

		SN54LVT273		SN74LVT273		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current		–24		32	mA
I_{OL}	Low-level output current		24		32	mA
I_{OL}^\ddagger	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

‡ Current duty cycle $\leq 50\%$, $f \geq 1$ kHz

SN54LVT273, SN74LVT273

3.3-V ABT OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54LVT273		SN74LVT273		UNIT		
		MIN	TYP†	MAX	MIN		TYP†	MAX
V_{IK}	$V_{CC} = 2.7\text{ V}$, $I_I = -18\text{ mA}$			-1.2			V	
V_{OH}	$V_{CC} = \text{MIN to MAX}^\ddagger$, $I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC} - 0.2$		$V_{CC} - 0.2$			V	
	$V_{CC} = 2.7\text{ V}$, $I_{OH} = -8\text{ mA}$	2.4		2.4				
	$V_{CC} = 3\text{ V}$, $I_{OH} = -24\text{ mA}$	2						
	$V_{CC} = 3\text{ V}$, $I_{OH} = -32\text{ mA}$			2				
V_{OL}	$V_{CC} = 2.7\text{ V}$, $I_{OL} = 100\text{ }\mu\text{A}$			0.2		0.2	V	
	$V_{CC} = 2.7\text{ V}$, $I_{OL} = 24\text{ mA}$			0.5		0.5		
	$V_{CC} = 3\text{ V}$, $I_{OL} = 16\text{ mA}$			0.4		0.4		
	$V_{CC} = 3\text{ V}$, $I_{OL} = 32\text{ mA}$			0.5		0.5		
	$V_{CC} = 3\text{ V}$, $I_{OL} = 48\text{ mA}$			0.55				
	$V_{CC} = 3\text{ V}$, $I_{OL} = 64\text{ mA}$					0.55		
I_I	$V_{CC} = 0\text{ or MAX}^\ddagger$, $V_I = 5.5\text{ V}$			10		10	μA	
	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}\text{ or GND}$	Control pins			± 1	± 1		
	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}$	Data pins			1	1		
	$V_{CC} = 3.6\text{ V}$, $V_I = 0$				-5	-5		
$I_I(\text{hold})$	$V_{CC} = 3\text{ V}$	$V_I = 0.8\text{ V}$	Data inputs	75	75		μA	
		$V_I = 2\text{ V}$		-75	-75			
I_{CC}	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}\text{ or GND}$	$I_O = 0$	Outputs high	0.12	0.19	0.12	0.19	mA
			Outputs low	8.6	12	8.6	12	
ΔI_{CC}^\S	$V_{CC} = 3\text{ V to }3.6\text{ V}$, Other inputs at $V_{CC}\text{ or GND}$			0.2		0.2	mA	
C_i	$V_I = 3\text{ V or }0$					4	pF	
C_o	$V_O = 3\text{ V or }0$					8	pF	

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		SN54LVT273		SN74LVT273		UNIT
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		
		MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			0	150	MHz
t_w	Pulse duration			3.3	3.3	ns
t_{su}	Setup time before CLK†	Data high or low		2.3	2.7	ns
		CLR high		2.7	3.2	
t_h	Hold time after CLK†	Data high or low		0	0	ns

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



SN54LVT273, SN74LVT273
3.3-V ABT OCTAL D-TYPE FLIP-FLOPS
WITH CLEAR

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switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT273			SN74LVT273			UNIT	
			$V_{CC} = 3.3 V \pm 0.3 V$		$V_{CC} = 2.7 V$	$V_{CC} = 3.3 V \pm 0.3 V$		$V_{CC} = 2.7 V$		
			MIN	MAX	MAX	MIN	TYP†	MAX		MAX
f_{max}						150			MHz	
t_{PLH}	CLK	Any Q				1.7	3.5	5.5	6.3	ns
t_{PHL}						1.9	3.5	5.5	5.9	
t_{PHL}	CLR	Any Q				1.3	3.2	5.1	6.2	ns

† All typical values are at $V_{CC} = 3.3 V$, $T_A = 25^\circ C$.

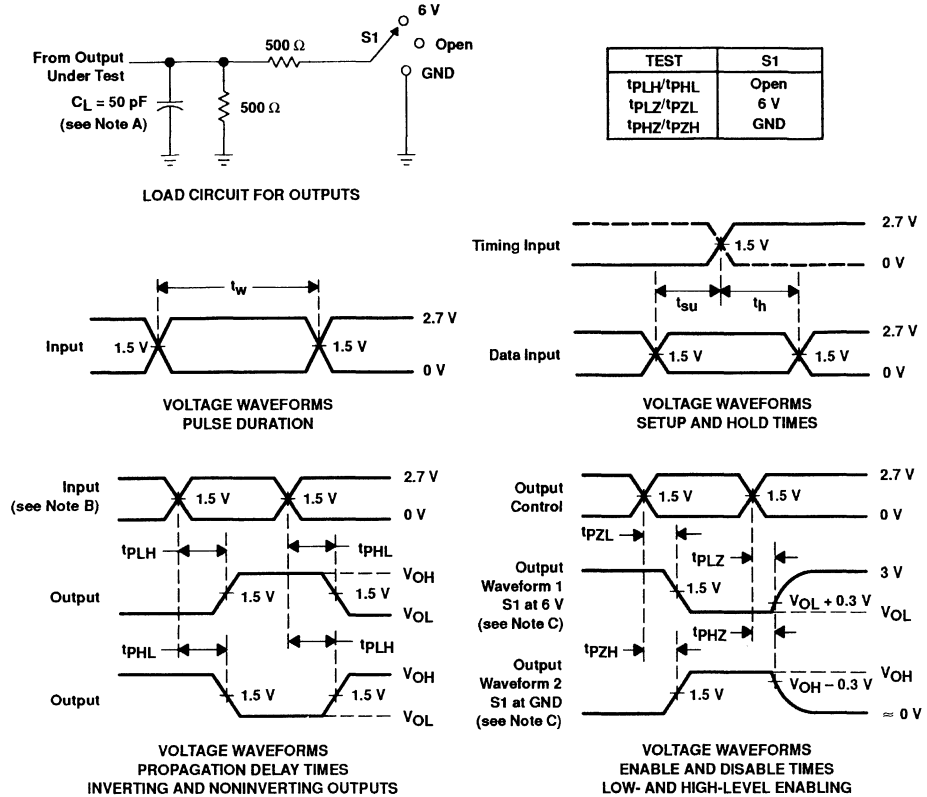
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SN54LVT273, SN74LVT273
3.3-V ABT OCTAL D-TYPE FLIP-FLOPS
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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SN54LVT543, SN74LVT543 3.3-V ABT OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

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- State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Package Options Include Plastic Small-Outline (SOIC), Shrink Small-Outline (SSOP), and Thin Shrink Small-Outline (TSSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs

description

These octal transceivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The LVT543 octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch-enable (\overline{LEAB} or \overline{LEBA}) and output-enable (\overline{OEAB} or \overline{OEBA}) inputs are provided for each register to permit independent control in either direction of data flow.

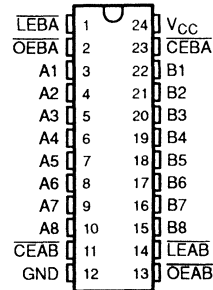
The A-to-B enable (\overline{CEAB}) input must be low in order to enter data from A or to output data from B. If \overline{CEAB} is low and \overline{LEAB} is low, the A-to-B latches are transparent; a subsequent low-to-high transition of \overline{LEAB} puts the A latches in the storage mode. With \overline{CEAB} and \overline{OEAB} both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the \overline{CEBA} , \overline{LEBA} , and \overline{OEBA} inputs.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

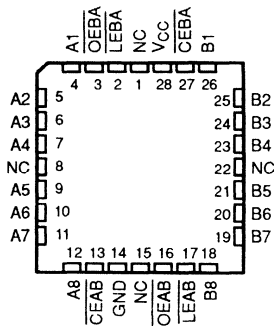
The SN74LVT543 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT543 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVT543 is characterized for operation from -40°C to 85°C .

SN54LVT543 . . . JT PACKAGE
SN74LVT543 . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVT543 . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

SN54LVT543, SN74LVT543

3.3-V ABT OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

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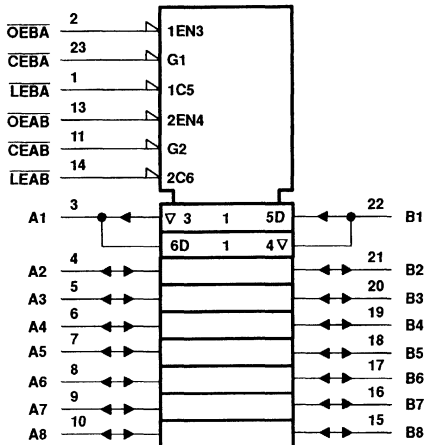
FUNCTION TABLE†

INPUTS				OUTPUT
CEAB	LEAB	OEAB	A	B
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B ₀ ‡
L	L	L	L	L
L	L	L	H	H

† A-to-B data flow is shown; B-to-A flow control is the same except that it uses CEBA, LEBA, and OEBA.

‡ Output level before the indicated steady-state input conditions were established.

logic symbols§

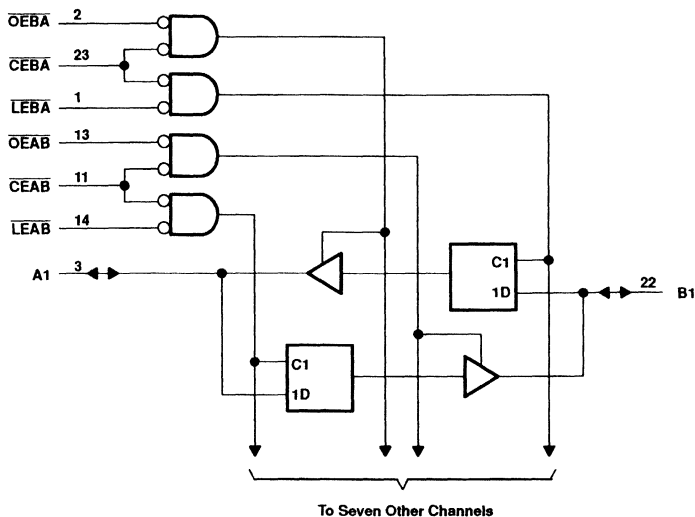


§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DB, DW, JT, and PW packages.

SN54LVT543, SN74LVT543 3.3-V ABT OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

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logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, and PW packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1)	-0.5 V to 7 V
Current into any output in the low state, I_O : SN54LVT543	96 mA
SN74LVT543	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT543	48 mA
SN74LVT543	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DB package	0.7 W
DW package	1 W
PW package	0.65 W
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

SN54LVT543, SN74LVT543
3.3-V ABT OCTAL REGISTERED TRANSCEIVERS
WITH 3-STATE OUTPUTS

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recommended operating conditions

		SN54LVT543		SN74LVT543		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage		5.5		5.5	V
I _{OH}	High-level output current		-24		-32	mA
I _{OL}	Low-level output current		24		32	mA
I _{OL} †	Low-level output current		48		64	mA
Δt/Δv	Input transition rise or fall rate		Outputs enabled		10	ns/V
T _A	Operating free-air temperature	-55	125	-40	85	°C

† Current duty cycle ≤ 50%, f ≥ 1 kHz

SN54LVT543, SN74LVT543 3.3-V ABT OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54LVT543		SN74LVT543		UNIT
			MIN	TYP†	MAX	MIN	
V_{IK}	$V_{CC} = 2.7\text{ V}$, $I_I = -18\text{ mA}$				-1.2		V
V_{OH}	$V_{CC} = \text{MIN to MAX}^\ddagger$, $I_{OH} = -100\ \mu\text{A}$		$V_{CC} - 0.2$		$V_{CC} - 0.2$		V
	$V_{CC} = 2.7\text{ V}$, $I_{OH} = -8\text{ mA}$		2.4		2.4		
	$V_{CC} = 3\text{ V}$, $I_{OH} = -24\text{ mA}$		2				
	$V_{CC} = 3\text{ V}$, $I_{OH} = -32\text{ mA}$				2		
V_{OL}	$V_{CC} = 2.7\text{ V}$, $I_{OL} = 100\ \mu\text{A}$				0.2		V
	$V_{CC} = 2.7\text{ V}$, $I_{OL} = 24\text{ mA}$				0.5		
	$V_{CC} = 3\text{ V}$, $I_{OL} = 16\text{ mA}$				0.4		
	$V_{CC} = 3\text{ V}$, $I_{OL} = 32\text{ mA}$				0.5		
	$V_{CC} = 3\text{ V}$, $I_{OL} = 48\text{ mA}$				0.55		
	$V_{CC} = 3\text{ V}$, $I_{OL} = 64\text{ mA}$				0.55		
I_I	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}\text{ or GND}$		Control pins		±1		μA
	$V_{CC} = 0\text{ or MAX}^\ddagger$, $V_I = 5.5\text{ V}$				10		
	$V_{CC} = 3.6\text{ V}$, $V_I = 5.5\text{ V}$		A or B ports§		20		
	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}$				5		
	$V_{CC} = 3.6\text{ V}$, $V_I = 0$				-10		
I_{off}	$V_{CC} = 0$, $V_I\text{ or }V_O = 0\text{ to }4.5\text{ V}$				±100		μA
$I_{I(\text{hold})}$	$V_{CC} = 3\text{ V}$		A or B ports		75		μA
					-75		
I_{OZH}	$V_{CC} = 3.6\text{ V}$, $V_O = 3\text{ V}$				1		μA
I_{OZL}	$V_{CC} = 3.6\text{ V}$, $V_O = 0.5\text{ V}$				-1		μA
I_{CC}	$V_{CC} = 3.6\text{ V}$, $I_O = 0$, $V_I = V_{CC}\text{ or GND}$		Outputs high		0.13 0.19		mA
			Outputs low		8.8 12		
			Outputs disabled		0.13 0.19		
ΔI_{CC}^\ddagger	$V_{CC} = 3\text{ V to }3.6\text{ V}$, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at $V_{CC}\text{ or GND}$				0.2		mA
C_i	$V_I = 3\text{ V or }0$				4.5		pF
C_{iO}	$V_O = 3\text{ V or }0$				11		pF

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ Unused pins at $V_{CC}\text{ or GND}$.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}\text{ or GND}$.

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SN54LVT543, SN74LVT543
3.3-V ABT OCTAL REGISTERED TRANSCEIVERS
WITH 3-STATE OUTPUTS

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			SN54LVT543		SN74LVT543		UNIT	
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	$V_{CC} = 2.7\text{ V}$	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	$V_{CC} = 2.7\text{ V}$		
			MIN	MIN	MIN	MIN		
t_w	Pulse duration	LEAB or LEBA low		3.3	3.3	3.3	3.3	ns
t_{su}	Setup time	Data before LEAB or LEBA↑	High	0	0	0	0	ns
			Low	0.8	1.1	0.8	1.1	
		Data before CEAB or CEBA↑	High	0	0	0	0	
			Low	0.9	1.2	0.9	1.2	
t_h	Hold time	Data after LEAB or LEBA↑		1.7	1.7	1.7	1.7	ns
		Data after CEAB or CEBA↑		1.8	1.8	1.8	1.8	

switching characteristics over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

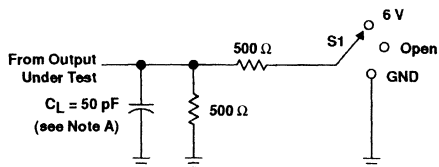
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT543			SN74LVT543			UNIT	
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		
			MIN	MAX	MAX	MIN	TYP†	MAX		MAX
t_{PLH}	A or B	B or A	1	4.9	5.7	1	2.9	4.7	5.5	ns
t_{PHL}			1	4.8	6	1	3.3	4.6	5.8	
t_{PLH}	LE	A or B	1	6.1	7.5	1	4	5.9	7.3	ns
t_{PHL}			1	5.9	7.5	1	4.1	5.7	7.3	
t_{PZH}	OE	A or B	1	6	7.8	1	4.1	5.8	7.6	ns
t_{PZL}			1.1	6.6	8.4	1.1	4.5	6.4	8.2	
t_{PHZ}	OE	A or B	2.4	6.7	7.3	2.4	4.8	6.5	7.1	ns
t_{PLZ}			2	6	6.1	2	4	5.8	5.9	
t_{PZH}	CE	A or B	1	6.2	7.8	1	4.2	6	7.6	ns
t_{PZL}			1.4	6.9	8.5	1.4	4.7	6.7	8.3	
t_{PHZ}	CE	A or B	2.3	6.6	7.3	2.3	4.7	6.4	7.1	ns
t_{PLZ}			2	5.6	5.8	2	3.8	5.4	5.6	

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

SN54LVT543, SN74LVT543 3.3-V ABT OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

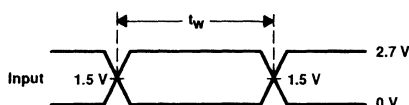
SCBS137A - D4518, MAY 1992 - REVISED MARCH 1993

PARAMETER MEASUREMENT INFORMATION

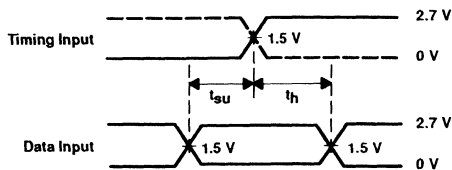


LOAD CIRCUIT FOR OUTPUTS

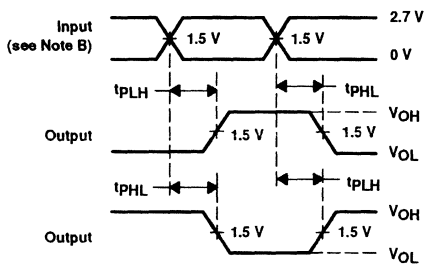
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



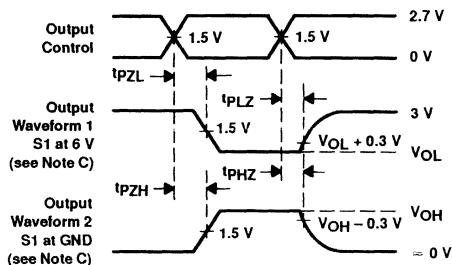
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SN54LVT573, SN74LVT573 3.3-V ABT OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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- State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Package Options Include Plastic Small-Outline (SOIC), Shrink Small-Outline (SSOP), and Thin Shrink Small-Outline (TSSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs

description

These octal latches are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The eight latches of the 'LVT573 are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When the latch enable is taken low, the Q outputs are latched at the logic levels that were set up at the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

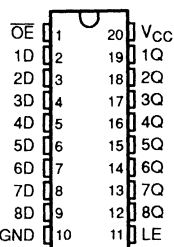
The output-enable (\overline{OE}) input does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

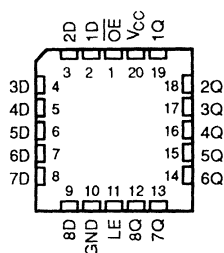
The SN74LVT573 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT573 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVT573 is characterized for operation from -40°C to 85°C .

SN54LVT573 ... J PACKAGE
SN74LVT573 ... DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVT573 ... FK PACKAGE
(TOP VIEW)



SN54LVT573, SN74LVT573

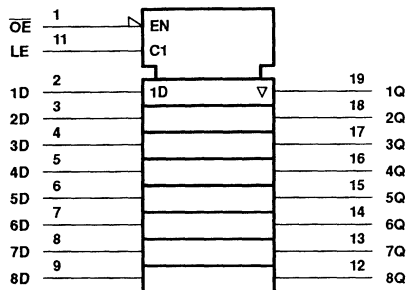
3.3-V ABT OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS138A – MAY 1992 – REVISED MARCH 1993

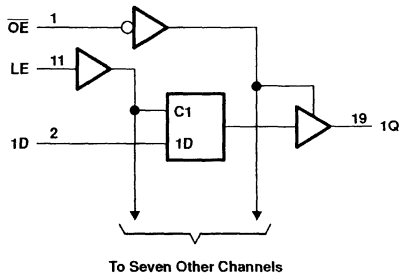
FUNCTION TABLE
(each latch)

INPUTS			OUTPUT
\overline{OE}	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Current into any output in the low state, I_{OL} : SN54LVT573	96 mA
SN74LVT573	128 mA
Current into any output in the high state, I_{OH} (see Note 2): SN54LVT573	48 mA
SN74LVT573	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DB package	0.65 W
DW package	0.85 W
PW package	0.6 W
Storage temperature range	–65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

SN54LVT573, SN74LVT573 3.3-V ABT OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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recommended operating conditions

		SN54LVT573		SN74LVT573		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage		5.5		5.5	V
I _{OH}	High-level output current		-24		-32	mA
I _{OL}	Low-level output current		24		32	mA
I _{OL} [†]	Low-level output current		48		64	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
T _A	Operating free-air temperature	-55	125	-40	85	°C

[†] Current duty cycle ≤ 50%, f ≥ 1 kHz

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



SN54LVT573, SN74LVT573

3.3-V ABT OCTAL TRANSPARENT D-TYPE LATCHES

WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54LVT573			SN74LVT573			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 2.7\text{ V}$, $I_I = -18\text{ mA}$		-1.2			-1.2			V
V_{OH}	$V_{CC} = \text{MIN to MAX}^\ddagger$, $I_{OH} = -100\ \mu\text{A}$		$V_{CC}-0.2$			$V_{CC}-0.2$			V
	$V_{CC} = 2.7\text{ V}$, $I_{OH} = -8\text{ mA}$		2.4			2.4			
	$V_{CC} = 3\text{ V}$, $I_{OH} = -24\text{ mA}$		2						
	$V_{CC} = 3\text{ V}$, $I_{OH} = -32\text{ mA}$					2			
V_{OL}	$V_{CC} = 2.7\text{ V}$, $I_{OL} = 100\ \mu\text{A}$		0.2			0.2			V
	$V_{CC} = 2.7\text{ V}$, $I_{OL} = 24\text{ mA}$		0.5			0.5			
	$V_{CC} = 3\text{ V}$, $I_{OL} = 16\text{ mA}$		0.4			0.4			
	$V_{CC} = 3\text{ V}$, $I_{OL} = 32\text{ mA}$		0.5			0.5			
	$V_{CC} = 3\text{ V}$, $I_{OL} = 48\text{ mA}$		0.55						
	$V_{CC} = 3\text{ V}$, $I_{OL} = 64\text{ mA}$					0.55			
I_I	$V_{CC} = 0\text{ or MAX}^\ddagger$, $V_I = 5.5\text{ V}$		10			10			μA
	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}\text{ or GND}$		Control pins			± 1			
	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}$		Data pins			1			
	$V_{CC} = 3.6\text{ V}$, $V_I = 0$					-5			
I_{off}	$V_{CC} = 0$, $V_I\text{ or }V_O = 0\text{ to }4.5\text{ V}$					± 100			μA
$I_I(\text{hold})$	$V_{CC} = 3\text{ V}$		$V_I = 0.8\text{ V}$		75		75		μA
			$V_I = 2\text{ V}$		-75		-75		
I_{OZH}	$V_{CC} = 3.6\text{ V}$, $V_O = 3\text{ V}$		5			5			μA
I_{OZL}	$V_{CC} = 3.6\text{ V}$, $V_O = 0.5\text{ V}$		-5			-5			μA
I_{CC}	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}\text{ or GND}$, $I_O = 0$		Outputs high		0.13 0.19		0.13 0.19		mA
			Outputs low		8.6 12		8.6 12		
			Outputs disabled		0.13 0.19		0.13 0.19		
ΔI_{CC}^\S	$V_{CC} = 3\text{ V to }3.6\text{ V}$, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at $V_{CC}\text{ or GND}$		0.2			0.2			mA
C_i	$V_I = 3\text{ V or }0$		4			4			pF
C_o	$V_O = 3\text{ V or }0$		8			8			pF

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			SN54LVT573				SN74LVT573				UNIT
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high		3.3		3.3		3.3		3.3		ns
t_{su}	Setup time, data before LE↓		High or low		0.7		0.6		0.7		ns
t_h	Hold time, data after LE↓		High or low		1.6		1.8		1.6		ns

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SN54LVT573, SN74LVT573 3.3-V ABT OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT573			SN74LVT573				UNIT
			$V_{CC} = 3.3 V \pm 0.3 V$		$V_{CC} = 2.7 V$	$V_{CC} = 3.3 V \pm 0.3 V$		$V_{CC} = 2.7 V$		
			MIN	MAX	MAX	MIN	TYP†	MAX	MAX	
t_{PLH}	D	Q	1	4.4	4.9	1	2.5	4.2	4.7	ns
t_{PHL}			1	4.5	5.4	1	2.7	4.3	5.2	
t_{PLH}	LE	Q	1.6	5.8	6.5	1.6	3.5	5.6	6.3	ns
t_{PHL}			2.5	6.7	7.4	2.5	4.3	6.5	7.2	
t_{PZH}	\overline{OE}	Q	1	5.3	6.4	1	2.8	5.1	6.2	ns
t_{PZL}			1.3	5.7	6.8	1.3	3.3	5.5	6.6	
t_{PHZ}	\overline{OE}	Q	2	5.9	6.9	2	3.7	5.7	6.7	ns
t_{PLZ}			1.5	4.8	5.3	1.5	3	4.6	5.1	

† All typical values are at $V_{CC} = 3.3 V$, $T_A = 25^\circ C$.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



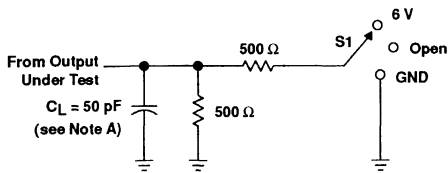
SN54LVT573, SN74LVT573

3.3-V ABT OCTAL TRANSPARENT D-TYPE LATCHES

WITH 3-STATE OUTPUTS

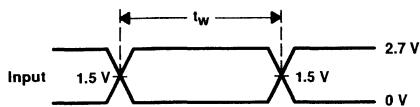
SCBS138A – MAY 1992 – REVISED MARCH 1993

PARAMETER MEASUREMENT INFORMATION

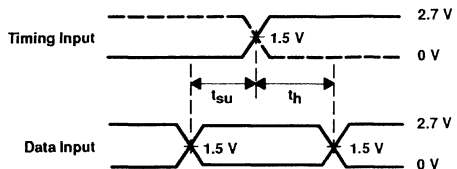


LOAD CIRCUIT FOR OUTPUTS

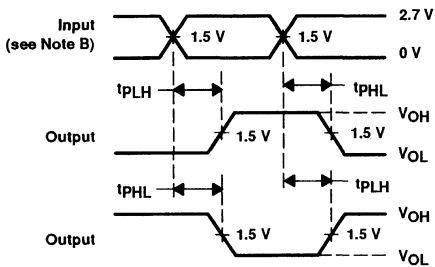
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



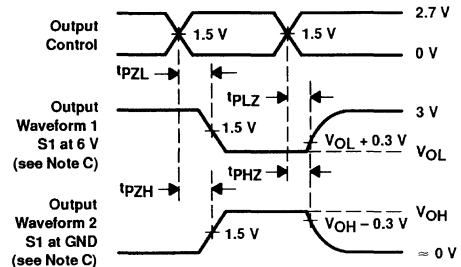
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one transition per measurement.

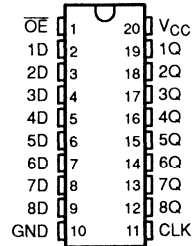
Figure 1. Load Circuit and Voltage Waveforms

SN54LVT574, SN74LVT574 3.3-V ABT OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

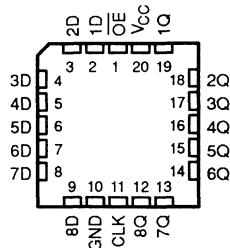
SCBS139A - MAY 1992 - REVISED MARCH 1993

- State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Package Options Include Plastic Small-Outline (SOIC), Shrink Small-Outline (SSOP), and Thin Shrink Small-Outline (TSSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs

SN54LVT574 . . . J PACKAGE
SN74LVT574 . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVT574 . . . FK PACKAGE
(TOP VIEW)



description

These octal flip-flops are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The eight flip-flops of the 'LVT574 are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels that were set up at the data (D) inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (\overline{OE}) input does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVT574 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT574 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVT574 is characterized for operation from -40°C to 85°C .

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SN54LVT574, SN74LVT574

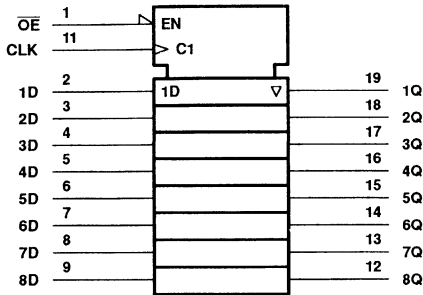
3.3-V ABT OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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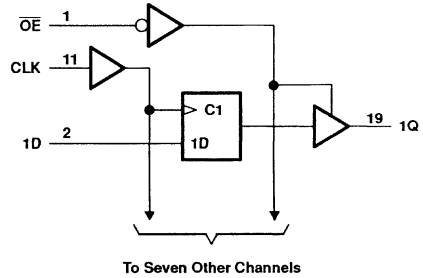
FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
\overline{OE}	CLK	D	Q
L	\uparrow	H	H
L	\uparrow	L	L
L	H or L	X	Q_0
H	X	X	Z

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1)	-0.5 V to 7 V
Current into any output in the low state, I_{OL} : SN54LVT574	96 mA
SN74LVT574	128 mA
Current into any output in the high state, I_{OH} (see Note 2): SN54LVT574	48 mA
SN74LVT574	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DB package	0.65 W
DW package	0.85 W
PW package	0.6 W
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

SN54LVT574, SN74LVT574 3.3-V ABT OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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recommended operating conditions

		SN54LVT574		SN74LVT574		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage		5.5		5.5	V
I _{OH}	High-level output current		-24		-32	mA
I _{OL}	Low-level output current		24		32	mA
I _{OL} †	Low-level output current		48		64	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
T _A	Operating free-air temperature	-55	125	-40	85	°C

† Current duty cycle ≤ 50%, f ≥ 1 kHz

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SN54LVT574, SN74LVT574

3.3-V ABT OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCBS139A – MAY 1992 – REVISED MARCH 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54LVT574		SN74LVT574		UNIT	
			MIN	TYPT [†] MAX	MIN	TYPT [†] MAX		
V _{IK}	V _{CC} = 2.7 V, I _I = -18 mA		-1.2		-1.2		V	
V _{OH}	V _{CC} = MIN to MAX [‡] , I _{OH} = -100 μA		V _{CC} - 0.2		V _{CC} - 0.2		V	
	V _{CC} = 2.7 V, I _{OH} = -8 mA		2.4		2.4			
	V _{CC} = 3 V, I _{OH} = -24 mA		2					
	V _{CC} = 3 V, I _{OH} = -32 mA				2			
V _{OL}	V _{CC} = 2.7 V, I _{OL} = 100 μA		0.2		0.2		V	
	V _{CC} = 2.7 V, I _{OL} = 24 mA		0.5		0.5			
	V _{CC} = 3 V, I _{OL} = 16 mA		0.4		0.4			
	V _{CC} = 3 V, I _{OL} = 32 mA		0.5		0.5			
	V _{CC} = 3 V, I _{OL} = 48 mA		0.55					
	V _{CC} = 3 V, I _{OL} = 64 mA				0.55			
I _I	V _{CC} = 0 or MAX [‡] , V _I = 5.5 V		10		10		μA	
	V _{CC} = 3.6 V, V _I = V _{CC} or GND		±1		±1			
	V _{CC} = 3.6 V, V _I = V _{CC}		1		1			
	V _{CC} = 3.6 V, V _I = 0		-5		-5			
I _{off}	V _{CC} = 0, V _I or V _O = 0 to 4.5 V				±100		μA	
I _{I(hold)}	V _{CC} = 3 V		75		75		μA	
	V _I = 0.8 V		-75		-75			
	V _I = 2 V							
I _{OZH}	V _{CC} = 3.6 V, V _O = 3 V		5		5		μA	
I _{OZL}	V _{CC} = 3.6 V, V _O = 0.5 V		-5		-5		μA	
I _{CC}	V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND		Outputs high		0.13	0.19	0.13	0.19
			Outputs low		8.7	12	8.7	12
			Outputs disabled		0.13	0.19	0.13	0.19
ΔI _{CC} [§]	V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND		0.2		0.2		mA	
C _i	V _I = 3 V or 0		4		4		pF	
C _O	V _O = 3 V or 0		8		8		pF	

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		SN54LVT574				SN74LVT574				UNIT
		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	0	150	0	150	0	150	0	150	MHz
t _w	Pulse duration, CLK high or low	3.3		3.3		3.3		3.3		ns
t _{su}	Setup time, data before CLK [↑]	2		2.4		2		2.4		ns
t _h	Hold time, data after CLK [↑]	0.3		0		0.3		0		ns

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



SN54LVT574, SN74LVT574 3.3-V ABT OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT574				SN74LVT574				UNIT
			$V_{CC} = 3.3 V \pm 0.3 V$		$V_{CC} = 2.7 V$		$V_{CC} = 3.3 V \pm 0.3 V$		$V_{CC} = 2.7 V$		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN	
f_{max}			150		150		150		150		MHz
t_{PLH}	CLK	Q	1.7	5.6	6.4		1.7	3.6	5.4	6.2	
t_{PHL}			2.4	6.1	6.8		2.4	4.3	5.9	6.6	
t_{PZH}	\overline{OE}	Q	1	5	6.1		1	2.9	4.8	5.9	
t_{PZL}			1.3	5.3	6.4		1.3	3.4	5.1	6.2	
t_{PHZ}	\overline{OE}	Q	1.9	5.3	6.1		1.9	4	5.5	5.9	
t_{PLZ}			1.7	4.7	4.7		1.7	3.2	4.5	4.5	

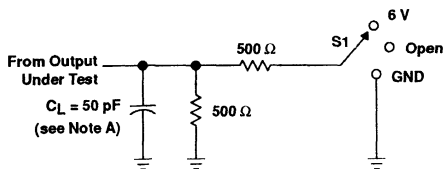
† All typical values are at $V_{CC} = 3.3 V$, $T_A = 25^\circ C$.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



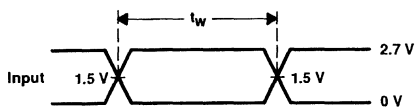
SN54LVT574, SN74LVT574
3.3-V ABT OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS
WITH 3-STATE OUTPUTS
 SCBS139A – MAY 1992 – REVISED MARCH 1993

PARAMETER MEASUREMENT INFORMATION

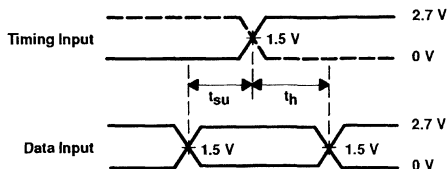


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

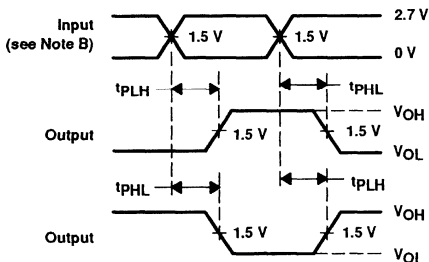
LOAD CIRCUIT FOR OUTPUTS



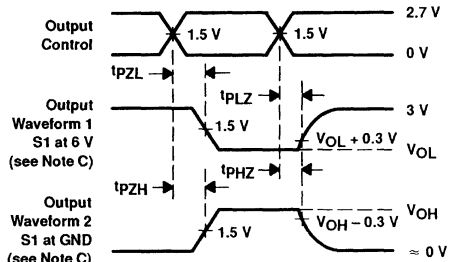
**VOLTAGE WAVEFORMS
 PULSE DURATION**



**VOLTAGE WAVEFORMS
 SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
 PROPAGATION DELAY TIMES
 INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS
 ENABLE AND DISABLE TIMES
 LOW- AND HIGH-LEVEL ENABLING**

- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



SN54LVT646, SN74LVT646

3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Package Options Include Plastic Small-Outline (SOIC), Shrink Small-Outline (SSOP), and Thin Shrink Small-Outline (TSSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs

description

These bus transceivers and registers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVT646 consists of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'LVT646.

Output-enable (\overline{OE}) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both.

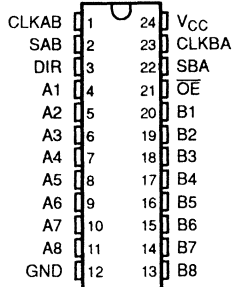
The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The direction control (DIR) determines which bus receives data when \overline{OE} is low. In the isolation mode (\overline{OE} high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

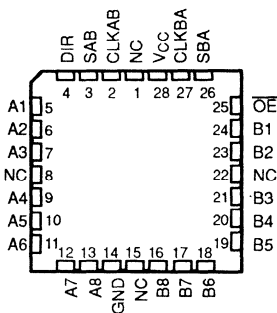
Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVT646 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

SN54LVT646 ... JT PACKAGE
SN74LVT646 ... DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVT646 ... FK PACKAGE
(TOP VIEW)



NC – No internal connection

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description (continued)

The SN54LVT646 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT646 is characterized for operation from –40°C to 85°C.

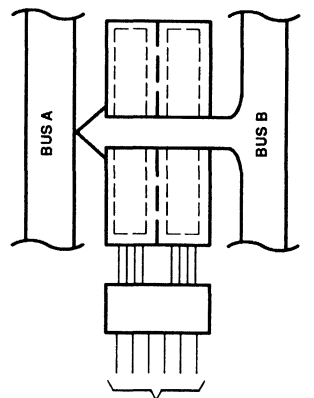
FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION
\overline{OE}	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	L	L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	L	X	H	X	Input	Output	Stored A data to B bus

† The data output functions may be enabled or disabled by various signals at the \overline{OE} and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.

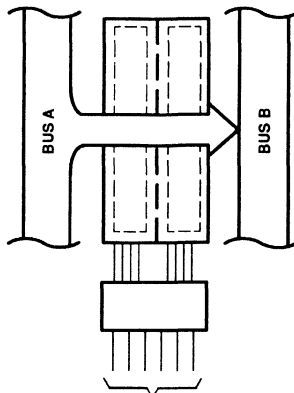
SN54LVT646, SN74LVT646 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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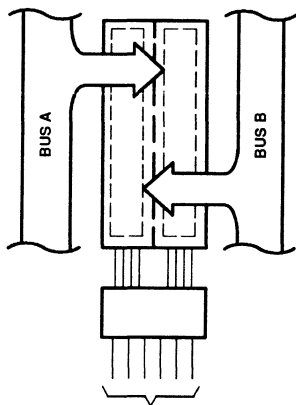
21	3	1	23	2	22
\overline{OE}	DIR	CLKAB	CLKBA	SAB	SBA
L	L	X	X	X	L

**REAL-TIME TRANSFER
BUS B TO BUS A**



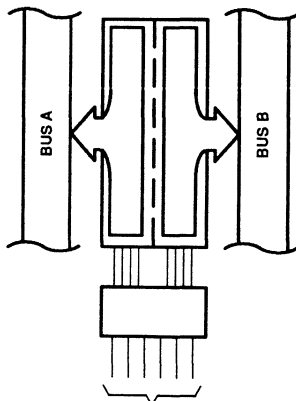
21	3	1	23	2	22
\overline{OE}	DIR	CLKAB	CLKBA	SAB	SBA
L	H	X	X	L	X

**REAL-TIME TRANSFER
BUS A TO BUS B**



21	3	1	23	2	22
\overline{OE}	DIR	CLKAB	CLKBA	SAB	SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

**STORAGE FROM
A, B, OR A AND B**



21	3	1	23	2	22
\overline{OE}	DIR	CLKAB	CLKBA	SAB	SBA
L	L	X	L	X	H
L	H	L	X	H	X

**TRANSFER STORED DATA
TO A AND/OR B**

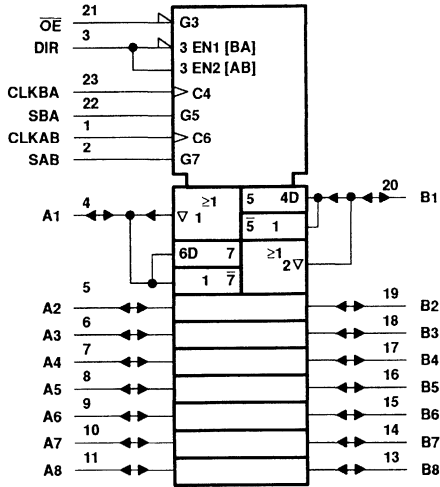
Figure 1. Bus-Management Functions

Pin numbers shown are for the DB, DW, JT, and PW packages.

SN54LVT646, SN74LVT646
3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS
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logic symbol†

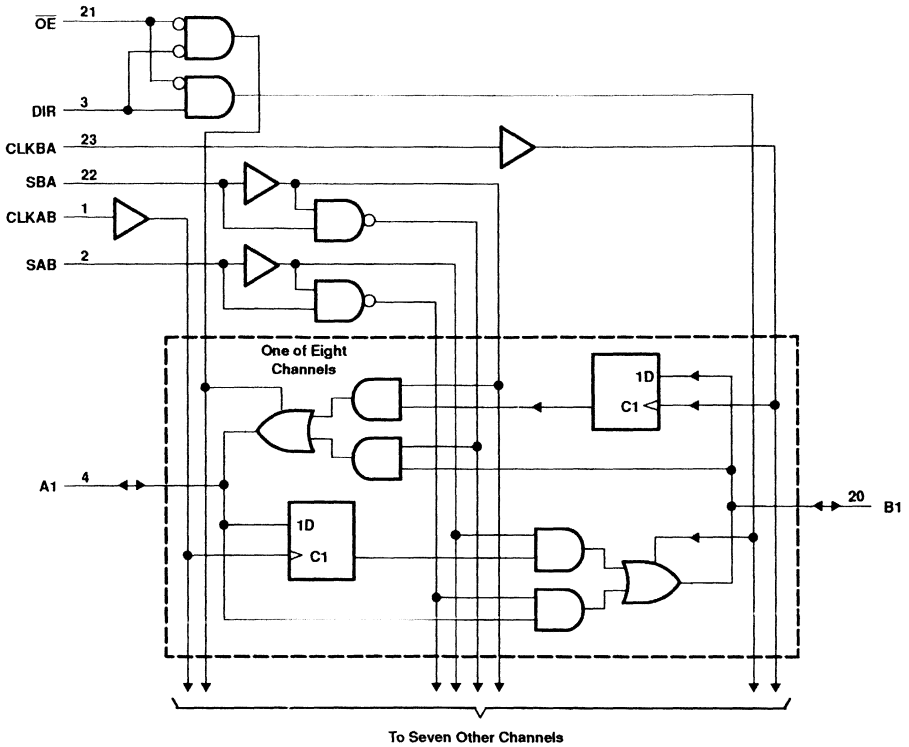


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
 Pin numbers shown are for the DB, DW, JT, and PW packages.

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logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, and PW packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1)	-0.5 V to 7 V
Current into any output in the low state, I_O : SN54LVT646	96 mA
SN74LVT646	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT646	48 mA
SN74LVT646	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DB package	0.7 W
DW package	1 W
PW package	0.65 W
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions

		SN54LVT646		SN74LVT646		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current		-24		-32	mA
I_{OL}	Low-level output current		24		32	mA
I_{OL}^\ddagger	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
T_A	Operating free-air temperature	-55	125	-40	85	°C

‡ Current duty cycle $\leq 50\%$, $f \geq 1$ kHz



SN54LVT646, SN74LVT646

3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54LVT646		SN74LVT646		UNIT	
			MIN	TYP†	MAX	MIN		TYP†
V_{IK}	$V_{CC} = 2.7\text{ V}$, $I_I = -18\text{ mA}$				-1.2		V	
V_{OH}	$V_{CC} = \text{MIN to MAX}^\ddagger$, $I_{OH} = -100\ \mu\text{A}$		$V_{CC} - 0.2$		$V_{CC} - 0.2$		V	
	$V_{CC} = 2.7\text{ V}$, $I_{OH} = -8\text{ mA}$		2.4		2.4			
	$V_{CC} = 3\text{ V}$, $I_{OH} = -24\text{ mA}$		2					
	$V_{CC} = 3\text{ V}$, $I_{OH} = -32\text{ mA}$				2			
V_{OL}	$V_{CC} = 2.7\text{ V}$, $I_{OL} = 100\ \mu\text{A}$				0.2		V	
	$V_{CC} = 2.7\text{ V}$, $I_{OL} = 24\text{ mA}$				0.5			
	$V_{CC} = 3\text{ V}$, $I_{OL} = 16\text{ mA}$				0.4			
	$V_{CC} = 3\text{ V}$, $I_{OL} = 32\text{ mA}$				0.5			
	$V_{CC} = 3\text{ V}$, $I_{OL} = 48\text{ mA}$				0.55			
	$V_{CC} = 3\text{ V}$, $I_{OL} = 64\text{ mA}$				0.55			
I_I	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}$ or GND		Control pins			± 1		μA
	$V_{CC} = 0$ or MAX^\ddagger , $V_I = 5.5\text{ V}$					10		
	$V_{CC} = 3.6\text{ V}$, $V_I = 5.5\text{ V}$		A or B ports§			100		
	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}$					5		
	$V_{CC} = 3.6\text{ V}$, $V_I = 0$					-10		
I_{off}	$V_{CC} = 0$, V_I or $V_O = 0$ to 4.5 V						± 100	
$I_{I(\text{hold})}$	$V_{CC} = 3\text{ V}$		A or B ports		$V_I = 0.8\text{ V}$		75	
					$V_I = 2\text{ V}$		-75	-75
I_{OZH}	$V_{CC} = 3.6\text{ V}$, $V_O = 3\text{ V}$				1		1	
I_{OZL}	$V_{CC} = 3.6\text{ V}$, $V_O = 0.5\text{ V}$				-1		-1	
I_{CC}	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}$ or GND, $I_O = 0$		Outputs high		0.13	0.5	0.13	0.19
			Outputs low		8.8	14	8.8	12
			Outputs disabled		0.13	0.5	0.13	0.19
ΔI_{CC}^\ddagger	$V_{CC} = 3\text{ V}$ to 3.6 V , One input at $V_{CC} - 0.6\text{ V}$, Other inputs at V_{CC} or GND				0.3		0.2	
C_i	$V_I = 3\text{ V}$ or 0				4.5		pF	
C_{io}	$V_O = 3\text{ V}$ or 0				11		pF	

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ Unused pins at V_{CC} or GND

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

SN54LVT646, SN74LVT646
3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS
WITH 3-STATE OUTPUTS

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

		SN54LVT646				SN74LVT646				UNIT
		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	0	150	0	150	0	150	0	150	MHz
t _w	Pulse duration, CLK high or low	3.3		3.3		3.3		3.3		ns
t _{su}	Setup time, A or B before CLKAB↑ or CLKBA↑	High	1.5		1.5		1.3		1.3	ns
		Low	2.5		3		2		2.4	
t _h	Hold time, A or B after CLKAB↑ or CLKBA↑	0.9		0.9		0.4		0.4		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT646				SN74LVT646				UNIT
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		
			MIN	MAX	MAX		MIN	TYP†	MAX	MAX	
f _{max}			150				150				MHz
t _{PLH}	CLKBA or CLKAB	A or B	1.2	5.9	6.9		1.8	3.8	5.7	6.7	ns
t _{PHL}			1.2	5.9	6.6		2.1	3.8	5.7	6.4	
t _{PLH}	A or B	B or A	0.8	4.9	5.6		1.3	2.8	4.7	5.4	ns
t _{PHL}			0.6	4.8	5.5		1	2.7	4.6	5.3	
t _{PLH}	SBA or SAB‡	A or B	1	6.4	7.4		1.4	3.7	6.2	7.2	ns
t _{PHL}			1	6.4	7		1.4	3.8	6.2	6.8	
t _{PZH}	OE	A or B	0.6	6	7.4		1	3	5.8	7.2	ns
t _{PZL}			0.6	6.2	7.5		1	3.2	6	7.3	
t _{PHZ}	OE	A or B	1.4	6.7	7.1		2.3	4.3	6.5	6.9	ns
t _{PLZ}			1.4	6.4	6.5		2.2	3.8	5.8	5.9	
t _{PZH}	DIR	A or B	0.6	6.7	7.7		1	3.4	6.5	7.5	ns
t _{PZL}			0.8	6.5	7.3		1.2	3.4	6.3	7.1	
t _{PHZ}	DIR	A or B	0.8	7.4	8.3		1.7	4.1	7.2	8.1	ns
t _{PLZ}			1	6.7	7		1.5	3.5	5.8	6.3	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

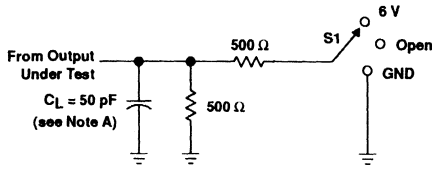
‡ These parameters are measured with the internal output state of the storage register opposite to that of the bus input.



SN54LVT646, SN74LVT646 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

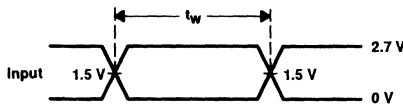
SCBS140A – MAY 1992 – REVISED AUGUST 1993

PARAMETER MEASUREMENT INFORMATION

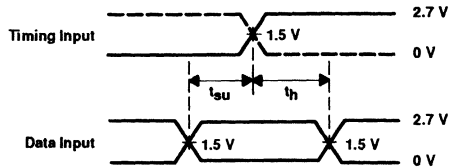


LOAD CIRCUIT FOR OUTPUTS

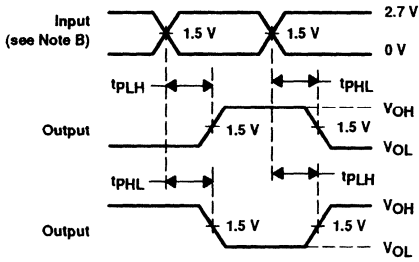
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



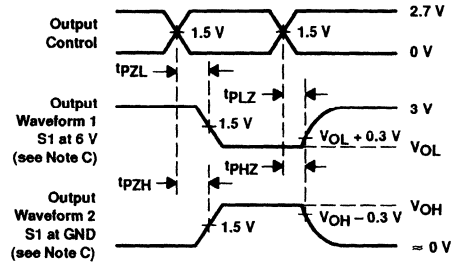
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms



SN54LVT652, SN74LVT652 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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- State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Package Options Include Plastic Small-Outline (SOIC), Shrink Small-Outline (SSOP), and Thin Shrink Small-Outline (TSSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs

description

These bus transceivers and registers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

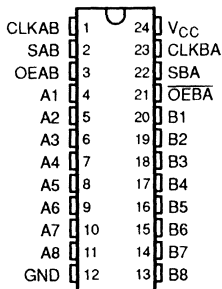
The 'LVT652 consists of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers.

Output-enable (OEAB and $\overline{\text{OEBA}}$) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input selects real-time data, and a high input selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'LVT652.

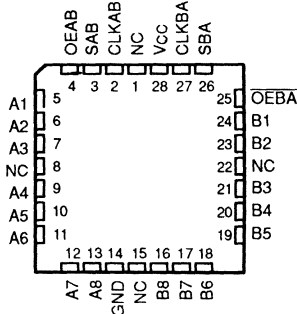
Data on the A or B data bus, or both, can be stored in the internal D-type flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the select- or enable-control pins. When SAB and SBA are in the real-time transfer mode, it is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. In this configuration each output reinforces its input. Therefore, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

SN54LVT652...JT PACKAGE
SN74LVT652...DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVT652...FK PACKAGE
(TOP VIEW)



NC - No internal connection

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SN54LVT652, SN74LVT652

3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS

WITH 3-STATE OUTPUTS

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description (continued)

The SN74LVT652 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT652 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVT652 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
L	H	L	L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	L	X	X	Input	Unspecified‡	Store A, hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers
L	X	L	↑	X	X	Unspecified‡	Input	Hold A, store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	L	X	H	X	Input	Output	Stored A data to B bus
H	L	L	L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

† The data output functions may be enabled or disabled by a variety of level combinations at the OEAB or OEBA inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition on the clock inputs.

‡ Select control = L; clocks can occur simultaneously.

Select control = H; clocks must be staggered in order to load both registers.

SN54LVT652, SN74LVT652 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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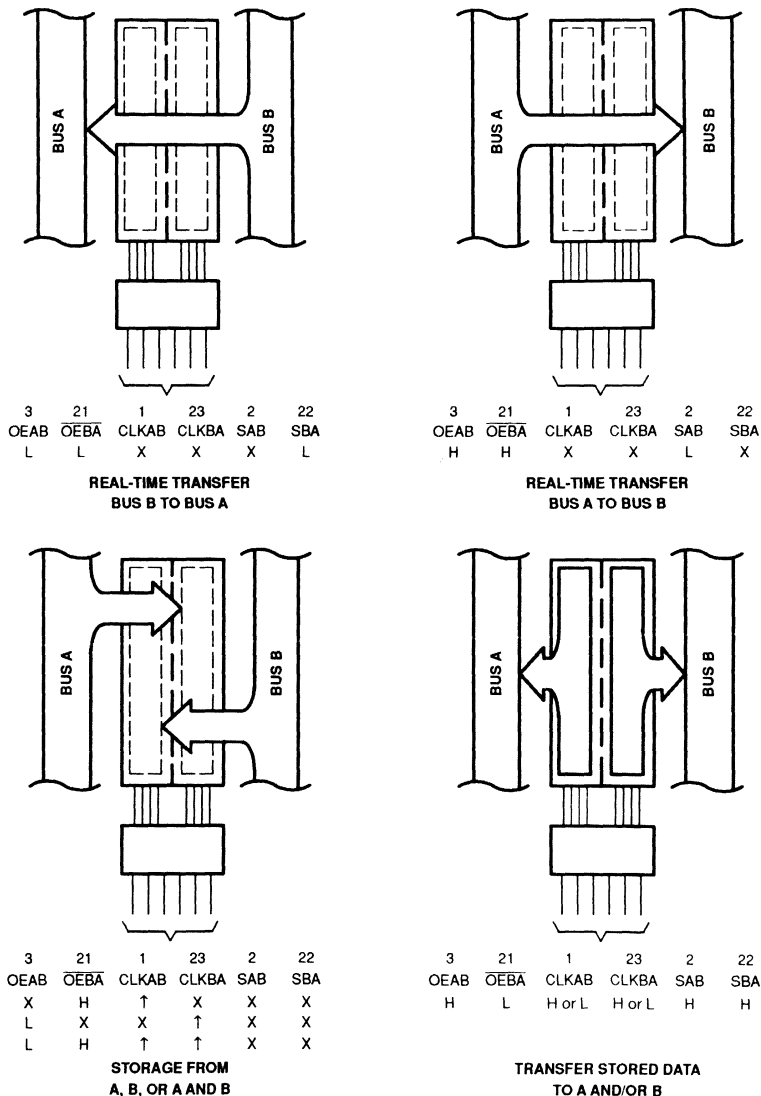


Figure 1. Bus-Management Functions

Pin numbers shown are for the DB, DW, JT, and PW packages.

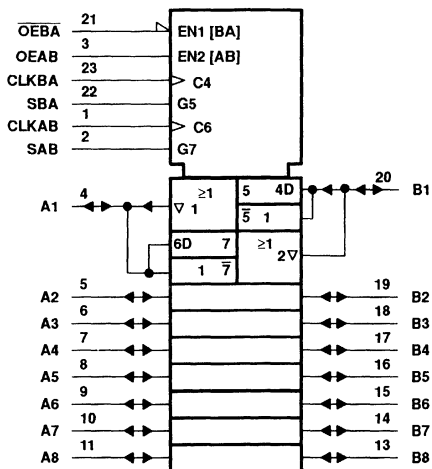
SN54LVT652, SN74LVT652

3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS

WITH 3-STATE OUTPUTS

SCBS141B - MAY 1992 - REVISED MARCH 1993

logic symbol†

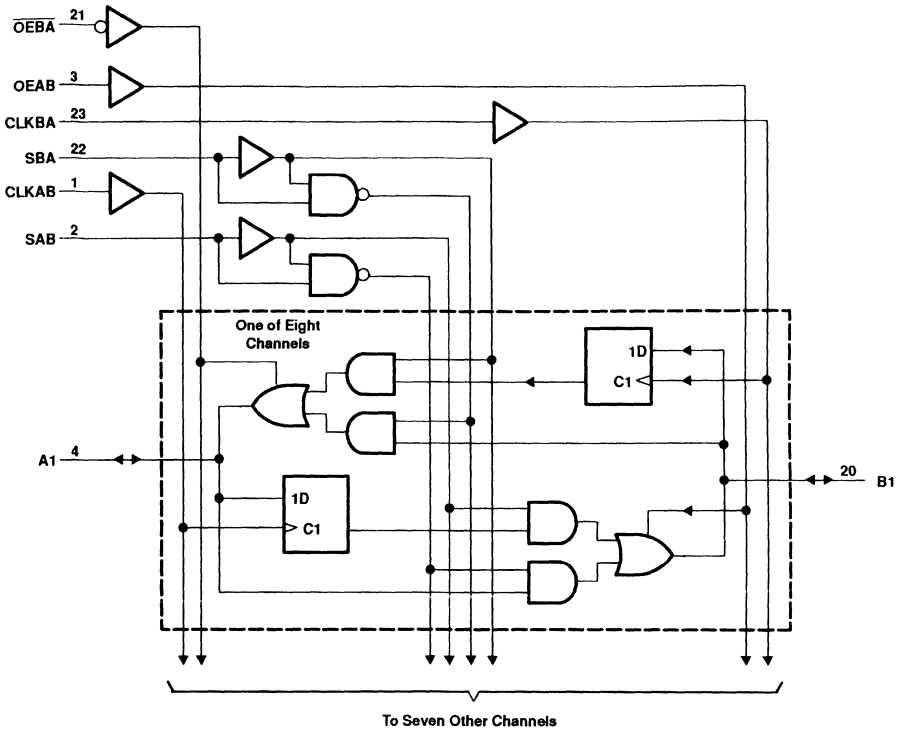


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DB, DW, JT, and PW packages.

SN54LVT652, SN74LVT652
3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS
WITH 3-STATE OUTPUTS

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logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, and PW packages.

SN54LVT652, SN74LVT652

3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1)	-0.5 V to 7 V
Current into any output in the low state, I_{OL} : SN54LVT652	96 mA
SN74LVT652	128 mA
Current into any output in the high state, I_{OH} (see Note 2): SN54LVT652	48 mA
SN74LVT652	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DB package	0.7 W
DW package	1 W
PW package	0.65 W
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions

	SN54LVT652		SN74LVT652		UNIT
	MIN	MAX	MIN	MAX	
V_{CC} Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH} High-level input voltage	2		2		V
V_{IL} Low-level input voltage		0.8		0.8	V
V_I Input voltage		5.5		5.5	V
I_{OH} High-level output current		-24		-32	mA
I_{OL} Low-level output current		24		32	mA
I_{OL}^\ddagger Low-level output current		48		64	mA
$\Delta t/\Delta v$ Input transition rise or fall rate	Outputs enabled		10	10	ns/V
T_A Operating free-air temperature	-55	125	-40	85	°C

‡ Current duty cycle $\leq 50\%$, $f \geq 1$ kHz

SN54LVT652, SN74LVT652 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54LVT652		SN74LVT652		UNIT
			MIN	TYP†	MAX	MIN	
V_{IK}	$V_{CC} = 2.7\text{ V}$, $I_I = -18\text{ mA}$				-1.2	-1.2	V
V_{OH}	$V_{CC} = \text{MIN to MAX}^\ddagger$, $I_{OH} = -100\ \mu\text{A}$		$V_{CC}-0.2$		$V_{CC}-0.2$		V
	$V_{CC} = 2.7\text{ V}$, $I_{OH} = -8\text{ mA}$		2.4		2.4		
	$V_{CC} = 3\text{ V}$, $I_{OH} = -24\text{ mA}$		2				
	$V_{CC} = 3\text{ V}$, $I_{OH} = -32\text{ mA}$				2		
V_{OL}	$V_{CC} = 2.7\text{ V}$, $I_{OL} = 100\ \mu\text{A}$				0.2	0.2	V
	$V_{CC} = 2.7\text{ V}$, $I_{OL} = 24\text{ mA}$				0.5	0.5	
	$V_{CC} = 3\text{ V}$, $I_{OL} = 16\text{ mA}$				0.4	0.4	
	$V_{CC} = 3\text{ V}$, $I_{OL} = 32\text{ mA}$				0.5	0.5	
	$V_{CC} = 3\text{ V}$, $I_{OL} = 48\text{ mA}$				0.55		
	$V_{CC} = 3\text{ V}$, $I_{OL} = 64\text{ mA}$					0.55	
I_I	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}$ or GND		Control pins			± 1	± 1
	$V_{CC} = 0$ or MAX^\ddagger , $V_I = 5.5\text{ V}$					10	10
	$V_{CC} = 3.6\text{ V}$, $V_I = 5.5\text{ V}$		A or B ports§			20	20
	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}$					5	5
	$V_{CC} = 3.6\text{ V}$, $V_I = 0$					-10	-10
I_{off}	$V_{CC} = 0$, V_I or $V_O = 0$ to 4.5 V					± 100	μA
$I_{I(\text{hold})}$	$V_{CC} = 3\text{ V}$	$V_I = 0.8\text{ V}$	A or B ports			75	75
		$V_I = 2\text{ V}$				-75	-75
I_{OZH}	$V_{CC} = 3.6\text{ V}$	$V_O = 3\text{ V}$			1	1	μA
I_{OZL}	$V_{CC} = 3.6\text{ V}$	$V_O = 0.5\text{ V}$			-1	-1	μA
I_{CC}	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}$ or GND	$I_O = 0$	Outputs high	0.13	0.19	0.13	0.19
			Outputs low	8.8	12	8.8	12
			Outputs disabled	0.13	0.19	0.13	0.19
ΔI_{CC}^\ddagger	$V_{CC} = 3\text{ V}$ to 3.6 V , One input at $V_{CC} - 0.6\text{ V}$, Other inputs at V_{CC} or GND				0.2	0.2	mA
C_i	$V_I = 3\text{ V}$ or 0				4.5	4.5	pF
C_{IO}	$V_O = 3\text{ V}$ or 0				11	11	pF

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ Unused pins at V_{CC} or GND

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



SN54LVT652, SN74LVT652

3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCBS141B – MAY 1992 – REVISED MARCH 1993

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

		SN54LVT652				SN74LVT652				UNIT
		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	0	150	0	150	0	150	0	150	MHz
t _w	Pulse duration, CLK high or low					3.3		3.3		ns
t _{su}	Setup time, A or B before CLKABT or CLKBA†	Data high				1.2		1.2		ns
		Data low				2		2.5		
t _h	Hold time, A or B after CLKABT or CLKBA†					0.5		0.5		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT652				SN74LVT652				UNIT
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN	
f _{max}							150		150		MHz
t _{PLH}	CLKBA or CLKAB	A or B					1.8	3.7	6	6.9	ns
t _{PHL}							2	3.7	5.7	6.4	
t _{PLH}	A or B	B or A					1.2	2.8	4.7	5.5	ns
t _{PHL}							1	2.6	4.6	5.3	
t _{PLH}	SBA or SAB†	A or B					1.4	3.7	6.4	7.6	ns
t _{PHL}							1.4	4	6.2	6.8	
t _{PZH}	OEBA	A					1	2.9	5.8	7.2	ns
t _{PZL}							1	3	6	7.3	
t _{PHZ}	OEBA	A					2.2	3.9	6.5	6.9	ns
t _{PLZ}							1.8	3.2	5.8	5.9	
t _{PZH}	OEAB	B					1	3.3	6.5	7.5	ns
t _{PZL}							1.2	3.4	6.3	7.1	
t _{PHZ}	OEAB	B					1.7	4.5	7.2	8.1	ns
t _{PLZ}							1.5	3.8	5.8	6.3	

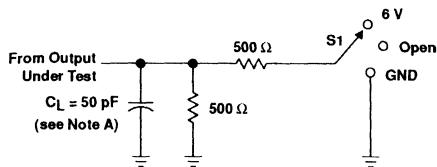
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

‡ These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

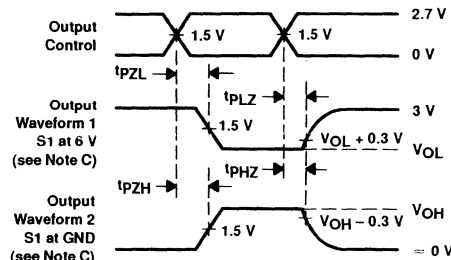
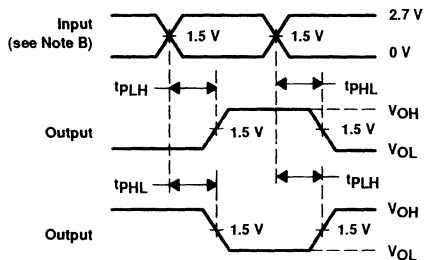
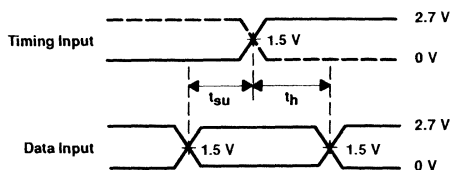
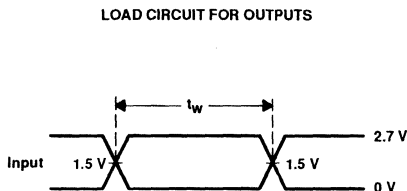
SN54LVT652, SN74LVT652 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCBS141B - MAY 1992 - REVISED MARCH 1993

PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

SN54LVT2952, SN74LVT2952 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCBS152B - MAY 1992 - REVISED SEPTEMBER 1993

- **State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Package Options Include Plastic Small-Outline (SOIC), Shrink Small-Outline (SSOP), and Thin Shrink Small-Outline (TSSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

description

These octal bus transceivers and registers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

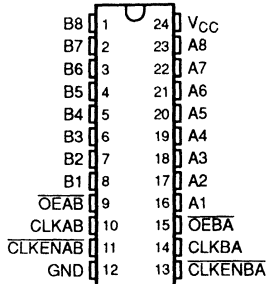
The 'LVT2952 consists of two 8-bit back-to-back registers that store data flowing in both directions between two bidirectional buses. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock (CLKAB or CLKBA) input provided that the clock-enable ($\overline{\text{CLKENAB}}$ or $\overline{\text{CLKENBA}}$) input is low. Taking the output-enable ($\overline{\text{OEAB}}$ or $\overline{\text{OEBA}}$) input low accesses the data on either port.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

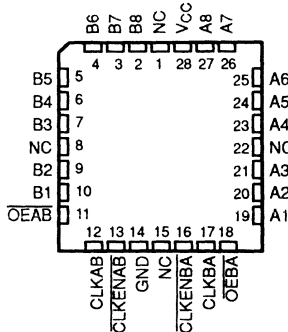
The SN74LVT2952 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT2952 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVT2952 is characterized for operation from -40°C to 85°C .

SN54LVT2952 . . . JT PACKAGE
SN74LVT2952 . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVT2952 . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

SN54LVT2952, SN74LVT2952
3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS
WITH 3-STATE OUTPUTS

SCBS152B – MAY 1992 – REVISED SEPTEMBER 1993

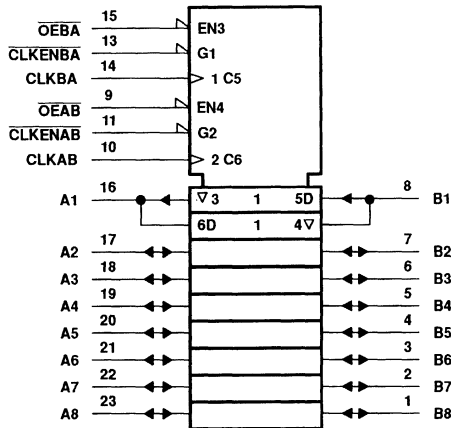
FUNCTION TABLE†

INPUTS				OUTPUT
CLKENAB	CLKAB	OEAB	A	B
H	X	L	X	B ₀ ‡
X	H or L	L	X	B ₀ ‡
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	Z

† A-to-B data flow is shown; B-to-A data flow is similar but uses CLKENBA, CLKBA, and OEBA.

‡ Level of B before the indicated steady-state input conditions were established.

logic symbols§

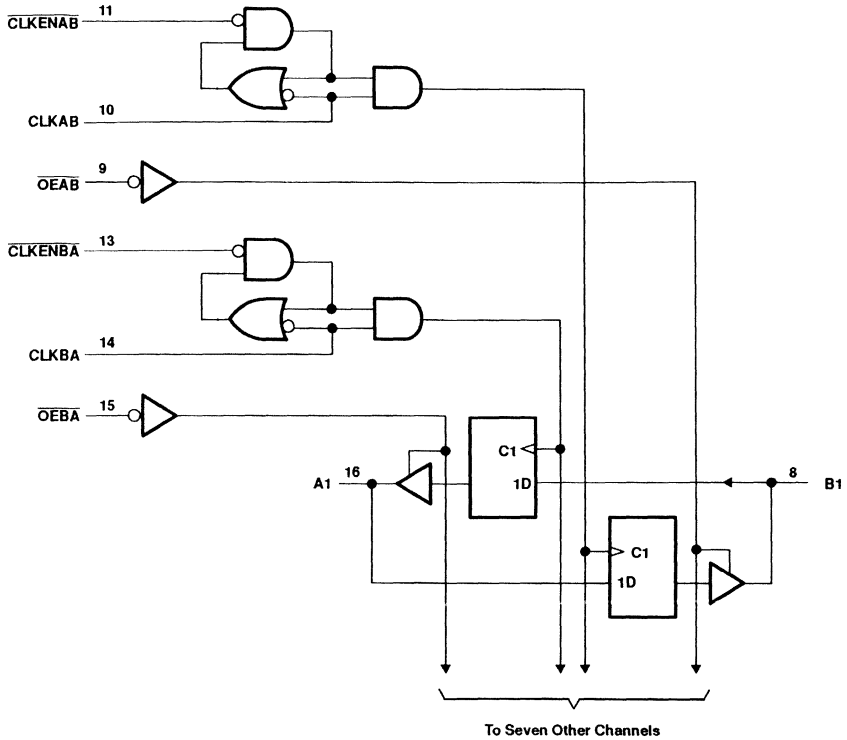


§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DB, DW, JT, and PW packages.

SN54LVT2952, SN74LVT2952
3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS
WITH 3-STATE OUTPUTS

SCBS152B - MAY 1992 - REVISED SEPTEMBER 1993

logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, and PW packages.

SN54LVT2952, SN74LVT2952

3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCBS152B – MAY 1992 – REVISED SEPTEMBER 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1)	-0.5 V to 7 V
Current into any output in the low state, I_O : SN54LVT2952	96 mA
SN74LVT2952	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT2952	48 mA
SN74LVT2952	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DB package	0.7 W
DW package	1 W
PW package	0.65 W
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions

	SN54LVT2952		SN74LVT2952		UNIT
	MIN	MAX	MIN	MAX	
V_{CC} Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH} High-level input voltage	2		2		V
V_{IL} Low-level input voltage		0.8		0.8	V
V_I Input voltage		5.5		5.5	V
I_{OH} High-level output current		-24		-32	mA
I_{OL} Low-level output current		24		32	mA
I_{OL}^\ddagger Low-level output current		48		64	mA
$\Delta t/\Delta v$ Input transition rise or fall rate	Outputs enabled		10	10	ns/V
T_A Operating free-air temperature	-55	125	-40	85	°C

‡ Current duty cycle $\leq 50\%$, $f \geq 1$ kHz

SN54LVT2952, SN74LVT2952 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54LVT2952		SN74LVT2952		UNIT
			MIN	TYP†	MAX	MIN	
V _{IK}	V _{CC} = 2.7 V, I _I = -18 mA				-1.2		V
V _{OH}	V _{CC} = MIN to MAX‡, I _{OH} = -100 µA		V _{CC} - 0.2		V _{CC} - 0.2		V
	V _{CC} = 2.7 V, I _{OH} = -8 mA		2.4		2.4		
	V _{CC} = 3 V, I _{OH} = -24 mA		2				
	V _{CC} = 3 V, I _{OH} = -32 mA				2		
V _{OL}	V _{CC} = 2.7 V, I _{OL} = 100 µA				0.2		V
	V _{CC} = 2.7 V, I _{OL} = 24 mA				0.5		
	V _{CC} = 3 V, I _{OL} = 16 mA				0.4		
	V _{CC} = 3 V, I _{OL} = 32 mA				0.5		
	V _{CC} = 3 V, I _{OL} = 48 mA				0.55		
	V _{CC} = 3 V, I _{OL} = 64 mA				0.55		
I _I	V _{CC} = 3.6 V, V _I = V _{CC} or GND		Control pins		±1		µA
	V _{CC} = 0 or MAX‡, V _I = 5.5 V				10		
	V _{CC} = 3.6 V, V _I = 5.5 V		A or B ports§		20		
	V _{CC} = 3.6 V, V _I = V _{CC}				5		
	V _{CC} = 3.6 V, V _I = 0				-10		
I _{off}	V _{CC} = 0, V _I or V _O = 0 to 4.5 V				±100		µA
I _I (hold)	V _{CC} = 3 V		A or B ports		75		µA
	V _I = 0.8 V				-75		
	V _I = 2 V				-75		
I _{OZH}	V _{CC} = 3.6 V, V _O = 3 V				1		µA
I _{OZL}	V _{CC} = 3.6 V, V _O = 0.5 V				-1		µA
I _{CC}	V _{CC} = 3.6 V, V _I = V _{CC} or GND		I _O = 0,				mA
			Outputs high		0.13 0.19		
			Outputs low		8.8 12		
			Outputs disabled		0.13 0.19		
ΔI _{CC} ¶	V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND				0.2		mA
C _t	V _I = 3 V or 0				4.5		pF
C _{io}	V _O = 3 V or 0				11.5		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ Unused pins at V_{CC} or GND

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



SN54LVT2952, SN74LVT2952
3.3-V ABT OCTAL BUS TRANSCIEVERS AND REGISTERS
WITH 3-STATE OUTPUTS

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timing requirement over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			SN54LVT2952				SN74LVT2952				UNIT
			$V_{CC} = 3.3 V \pm 0.3 V$		$V_{CC} = 2.7 V$		$V_{CC} = 3.3 V \pm 0.3 V$		$V_{CC} = 2.7 V$		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency						150				MHz
t_w	Pulse duration		CLK high				3.3		3.3		ns
			CLK low				3.3		3.3		
t_{su}	A or B	High	2.6		2.9		2.5		2.8		ns
		Low	2.6		3.1		2.5		3		
	\overline{CE}	High	0.9		0.8		0.9		0.8		
		Low	2.5		2.7		2.4		2.7		
t_h	A or B		1.5		0.7		1.5		0.7		ns
	\overline{CE}		2.6		2.6		2.5		2.6		

switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

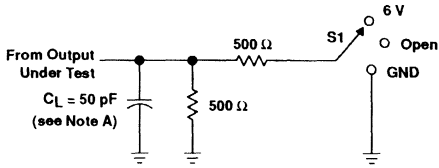
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT2952				SN74LVT2952				UNIT	
			$V_{CC} = 3.3 V \pm 0.3 V$		$V_{CC} = 2.7 V$		$V_{CC} = 3.3 V \pm 0.3 V$		$V_{CC} = 2.7 V$			
			MIN	TYP†	MAX	MIN	MAX	MIN	TYP†	MAX		MIN
f_{max}							150				MHz	
t_{PLH}	CLKBA or CLKAB	A or B	1.3	6.4	2.7	7.4	1.3	3.6	6.1	2.7	7.1	ns
t_{PHL}			1.8	6.1	2.7	7	1.8	3.7	6	2.7	6.9	
t_{PZH}	\overline{OEBA} or \overline{OEAB}	A or B	1	6.3	2.6	7.3	1	3.2	5.6	2.6	6.7	ns
t_{PZL}			1.1	6.6	2.9	8.2	1.2	3.2	6.5	2.9	8	
t_{PHZ}	\overline{OEBA} or \overline{OEAB}	A or B	1	7	2.7	7.6	1	4.1	6.3	2.7	6.9	ns
t_{PLZ}			1.6	5.8	1.7	6	1.6	3.3	5.1	1.8	5.3	

† All typical values are at $V_{CC} = 3.3 V$, $T_A = 25^\circ C$.

SN54LVT2952, SN74LVT2952 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

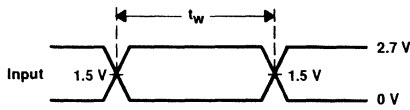
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PARAMETER MEASUREMENT INFORMATION

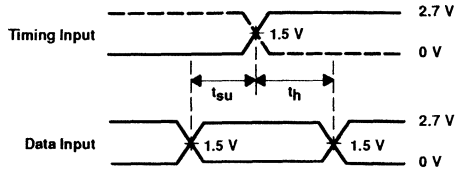


LOAD CIRCUIT FOR OUTPUTS

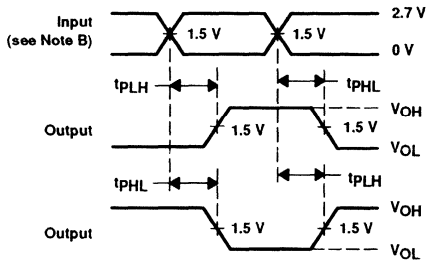
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



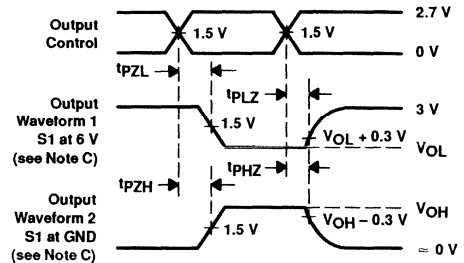
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one transition per measurement.

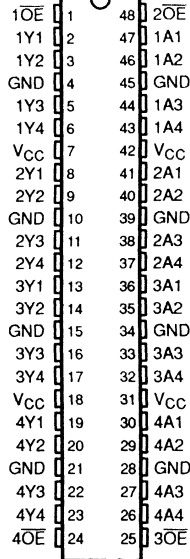
Figure 1. Load Circuit and Voltage Waveforms

SN54LVT16244A, SN74LVT16244A
3.3-V ABT 16-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

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- State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Member of the Texas Instruments *Widebus™* Family
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings

SN54LVT16244A . . . WD PACKAGE
 SN74LVT16244A . . . DGG OR DL PACKAGE
 (TOP VIEW)



description

The LVT16244A is a 16-bit buffer and line driver designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides true outputs and symmetrical \overline{OE} (active-low output-enable) inputs.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVT16244A is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT16244A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVT16244A is characterized for operation from -40°C to 85°C .

Widebus is a trademark of Texas Instruments Incorporated.

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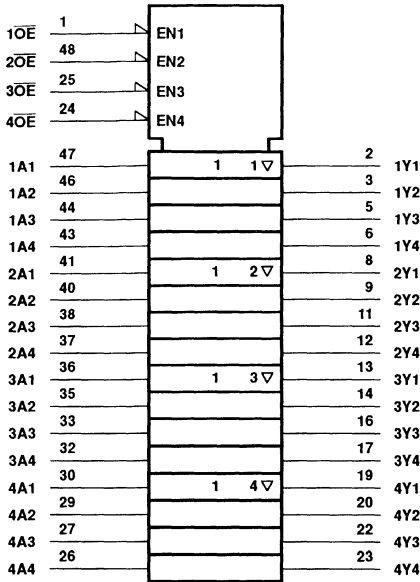


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SN54LVT16244A, SN74LVT16244A
3.3-V ABT 16-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

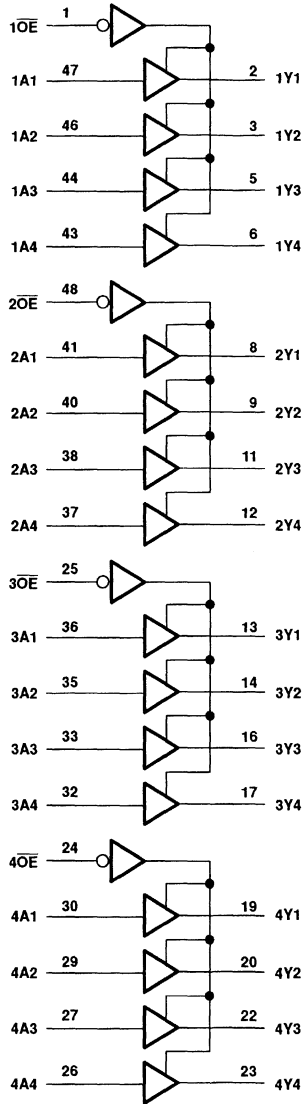
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN54LVT16244A, SN74LVT16244A
3.3-V ABT 16-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

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FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
\overline{OE}	A	Y
L	H	H
L	L	L
H	X	Z

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1)	-0.5 V to 7 V
Current into any output in the low state, I_O : SN54LVT16244A	96 mA
SN74LVT16244A	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT16244A	48 mA
SN74LVT16244A	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DGG package	0.8 W
DL package	0.85 W
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions

		SN54LVT16244A		SN74LVT16244A		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current		-24		-32	mA
I_{OL}	Low-level output current		24		32	mA
I_{OL}^\ddagger	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
T_A	Operating free-air temperature	-55	125	-40	85	°C

‡ Current duty cycle $\leq 50\%$, $f \geq 1$ kHz

SN54LVT16244A, SN74LVT16244A

3.3-V ABT 16-BIT BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

SCBS142A – MAY 1992 – REVISED SEPTEMBER 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54LVT16244A		SN74LVT16244A		UNIT	
			MIN	MAX	MIN	TYP†		MAX
V_{IK}	$V_{CC} = 2.7\text{ V}$, $I_I = -18\text{ mA}$		-1.2		-1.2		V	
V_{OH}	$V_{CC} = \text{MIN to MAX}^\ddagger$, $I_{OH} = -100\ \mu\text{A}$		$V_{CC} - 0.2$		$V_{CC} - 0.2$		V	
	$V_{CC} = 2.7\text{ V}$, $I_{OH} = -8\text{ mA}$		2.4		2.4			
	$V_{CC} = 3\text{ V}$, $I_{OH} = -24\text{ mA}$		2					
	$V_{CC} = 3\text{ V}$, $I_{OH} = -32\text{ mA}$				2			
V_{OL}	$V_{CC} = 2.7\text{ V}$, $I_{OL} = 100\ \mu\text{A}$		0.2		0.2		V	
	$V_{CC} = 2.7\text{ V}$, $I_{OL} = 24\text{ mA}$		0.5		0.5			
	$V_{CC} = 3\text{ V}$, $I_{OL} = 16\text{ mA}$		0.4		0.4			
	$V_{CC} = 3\text{ V}$, $I_{OL} = 32\text{ mA}$		0.5		0.5			
	$V_{CC} = 3\text{ V}$, $I_{OL} = 48\text{ mA}$		0.55		0.55			
	$V_{CC} = 3\text{ V}$, $I_{OL} = 64\text{ mA}$				0.55			
I_I	$V_{CC} = 0\text{ or MAX}^\ddagger$, $V_I = 5.5\text{ V}$		10		10		μA	
	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}\text{ or GND}$		Control pins		± 1			
	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}$		Data pins		1			
	$V_{CC} = 3.6\text{ V}$, $V_I = 0$				-5			
I_{off}	$V_{CC} = 0$, $V_I\text{ or }V_O = 0\text{ to }4.5\text{ V}$				± 100		μA	
$I_I(\text{hold})$	$V_{CC} = 3\text{ V}$	$V_I = 0.8\text{ V}$	A inputs		75		μA	
		$V_I = 2\text{ V}$			-75			
I_{OZH}	$V_{CC} = 3.6\text{ V}$, $V_O = 3\text{ V}$		5		5		μA	
I_{OZL}	$V_{CC} = 3.6\text{ V}$, $V_O = 0.5\text{ V}$		-5		-5		μA	
I_{CC}	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}\text{ or GND}$	$I_O = 0$,	Outputs high	0.09		0.09		mA
			Outputs low	5		5		
			Outputs disabled	0.09		0.09		
ΔI_{CC}^\S	$V_{CC} = 3\text{ V to }3.6\text{ V}$, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at $V_{CC}\text{ or GND}$		0.2		0.2		mA	
C_i	$V_I = 3\text{ V or }0$				4		pF	
C_o	$V_O = 3\text{ V or }0$				10		pF	

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}\text{ or GND}$.

switching characteristics over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT16244A				SN74LVT16244A				UNIT
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN	
t_{PLH}	A	Y	1	4.2	5.1	1	2.3	4.1	5		ns
t_{PHL}			1	4.2	5.3	1	2.3	4.1	5.2		
t_{PZH}	\overline{OE}	Y	1	5.3	6.4	1	2.6	5.2	6.3		ns
t_{PZL}			1	5.3	6.8	1	2.6	5.2	6.7		
t_{PHZ}	\overline{OE}	Y	2.1	5.9	6.4	2.2	3.9	5.7	6.3		ns
t_{PLZ}			1.9	5.3	5.7	2	3.7	5.1	5.6		

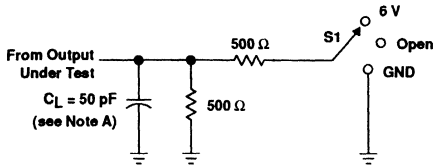
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SN54LVT16244A, SN74LVT16244A
3.3-V ABT 16-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

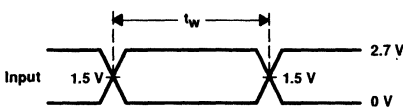
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PARAMETER MEASUREMENT INFORMATION

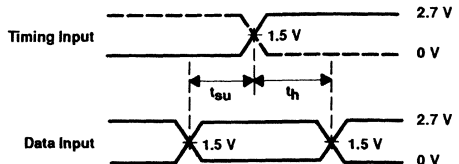


LOAD CIRCUIT FOR OUTPUTS

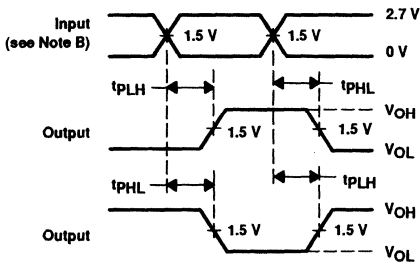
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



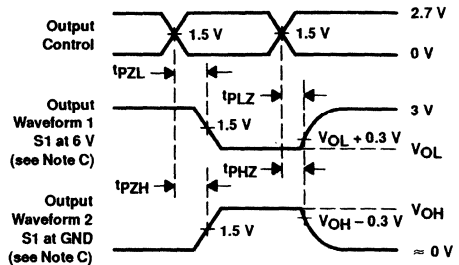
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

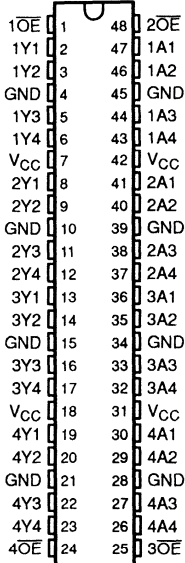
Figure 1. Load Circuit and Voltage Waveforms

SN54LVT162244, SN74LVT162244
3.3-V ABT 16-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

JUNE 1993

- Output Ports Have Equivalent 22- Ω Series Resistors, So No External Resistors Are Required
- State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Member of the Texas Instruments *Widebus*[™] Family
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings

SN54LVT162244 . . . WD PACKAGE
 SN74LVT162244 . . . DGG OR DL PACKAGE
 (TOP VIEW)



description

The 1LVT162244 is a 16-bit buffer and line driver designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides true outputs and symmetrical \overline{OE} (active-low output-enable) inputs.

The outputs, which are designed to source or sink up to 12 mA, include 22- Ω series resistors to reduce overshoot and undershoot.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVT162244 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT162244 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVT162244 is characterized for operation from -40°C to 85°C .

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PRODUCT PREVIEW

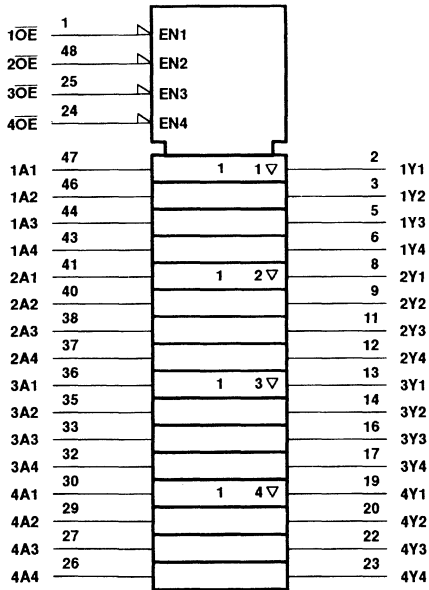
SN54LVT162244, SN74LVT162244
3.3-V ABT 16-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

JUNE 1993

FUNCTION TABLE
(each buffer)

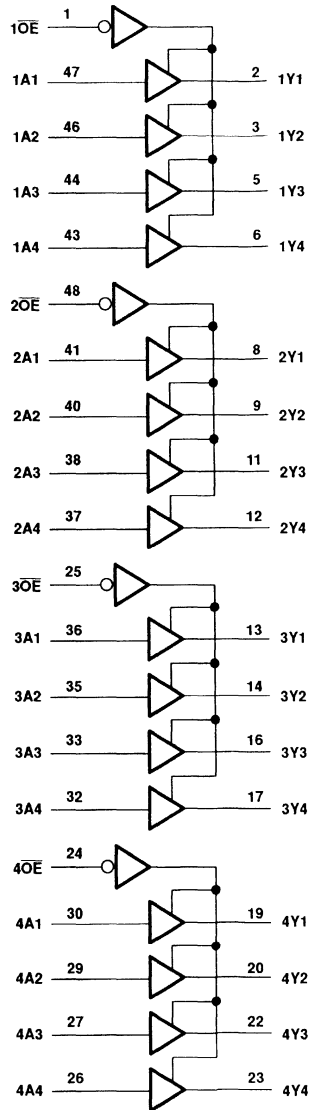
INPUTS		OUTPUT
\overline{OE}	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

SN54LVT162244, SN74LVT162244
3.3-V ABT 16-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

JUNE 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1)	-0.5 V to 7 V
Current into any output in the low state, I_{OL}	30 mA
Current into any output in the high state, I_{OH} (see Note 2)	30 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DGG package	0.8 W
DL package	0.85 W
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions

		SN54LVT162244		SN74LVT162244		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current		-12		-12	mA
I_{OL}	Low-level output current		12		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
T_A	Operating free-air temperature	-55	125	-40	85	°C

PRODUCT PREVIEW

SN54LVT162244, SN74LVT162244
3.3-V ABT 16-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

JUNE 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54LVT162244		SN74LVT162244		UNIT	
			MIN	MAX	MIN	MAX		
V_{IK}	$V_{CC} = 2.7 \text{ V}$, $I_I = -18 \text{ mA}$		-1.2		-1.2		V	
V_{OH}	$V_{CC} = 3 \text{ V}$, $I_{OH} = -12 \text{ mA}$		2		2		V	
V_{OL}	$V_{CC} = 3 \text{ V}$, $I_{OL} = 12 \text{ mA}$		0.8		0.8		V	
I_I	$V_{CC} = 0 \text{ or MAX}^\ddagger$, $V_I = 5.5 \text{ V}$		10		10		μA	
	$V_{CC} = 3.6 \text{ V}$, $V_I = V_{CC} \text{ or GND}$	Control pins	± 1		± 1			
	$V_{CC} = 3.6 \text{ V}$, $V_I = V_{CC}$	Data pins	1		1			
	$V_{CC} = 3.6 \text{ V}$, $V_I = 0$		-5		-5			
I_{off}	$V_{CC} = 0$, $V_I \text{ or } V_O = 0 \text{ to } 4.5 \text{ V}$				± 100		μA	
$I_I(\text{hold})$	$V_{CC} = 3 \text{ V}$	$V_I = 0.8 \text{ V}$	75		75		μA	
		$V_I = 2 \text{ V}$	-75		-75			
I_{OZH}	$V_{CC} = 3.6 \text{ V}$, $V_O = 3 \text{ V}$	5		5		μA		
I_{OZL}	$V_{CC} = 3.6 \text{ V}$, $V_O = 0.5 \text{ V}$	-5		-5		μA		
I_{CC}	$V_{CC} = 3.6 \text{ V}$, $V_I = V_{CC} \text{ or GND}$	$I_O = 0$	Outputs high	0.19		0.1		mA
			Outputs low	5		5		
			Outputs disabled	0.19		0.1		
ΔI_{CC}^\S	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$, One input at $V_{CC} - 0.6 \text{ V}$, Other inputs at $V_{CC} \text{ or GND}$		0.2		0.2		mA	
C_i	$V_I = 3 \text{ V or } 0$						pF	
C_o	$V_O = 3 \text{ V or } 0$						pF	

† All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

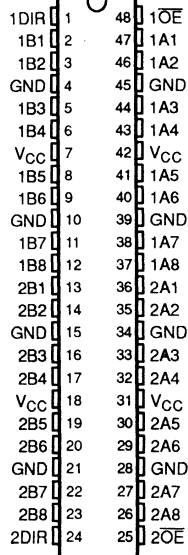
PRODUCT PREVIEW

SN54LVT16245, SN74LVT16245 3.3-V ABT 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS143A – MAY 1992 – REVISED MARCH 1993

- State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Member of the Texas Instruments *Widebus™* Family
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings

SN54LVT16245 . . . WD PACKAGE
SN74LVT16245 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The LVT16245 is a 16-bit (dual-octal) noninverting 3-state transceiver designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so that the buses are effectively isolated.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVT16245 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT16245 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVT16245 is characterized for operation from -40°C to 85°C .

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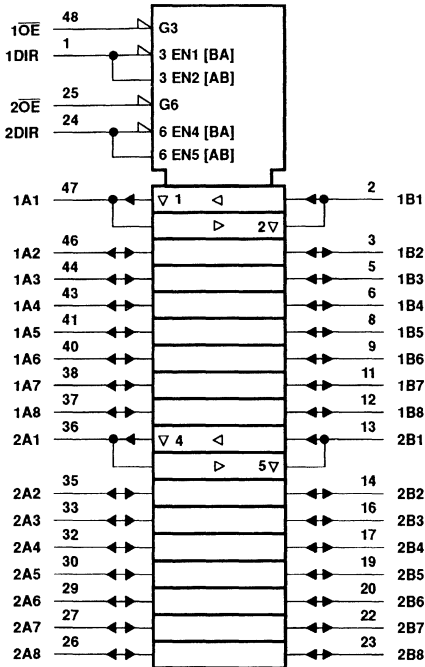
SN54LVT16245, SN74LVT16245
3.3-V ABT 16-BIT BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

SCBS143A – MAY 1992 – REVISED MARCH 1993

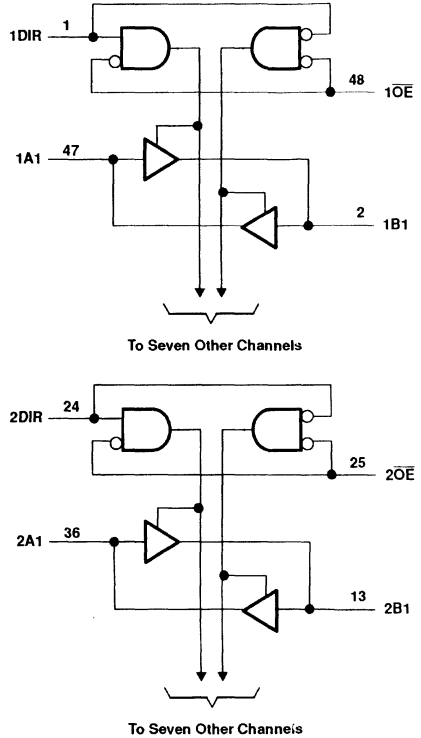
FUNCTION TABLE
 (each 8-bit section)

INPUTS		OPERATION
OE	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic symbol



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN54LVT16245, SN74LVT16245 3.3-V ABT 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS143A – MAY 1992 – REVISED MARCH 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Current into any output in the low state, I_O : SN54LVT16245	96 mA
SN74LVT16245	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT16245	48 mA
SN74LVT16245	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DGG package	0.8 W
DL package	0.85 W
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions

		SN54LVT16245		SN74LVT16245		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		24		32	mA
I_{OL}^\ddagger	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

‡ Current duty cycle $\leq 50\%$, $f \geq 1$ kHz

SN54LVT16245, SN74LVT16245

3.3-V ABT 16-BIT BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

SCBS143A - MAY 1992 - REVISED MARCH 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54LVT16245		SN74LVT16245		UNIT
			MIN	TYP†	MAX	MIN	
V_{IK}	$V_{CC} = 2.7 \text{ V}$, $I_I = -18 \text{ mA}$			-1.2		-1.2	V
V_{OH}	$V_{CC} = \text{MIN to MAX}^\ddagger$, $I_{OH} = -100 \mu\text{A}$		$V_{CC} - 0.2$		$V_{CC} - 0.2$		V
	$V_{CC} = 2.7 \text{ V}$, $I_{OH} = -8 \text{ mA}$		2.4		2.4		
	$V_{CC} = 3 \text{ V}$, $I_{OH} = -24 \text{ mA}$		2				
	$V_{CC} = 3 \text{ V}$, $I_{OH} = -32 \text{ mA}$				2		
V_{OL}	$V_{CC} = 2.7 \text{ V}$, $I_{OL} = 100 \mu\text{A}$			0.2		0.2	V
	$V_{CC} = 2.7 \text{ V}$, $I_{OL} = 24 \text{ mA}$			0.5		0.5	
	$V_{CC} = 3 \text{ V}$, $I_{OL} = 16 \text{ mA}$			0.4		0.4	
	$V_{CC} = 3 \text{ V}$, $I_{OL} = 32 \text{ mA}$			0.5		0.5	
	$V_{CC} = 3 \text{ V}$, $I_{OL} = 48 \text{ mA}$			0.55			
	$V_{CC} = 3 \text{ V}$, $I_{OL} = 64 \text{ mA}$					0.55	
I_I	$V_{CC} = 3.6 \text{ V}$, $V_I = V_{CC} \text{ or GND}$		Control pins	± 1		± 1	μA
	$V_{CC} = 0 \text{ or MAX}^\ddagger$, $V_I = 5.5 \text{ V}$			10		10	
	$V_{CC} = 3.6 \text{ V}$, $V_I = 5.5 \text{ V}$		A or B ports§	20		20	
	$V_{CC} = 3.6 \text{ V}$, $V_I = V_{CC}$			1		1	
	$V_{CC} = 3.6 \text{ V}$, $V_I = 0$			-5		-5	
I_{off}	$V_{CC} = 0$, $V_I \text{ or } V_O = 0 \text{ to } 4.5 \text{ V}$					± 100	μA
$I_I(\text{hold})$	$V_{CC} = 3 \text{ V}$		A or B ports	75		75	μA
	$V_I = 0.8 \text{ V}$			-75		-75	
I_{OZH}	$V_{CC} = 3.6 \text{ V}$, $V_O = 3 \text{ V}$			1		1	μA
I_{OZL}	$V_{CC} = 3.6 \text{ V}$, $V_O = 0.5 \text{ V}$			-1		-1	μA
I_{CC}	$V_{CC} = 3.6 \text{ V}$, $I_O = 0$, $V_I = V_{CC} \text{ or GND}$		Outputs high	0.19		0.19	mA
			Outputs low	5		5	
			Outputs disabled	0.19		0.19	
ΔI_{CC}^\ddagger	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$, One input at $V_{CC} - 0.6 \text{ V}$, Other inputs at $V_{CC} \text{ or GND}$			0.2		0.2	mA
C_i	$V_I = 3 \text{ V or } 0$			4		4	pF
C_{io}	$V_O = 3 \text{ V or } 0$			11		11	pF

† All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ Unused pins at V_{CC} or GND

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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SN54LVT16245, SN74LVT16245
3.3-V ABT 16-BIT BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

SCBS143A – MAY 1992 – REVISED MARCH 1993

switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT16245				SN74LVT16245				UNIT
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	
t_{PLH}	A or B	B or A					1	2.4	4.1	5	ns
t_{PHL}							1	2.3	4.1	5.2	
t_{PZH}	\overline{OE}	A or B					1	3	5.3	6.3	ns
t_{PZL}							1	3.1	5.2	6.7	
t_{PHZ}	\overline{OE}	A or B					2.7	4.6	6.4	7.2	ns
t_{PLZ}							2.6	4.3	5.8	6.1	

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

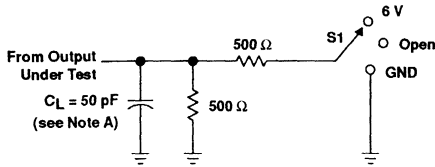
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SN54LVT16245, SN74LVT16245
3.3-V ABT 16-BIT BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

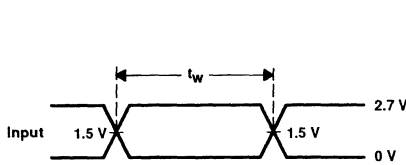
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PARAMETER MEASUREMENT INFORMATION

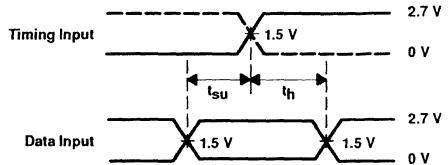


LOAD CIRCUIT FOR OUTPUTS

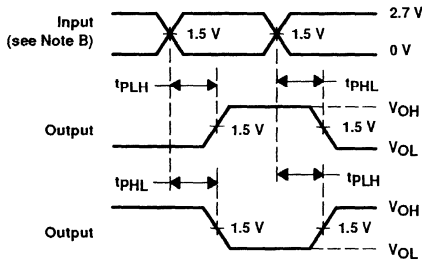
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



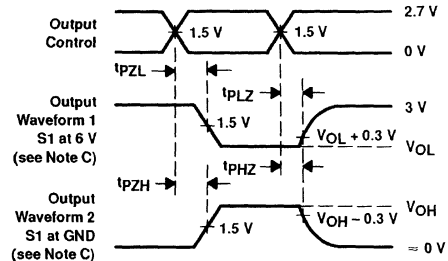
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one transition per measurement.

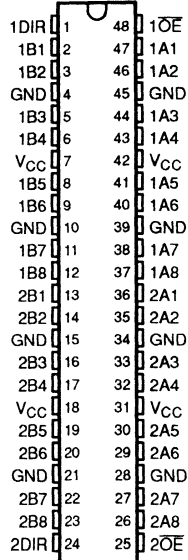
Figure 1. Load Circuit and Voltage Waveforms

SN74LVT162245, SN74LVT162245
3.3-V ABT 16-BIT BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

JUNE 1993

- **A-Port Outputs Have Equivalent 22- Ω Series Resistors, So No External Resistors Are Required**
- **State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **Member of the Texas Instruments Widebus™ Family**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54LVT162245 . . . WD PACKAGE
 SN74LVT162245 . . . DGG OR DL PACKAGE
 (TOP VIEW)



PRODUCT PREVIEW

description

The 'LVT162245 is a 16-bit (dual-octal) noninverting 3-state transceiver designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so that the buses are effectively isolated.

The A-port outputs, which are designed to source or sink up to 12 mA, include 22- Ω series resistors to reduce overshoot and undershoot.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVT162245 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

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SNLVT162245, SN74LVT162245
3.3-V ABT 16-BIT BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS
 JUNE 1993

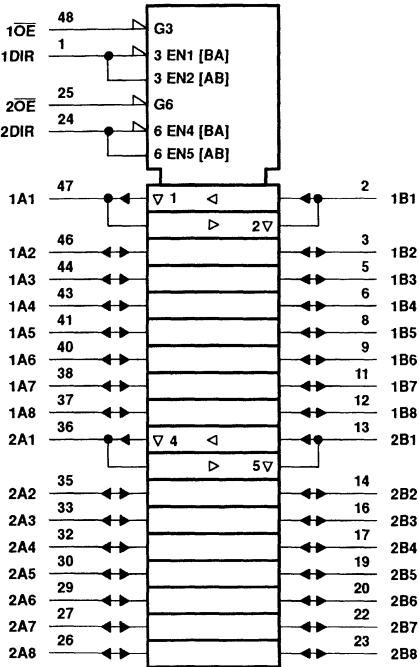
description (continued)

The SN54LVT162245 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVT162245 is characterized for operation from -40°C to 85°C .

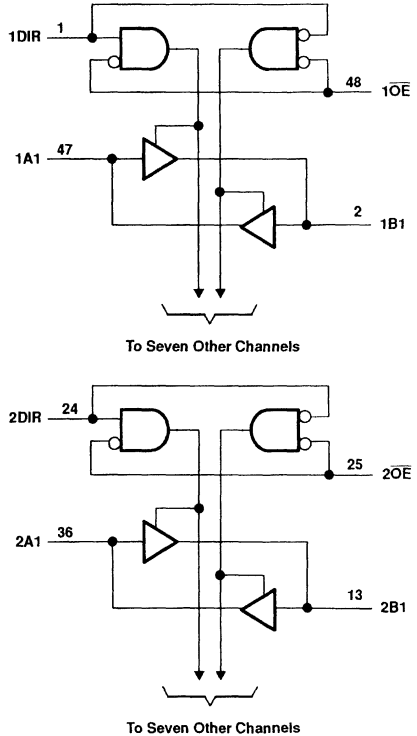
FUNCTION TABLE
 (each 8-bit section)

INPUTS		OPERATION
$\overline{\text{OE}}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

SNLV162245, SN74LVT162245
3.3-V ABT 16-BIT BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

JUNE 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1)	-0.5 V to 7 V
Current into any output in the low state, I_O : SN54LVT162245 (except A port)	96 mA
SN74LVT162245 (except A port)	128 mA
A port	30 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT162245 (B port)	48 mA
SN74LVT162245 (B port)	64 mA
A port	30 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DGG package	0.8 W
DL package	0.85 W
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions

		SN54LVT162245		SN74LVT162245		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current	B port	-24	-32		mA
		A port	-12	-12		mA
I_{OL}	Low-level output current	B port	24	32		mA
		A port	12	12		mA
I_{OL}^\ddagger	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
T_A	Operating free-air temperature	-55	125	-40	85	°C

‡ Current duty cycle $\leq 50\%$, $f \geq 1$ kHz

PRODUCT PREVIEW

SNLVT162245, SN74LVT162245
3.3-V ABT 16-BIT BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

JUNE 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54LVT162245		SN74LVT162245		UNIT	
			MIN	MAX	MIN	MAX		
V_{IK}	$V_{CC} = 2.7\text{ V}$,	$I_I = -18\text{ mA}$		-1.2		-1.2	V	
V_{OH}	$V_{CC} = 3\text{ V}$,	$I_{OH} = -12\text{ mA}$	A port	2		2	V	
	$V_{CC} = \text{MIN to MAX}^\ddagger$,	$I_{OH} = -100\ \mu\text{A}$		$V_{CC}-0.2$		$V_{CC}-0.2$		
	$V_{CC} = 2.7\text{ V}$,	$I_{OH} = -8\text{ mA}$		2.4		2.4		
	$V_{CC} = 3\text{ V}$,	$I_{OH} = -24\text{ mA}$		2				
	$V_{CC} = 3\text{ V}$,	$I_{OH} = -32\text{ mA}$				2		
V_{OL}	$V_{CC} = 2.7\text{ V}$,	$I_{OL} = 12\text{ mA}$	A port	0.8		0.8	V	
	$V_{CC} = 2.7\text{ V}$,	$I_{OL} = 100\ \mu\text{A}$	B port	0.2		0.2		
	$V_{CC} = 2.7\text{ V}$,	$I_{OL} = 24\text{ mA}$		0.5		0.5		
	$V_{CC} = 3\text{ V}$,	$I_{OL} = 16\text{ mA}$		0.4		0.4		
	$V_{CC} = 3\text{ V}$,	$I_{OL} = 32\text{ mA}$		0.5		0.5		
	$V_{CC} = 3\text{ V}$,	$I_{OL} = 48\text{ mA}$		0.55				
	$V_{CC} = 3\text{ V}$,	$I_{OL} = 64\text{ mA}$				0.55		
I_I	$V_{CC} = 3.6\text{ V}$,	$V_I = V_{CC}$ or GND		Control pins	± 1		± 1	μA
	$V_{CC} = 0$ or MAX^\ddagger ,	$V_I = 5.5\text{ V}$		10		10		
	$V_{CC} = 3.6\text{ V}$,	$V_I = 5.5\text{ V}$	A or B ports §	20		20		
	$V_{CC} = 3.6\text{ V}$,	$V_I = V_{CC}$		1		1		
	$V_{CC} = 3.6\text{ V}$,	$V_I = 0$		-5		-5		
I_{off}	$V_{CC} = 0$,	V_I or $V_O = 0$ to 4.5 V				± 100	μA	
$I_I(\text{hold})$	$V_{CC} = 3\text{ V}$	$V_I = 0.8\text{ V}$	A or B ports	75		75	μA	
		$V_I = 2\text{ V}$		-75		-75		
I_{OZH}	$V_{CC} = 3.6\text{ V}$,	$V_O = 3\text{ V}$		1		1	μA	
I_{OZL}	$V_{CC} = 3.6\text{ V}$,	$V_O = 0.5\text{ V}$		-1		-1	μA	
I_{CC}	$V_{CC} = 3.6\text{ V}$,	$V_I = V_{CC}$ or GND	$I_O = 0$,	Outputs high	0.1		0.1	mA
				Outputs low	5		5	
				Outputs disabled	0.1		0.1	
ΔI_{CC}^\P	$V_{CC} = 3\text{ V}$ to 3.6 V,	One input at $V_{CC} - 0.6\text{ V}$,		0.2		0.2	mA	
C_I	$V_I = 3\text{ V}$ or 0						pF	
C_{IO}	$V_O = 3\text{ V}$ or 0						pF	

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ Unused pins at V_{CC} or GND.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

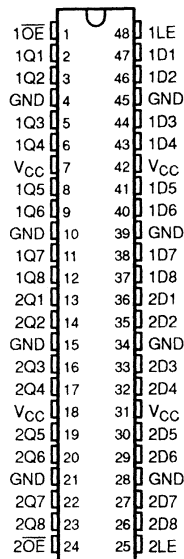


SN54LVT16373, SN74LVT16373 3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS144A - MAY 1992 - REVISED NOVEMBER 1993

- State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Member of the Texas Instruments *Widebus™* Family
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings

SN54LVT16373 . . . WD PACKAGE
SN74LVT16373 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The LVT16373 is a 16-bit transparent D-type latch with 3-state outputs designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The device can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (\overline{OE}) input does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

Widebus is a trademark of Texas Instruments Incorporated.

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SN54LVT16373, SN74LVT16373

3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS144A – MAY 1992 – REVISED NOVEMBER 1993

description (continued)

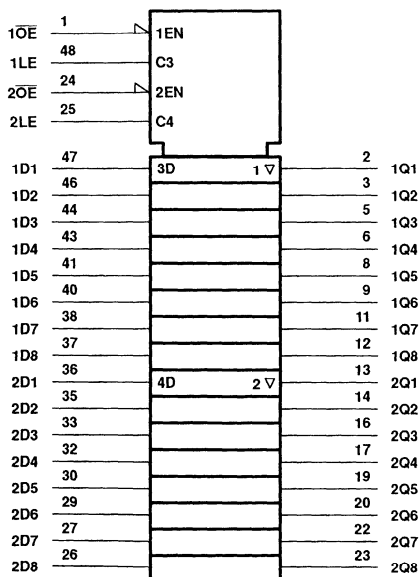
The SN74LVT16373 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT16373 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVT16373 is characterized for operation from -40°C to 85°C .

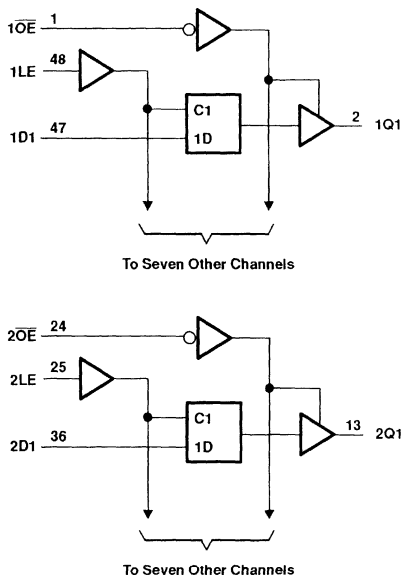
FUNCTION TABLE
(each 8-bit section)

INPUTS			OUTPUT
$\overline{\text{OE}}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN54LVT16373, SN74LVT16373 3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS144A - MAY 1992 - REVISED NOVEMBER 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1)	-0.5 V to 7 V
Current into any output in the low state, I_O : SN54LVT16373	96 mA
SN74LVT16373	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT16373	48 mA
SN74LVT16373	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DGG package	0.8 W
DL package	0.85 W
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions

		SN54LVT16373		SN74LVT16373		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current		-24		-32	mA
I_{OL}	Low-level output current		24		32	mA
I_{OL}^\ddagger	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
T_A	Operating free air temperature	-55	125	-40	85	°C

‡ Current duty cycle $\leq 50\%$, $f \geq 1$ kHz

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



SN54LVT16373, SN74LVT16373
3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES
WITH 3-STATE OUTPUTS

SCBS144A – MAY 1992 – REVISED NOVEMBER 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54LVT16373		SN74LVT16373		UNIT
			MIN	TYP†	MAX	MIN	
V_{IK}	$V_{CC} = 2.7\text{ V}$, $I_I = -18\text{ mA}$				-1.2		V
V_{OH}	$V_{CC} = \text{MIN to MAX}^\ddagger$, $I_{OH} = -100\ \mu\text{A}$		$V_{CC} - 0.2$		$V_{CC} - 0.2$		V
	$V_{CC} = 2.7\text{ V}$, $I_{OH} = -8\text{ mA}$		2.4		2.4		
	$V_{CC} = 3\text{ V}$, $I_{OH} = -24\text{ mA}$		2				
V_{OL}	$V_{CC} = 3\text{ V}$, $I_{OH} = -32\text{ mA}$				2		V
	$V_{CC} = 2.7\text{ V}$, $I_{OL} = 100\ \mu\text{A}$				0.2		
	$V_{CC} = 2.7\text{ V}$, $I_{OL} = 24\text{ mA}$				0.5		
	$V_{CC} = 3\text{ V}$, $I_{OL} = 16\text{ mA}$				0.4		
	$V_{CC} = 3\text{ V}$, $I_{OL} = 32\text{ mA}$				0.5		
I_I	$V_{CC} = 3\text{ V}$, $I_{OL} = 48\text{ mA}$				0.55		V
	$V_{CC} = 3\text{ V}$, $I_{OL} = 64\text{ mA}$				0.55		
	$V_{CC} = 0\text{ or MAX}^\ddagger$, $V_I = 5.5\text{ V}$				10		
	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}\text{ or GND}$		Control pins		± 1		
I_I	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}$		Data pins		1		μA
	$V_{CC} = 3.6\text{ V}$, $V_I = 0$				-5		
	$V_{CC} = 0$, $V_I\text{ or }V_O = 0\text{ to }4.5\text{ V}$				± 100		
I_{off}	$V_{CC} = 0$, $V_I\text{ or }V_O = 0\text{ to }4.5\text{ V}$				± 100		μA
$I_I(\text{hold})$	$V_{CC} = 3\text{ V}$		Data inputs		5		μA
	$V_I = 0.8\text{ V}$				75		
I_{OH}	$V_{CC} = 3\text{ V}$		Data inputs		-75		μA
	$V_I = 2\text{ V}$				-75		
I_{OZH}	$V_{CC} = 3.6\text{ V}$, $V_O = 3\text{ V}$				5		μA
I_{OZL}	$V_{CC} = 3.6\text{ V}$, $V_O = 0.5\text{ V}$				-5		μA
I_{CC}	$V_{CC} = 3.6\text{ V}$, $I_O = 0$, $V_I = V_{CC}\text{ or GND}$		Outputs high		0.09		mA
			Outputs low		5		
			Outputs disabled		0.09		
ΔI_{CC}^\S	$V_{CC} = 3\text{ V to }3.6\text{ V}$, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at $V_{CC}\text{ or GND}$				0.2		mA
C_i	$V_I = 3\text{ V or }0$				5		pF
C_o	$V_O = 3\text{ V or }0$				9.5		pF

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		SN54LVT16373				SN74LVT16373				UNIT
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pw}	Pulse duration, LE high	3.3		3.3		3.3		3.3		ns
t_{su}	Setup time, data before LE↓	0.5		0.5		0.5		0.5		ns
t_h	Hold time, data after LE↓	1.8		2		1.8		2		ns

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



SN54LVT16373, SN74LVT16373
3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES
WITH 3-STATE OUTPUTS

SCBS144A - MAY 1992 - REVISED NOVEMBER 1993

switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT16373			SN74LVT16373				UNIT
			$V_{CC} = 3.3 V \pm 0.3 V$		$V_{CC} = 2.7 V$	$V_{CC} = 3.3 V \pm 0.3 V$		$V_{CC} = 2.7 V$		
			MIN	MAX	MAX	MIN	TYP†	MAX	MAX	
t_{PLH}	D	Q	1.3	5.1	5.8	1.3	2.7	5	5.7	ns
t_{PHL}			1.4	5	5.8	1.4	2.9	4.9	5.7	
t_{PLH}	LE	Q	2.1	7	7.5	2.1	3.6	6	6.8	ns
t_{PHL}			3	8.1	9.4	3	4.7	6.9	8.8	
t_{PZH}	\overline{OE}	Q	1	5.6	6.4	1	2.9	5.3	6.3	ns
t_{PZL}			1.3	5.3	6	1.3	3	5.1	5.9	
t_{PHZ}	\overline{OE}	Q	2.7	7.2	8.2	2.7	4.3	6.8	7.6	ns
t_{PLZ}			2.6	6.1	6.2	2.6	4	5.8	5.9	

† All typical values are at $V_{CC} = 3.3 V$, $T_A = 25^\circ C$.

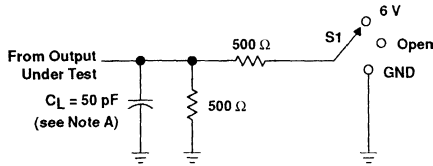
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SN54LVT16373, SN74LVT16373
3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES
WITH 3-STATE OUTPUTS

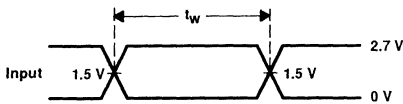
SCBS144A – MAY 1992 – REVISED NOVEMBER 1993

PARAMETER MEASUREMENT INFORMATION

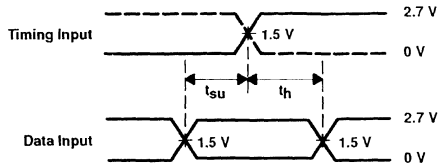


LOAD CIRCUIT FOR OUTPUTS

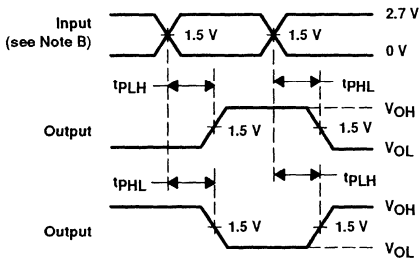
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



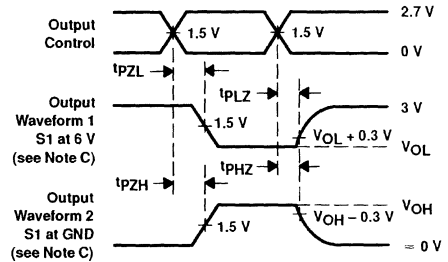
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one transition per measurement.

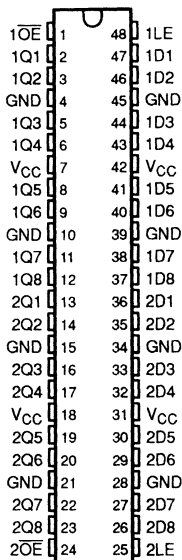
Figure 1. Load Circuit and Voltage Waveforms

SN54LVT162373, SN74LVT162373 3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

JULY 1993

- Output Ports Have Equivalent 22-Ω Series Resistors, So No External Resistors Are Required
- State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Member of the Texas Instruments *Widebus™* Family
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings

SN54LVT162373 ... WD PACKAGE
SN74LVT162373 ... DGG OR DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

The LVT162373 is a 16-bit transparent D-type latch with 3-state outputs designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The device can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (\overline{OE}) input does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

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SN54LVT162373, SN74LVT162373
3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES
WITH 3-STATE OUTPUTS

JULY 1993

description (continued)

The outputs, which are designed to source or sink up to 12 mA, include 22- Ω series resistors to reduce overshoot and undershoot.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVT162373 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

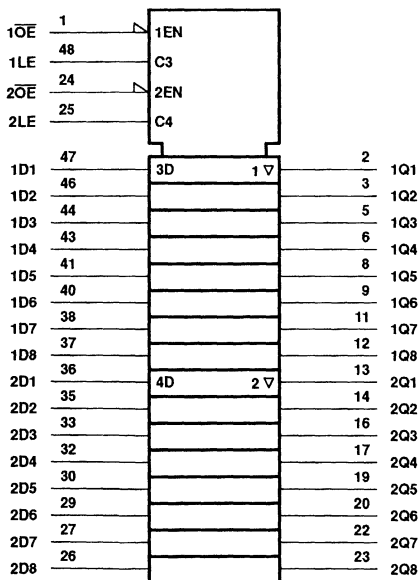
The SN54LVT162373 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVT162373 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each 8-bit section)

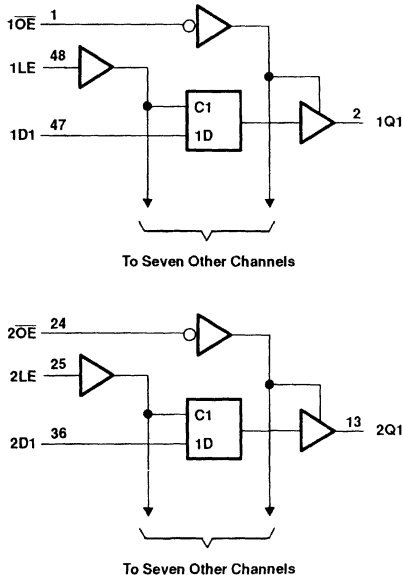
INPUTS			OUTPUT
$\overline{\text{OE}}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

PRODUCT PREVIEW

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN54LVT162373, SN74LVT162373
3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES
WITH 3-STATE OUTPUTS

JULY 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1)	-0.5 V to 7 V
Current into any output in the low state, I_{OL}	30 mA
Current into any output in the high state, I_{OH} (see Note 2)	30 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DGG package	0.8 W
DL package	0.85 W
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp current ratings are observed.
 2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions

		SN54LVT162373		SN74LVT162373		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current		-12		-12	mA
I_{OL}	Low-level output current		12		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
T_A	Operating free-air temperature	-55	125	-40	85	°C

PRODUCT PREVIEW

SN54LVT162373, SN74LVT162373
3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES
WITH 3-STATE OUTPUTS

JULY 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54LVT162373		SN74LVT162373		UNIT
			MIN	MAX	MIN	MAX	
V_{IK}	$V_{CC} = 2.7 \text{ V}$,	$I_I = -18 \text{ mA}$		-1.2		-1.2	V
V_{OH}	$V_{CC} = 3 \text{ V}$,	$I_{OH} = -12 \text{ mA}$	2		2		V
V_{OL}	$V_{CC} = 3 \text{ V}$,	$I_{OL} = 12 \text{ mA}$		0.8		0.8	V
I_I	$V_{CC} = 0 \text{ or MAX}^\ddagger$, $V_I = 5.5 \text{ V}$			10		10	μA
	$V_{CC} = 3.6 \text{ V}$,	$V_I = V_{CC} \text{ or GND}$	Control pins	± 1		± 1	
	$V_{CC} = 3.6 \text{ V}$,	$V_I = V_{CC}$	Data pins	1		1	
	$V_{CC} = 3.6 \text{ V}$,	$V_I = 0$		-5		-5	
I_{off}	$V_{CC} = 0$,	$V_I \text{ or } V_O = 0 \text{ to } 4.5 \text{ V}$				± 100	μA
$I_I(\text{hold})$	$V_{CC} = 3 \text{ V}$	$V_I = 0.8 \text{ V}$	A inputs	75		75	μA
		$V_I = 2 \text{ V}$		-75		-75	
I_{OZH}	$V_{CC} = 3.6 \text{ V}$,	$V_O = 3 \text{ V}$		1		1	μA
I_{OZL}	$V_{CC} = 3.6 \text{ V}$,	$V_O = 0.5 \text{ V}$		-1		-1	μA
I_{CC}	$V_{CC} = 3.6 \text{ V}$,	$V_I = V_{CC} \text{ or GND}$	$I_O = 0$,	Outputs high	0.19	0.1	mA
				Outputs low	5	5	
				Outputs disabled	0.19	0.1	
ΔI_{CC}^\S	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$, One input at $V_{CC} - 0.6 \text{ V}$, Other inputs at V_{CC} or GND			0.2		0.2	mA
C_i	$V_I = 3 \text{ V or } 0$						pF
C_O	$V_O = 3 \text{ V or } 0$						pF

† All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

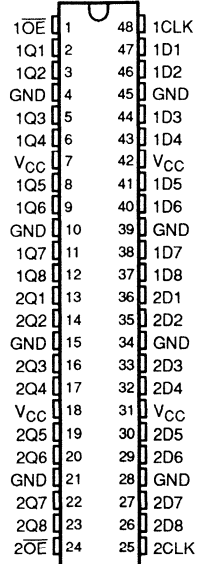


SN54LVT16374, SN74LVT16374 3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCBS145A – MAY 1992 – REVISED OCTOBER 1993

- **State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **Member of the Texas Instruments Widebus™ Family**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54LVT16374 . . . WD PACKAGE
SN74LVT16374 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The LVT16374 is a 16-bit edge-triggered D-type flip-flop with 3-state outputs designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The LVT16374 can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK), the Q outputs of the flip-flop take on the logic levels set up at the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (\overline{OE}) input does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVT16374 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

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SN54LVT16374, SN74LVT16374

3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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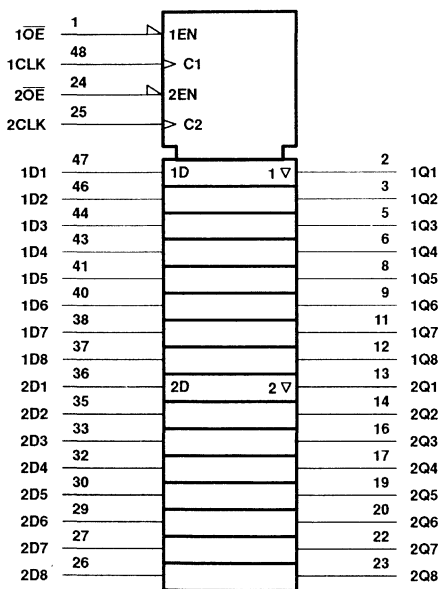
description (continued)

The SN54LVT16374 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVT16374 is characterized for operation from -40°C to 85°C .

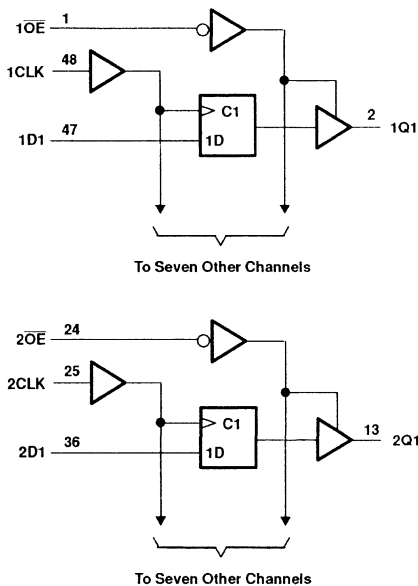
FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
OE	CLK	D	Q
L	\uparrow	H	H
L	\uparrow	L	L
L	H or L	X	Q_0
H	X	X	Z

logic symbol



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN54LVT16374, SN74LVT16374 3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCBS145A – MAY 1992 – REVISED OCTOBER 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1)	-0.5 V to 7 V
Current into any output in the low state, I_{OL} : SN54LVT16374	96 mA
SN74LVT16374	128 mA
Current into any output in the high state, I_{OH} (see Note 2): SN54LVT16374	48 mA
SN74LVT16374	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DGG package	0.8 W
DL package	0.85 W
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions

		SN54LVT16374		SN74LVT16374		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current		-24		-32	mA
I_{OL}	Low-level output current		24		32	mA
I_{OL}^\ddagger	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
T_A	Operating free air temperature	-55	125	-40	85	°C

‡ Current duty cycle $\leq 50\%$, $f \geq 1$ kHz

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SN54LVT16374, SN74LVT16374
3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS
WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54LVT16374			SN74LVT16374			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 2.7\text{ V}$, $I_I = -18\text{ mA}$		-1.2			-1.2			V
V_{OH}	$V_{CC} = \text{MIN to MAX}^\ddagger$, $I_{OH} = -100\ \mu\text{A}$		$V_{CC} - 0.2$			$V_{CC} - 0.2$			V
	$V_{CC} = 2.7\text{ V}$, $I_{OH} = -8\text{ mA}$		2.4			2.4			
	$V_{CC} = 3\text{ V}$, $I_{OH} = -24\text{ mA}$		2						
	$V_{CC} = 3\text{ V}$, $I_{OH} = -32\text{ mA}$					2			
V_{OL}	$V_{CC} = 2.7\text{ V}$, $I_{OL} = 100\ \mu\text{A}$		0.2			0.2			V
	$V_{CC} = 2.7\text{ V}$, $I_{OL} = 24\text{ mA}$		0.5			0.5			
	$V_{CC} = 3\text{ V}$, $I_{OL} = 16\text{ mA}$		0.4			0.4			
	$V_{CC} = 3\text{ V}$, $I_{OL} = 32\text{ mA}$		0.5			0.5			
	$V_{CC} = 3\text{ V}$, $I_{OL} = 48\text{ mA}$		0.55			0.55			
	$V_{CC} = 3\text{ V}$, $I_{OL} = 64\text{ mA}$					0.55			
I_I	$V_{CC} = 0\text{ or MAX}^\ddagger$, $V_I = 5.5\text{ V}$		10			10			μA
	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}\text{ or GND}$		Control pins			± 1			
	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}$		Data pins			1			
	$V_{CC} = 3.6\text{ V}$, $V_I = 0$					-5			
I_{off}	$V_{CC} = 0$, $V_I\text{ or }V_O = 0\text{ to }4.5\text{ V}$					± 100			μA
$I_{I(\text{hold})}$	$V_{CC} = 3\text{ V}$, $V_I = 0.8\text{ V}$		Data inputs			75			μA
	$V_{CC} = 3\text{ V}$, $V_I = 2\text{ V}$					-75			
I_{OZH}	$V_{CC} = 3.6\text{ V}$, $V_O = 3\text{ V}$		5			5			μA
I_{OZL}	$V_{CC} = 3.6\text{ V}$, $V_O = 0.5\text{ V}$		-5			-5			μA
I_{CC}	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}\text{ or GND}$, $I_O = 0$		Outputs high			0.1			mA
			Outputs low			5			
			Outputs disabled			0.1			
ΔI_{CC}^\S	$V_{CC} = 3\text{ V to }3.6\text{ V}$, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at $V_{CC}\text{ or GND}$		0.2			0.2			mA
C_i	$V_I = 3\text{ V or }0$		5			5			pF
C_o	$V_O = 3\text{ V or }0$		9.5			9.5			pF

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		SN54LVT16374				SN74LVT16374				UNIT
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	150	0	150	0	150	0	150	MHz
t_w	Pulse duration, CLK high or low	3.3		3.3		3.3		3.3		ns
t_{su}	Setup time, data before CLK \uparrow	High or low		2.2		2.6		2.2		ns
t_h	Hold time, data after CLK \uparrow	High or low		0.6		0		0.6		ns

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SN54LVT16374, SN74LVT16374 3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCBS145A – MAY 1992 – REVISED OCTOBER 1993

switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

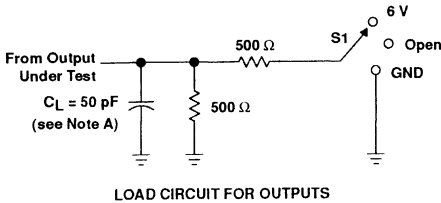
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT16374				SN74LVT16374				UNIT	
			$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CC} = 2.7 \text{ V}$		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CC} = 2.7 \text{ V}$			
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
f_{max}			150		150		150		150		MHz	
t_{PLH}	CLK	Q	1.9	6.6	7.4		1.9	3.6	6.3	7		ns
t_{PHL}			2.3	6.9	7.5		2.3	4.1	6.6	7.2		
t_{PZH}	\overline{OE}	Q	1	5.6	6.4		1	2.7	5.3	6.3		ns
t_{PZL}			1.3	5.3	6		1.3	2.8	5.1	5.9		
t_{PHZ}	\overline{OE}	Q	2.7	7.2	8.2		2.7	4.3	6.8	7.6		ns
t_{PLZ}			2.6	6.1	8.2		2.6	3.9	5.8	5.9		

† All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.

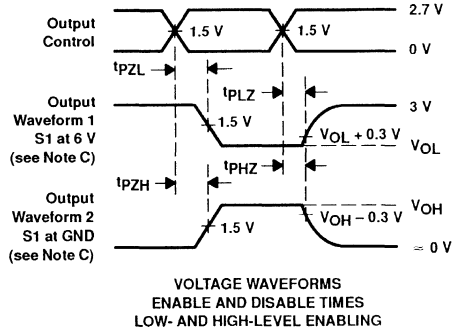
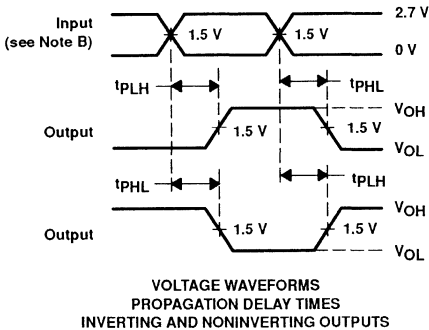
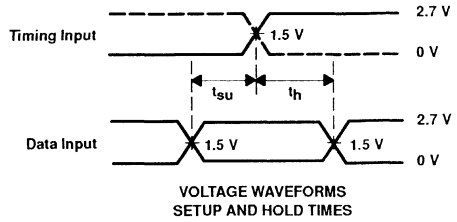
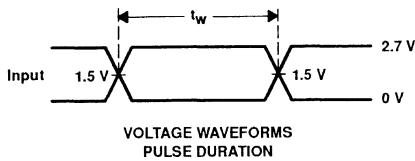
SN54LVT16374, SN74LVT16374
3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS
WITH 3-STATE OUTPUTS

SCBS145A – MAY 1992 – REVISED OCTOBER 1993

PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

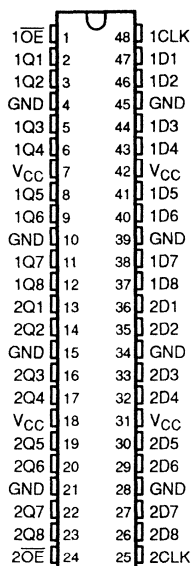
SN54LVT162374, SN74LVT162374

3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

JULY 1993

- Output Ports Have Equivalent 22-Ω Series Resistors, So No External Resistors Are Required
- State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Member of the Texas Instruments *Widebus*™ Family
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings

SN54LVT162374 . . . WD PACKAGE
SN74LVT162374 . . . DGG OR DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

The 'LVT162374 is a 16-bit edge-triggered D-type flip-flop with 3-state outputs designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The 'LVT162374 can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK), the Q outputs of the flip-flop take on the logic levels set up at the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (\overline{OE}) input does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

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SN54LVT162374, SN74LVT162374
3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS
WITH 3-STATE OUTPUTS

JULY 1993

description (continued)

The outputs, which are designed to source or sink up to 12 mA, include 22-Ω series resistors to reduce overshoot and undershoot.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVT162374 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

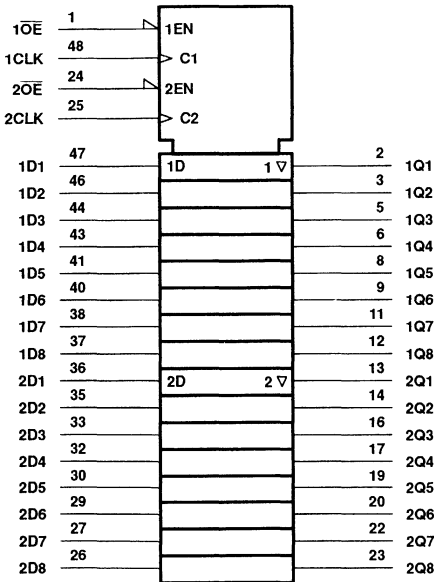
The SN54LVT162374 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LVT162374 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE
(each flip-flop)

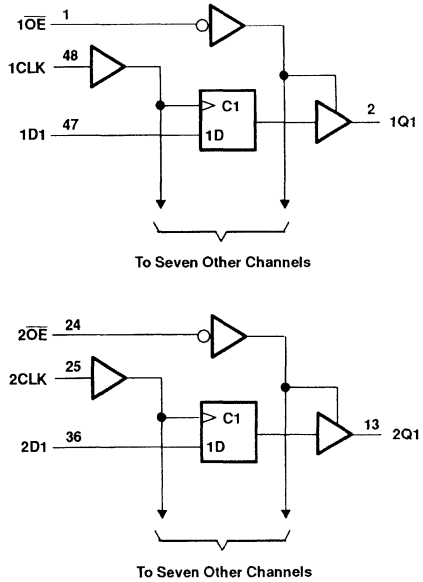
INPUTS			OUTPUT
\overline{OE}	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q ₀
H	X	X	Z

PRODUCT PREVIEW

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN54LVT162374, SN74LVT162374
3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS
WITH 3-STATE OUTPUTS

JULY 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1)	-0.5 V to 7 V
Current into any output in the low state, I_O	30 mA
Current into any output in the high state, I_O (see Note 2)	30 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DGG package	0.8 W
DL package	0.85 W
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions

		SN54LVT162374		SN74LVT162374		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage	0.8		0.8		V
V_I	Input voltage	5.5		5.5		V
I_{OH}	High-level output current	-12		-12		mA
I_{OL}	Low-level output current	12		12		mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
T_A	Operating free-air temperature	-55	125	-40	85	°C

PRODUCT PREVIEW



SN54LVT162374, SN74LVT162374
3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS
WITH 3-STATE OUTPUTS

JULY 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54LVT162374		SN74LVT162374		UNIT	
			MIN	MAX	MIN	MAX		
V_{IK}	$V_{CC} = 2.7 \text{ V}$, $I_I = -18 \text{ mA}$		-1.2		-1.2		V	
V_{OH}	$V_{CC} = 3 \text{ V}$, $I_{OH} = -12 \text{ mA}$		2		2		V	
V_{OL}	$V_{CC} = 3 \text{ V}$, $I_{OL} = 12 \text{ mA}$		0.8		0.8		V	
I_I	$V_{CC} = 0$ or MAX [†] , $V_I = 5.5 \text{ V}$		10		10		μA	
	$V_{CC} = 3.6 \text{ V}$, $V_I = V_{CC}$ or GND	Control pins	± 1		± 1			
	$V_{CC} = 3.6 \text{ V}$, $V_I = V_{CC}$	Data pins	1		1			
	$V_{CC} = 3.6 \text{ V}$, $V_I = 0$		-5		-5			
I_{off}	$V_{CC} = 0$, V_I or $V_O = 0$ to 4.5 V				± 100		μA	
$I_I(\text{hold})$	$V_{CC} = 3 \text{ V}$	$V_I = 0.8 \text{ V}$	A inputs	75		75		μA
		$V_I = 2 \text{ V}$		-75		-75		
I_{OZH}	$V_{CC} = 3.6 \text{ V}$, $V_O = 3 \text{ V}$		1		1		μA	
I_{OZL}	$V_{CC} = 3.6 \text{ V}$, $V_O = 0.5 \text{ V}$		-1		-1		μA	
I_{CC}	$V_{CC} = 3.6 \text{ V}$, $I_O = 0$, $V_I = V_{CC}$ or GND		Outputs high	0.19		0.1		mA
			Outputs low	5		5		
			Outputs disabled	0.19		0.1		
ΔI_{CC}^{\S}	$V_{CC} = 3 \text{ V}$ to 3.6 V , One input at $V_{CC} - 0.6 \text{ V}$, Other inputs at V_{CC} or GND		0.2		0.2		mA	
C_i	$V_I = 3 \text{ V}$ or 0						pF	
C_o	$V_O = 3 \text{ V}$ or 0						pF	

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.

[‡] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

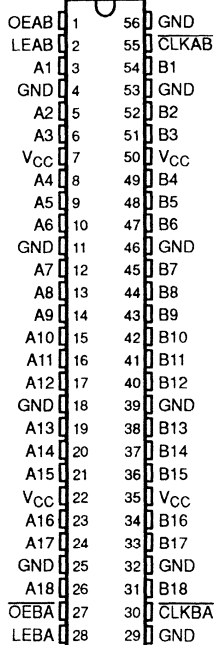
PRODUCT PREVIEW

SN54LVT16500, SN74LVT16500 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS146 - MAY 1992 - REVISED JULY 1993

- State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Member of the Texas Instruments *Widebus™* Family
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- *UBT™* (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings

SN54LVT16500 . . . WD PACKAGE
SN74LVT16500 . . . DGG OR DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

The 'LVT16500 is an 18-bit universal bus transceiver designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

Data flow in each direction is controlled by output-enable (\overline{OEAB} and \overline{OEBA}), latch-enable (LEAB and LEBA), and clock (\overline{CLKAB} and \overline{CLKBA}) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if \overline{CLKAB} is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the high-to-low transition of \overline{CLKAB} . Output-enable OEAB is active high. When OEAB is high, the B-port outputs are active. When OEAB is low, the B-port outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses \overline{OEBA} , LEBA, and \overline{CLKBA} . The output enables are complementary (OEAB is active high, and \overline{OEBA} is active low).

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

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SN54LVT16500, SN74LVT16500
3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

SCBS146 – MAY 1992 – REVISED JULY 1993

description (continued)

The SN74LVT16500 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT16500 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVT16500 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE†

INPUTS				OUTPUT
OEAB	LEAB	CLKAB	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	B_0^{\ddagger}
H	L	L	X	B_0^{\S}

† A-to-B data flow is shown; B-to-A flow is similar but uses OEBA, LEBA, and CLKBA.

‡ Output level before the indicated steady-state input conditions were established.

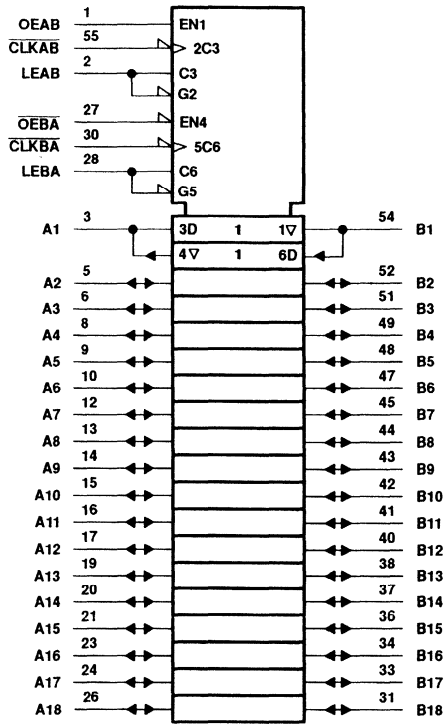
§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low.

PRODUCT PREVIEW

SN54LVT16500, SN74LVT16500
 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS
 WITH 3-STATE OUTPUTS

SCBS146 - MAY 1992 - REVISED JULY 1993

logic symbol



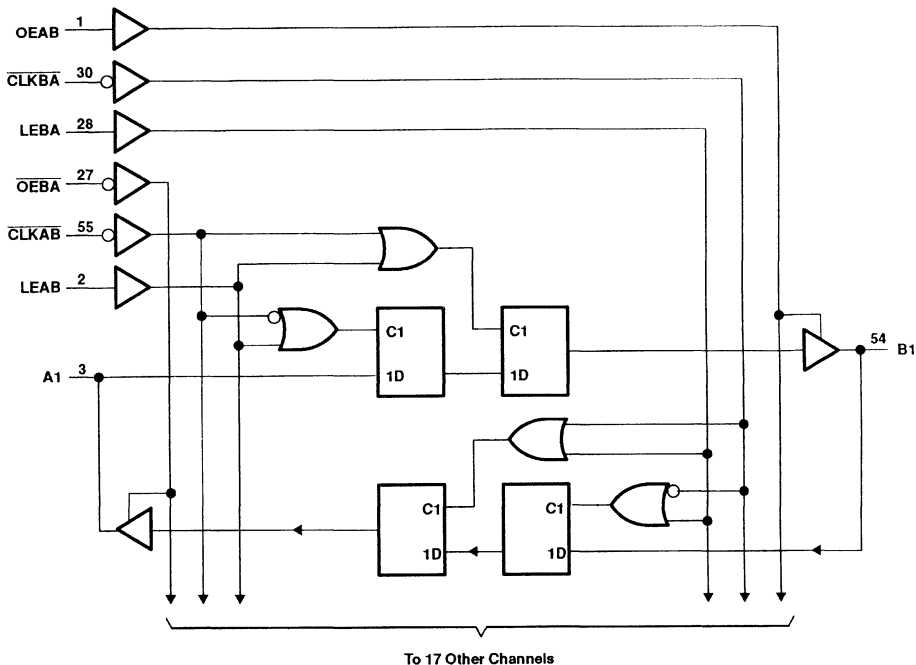
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

SN54LVT16500, SN74LVT16500
3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

SCBS146 – MAY 1992 – REVISED JULY 1993

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1)	-0.5 V to 7 V
Current into any output in the low state, I_{OL} : SN54LVT16500	96 mA
SN74LVT16500	128 mA
Current into any output in the high state, I_{OH} (see Note 2): SN54LVT16500	48 mA
SN74LVT16500	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DGG package	1 W
DL package	1 W
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.



SN54LVT16500, SN74LVT16500
3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

SCBS146 – MAY 1992 – REVISED JULY 1993

recommended operating conditions

		SN54LVT16500		SN74LVT16500		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage	0.8		0.8		V
V _I	Input voltage	5.5		5.5		V
I _{OH}	High-level output current	-24		-32		mA
I _{OL}	Low-level output current	24		32		mA
I _{OL} †	Low-level output current	48		64		mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled		10		ns/V
T _A	Operating free-air temperature	-55	125	-40	85	°C

† Current duty cycle ≤ 50%, f ≥ 1 kHz

PRODUCT PREVIEW

SN54LVT16500, SN74LVT16500
3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

SCBS146 - MAY 1992 - REVISED JULY 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54LVT16500		SN74LVT16500		UNIT
			MIN	MAX	MIN	MAX	
V_{IK}	$V_{CC} = 2.7\text{ V}$, $I_I = -18\text{ mA}$		-1.2		-1.2		V
V_{OH}	$V_{CC} = \text{MIN to MAX}^\ddagger$, $I_{OH} = -100\ \mu\text{A}$		$V_{CC}-0.2$		$V_{CC}-0.2$		V
	$V_{CC} = 2.7\text{ V}$, $I_{OH} = -8\text{ mA}$		2.4		2.4		
	$V_{CC} = 3\text{ V}$, $I_{OH} = -24\text{ mA}$		2				
	$V_{CC} = 3\text{ V}$, $I_{OH} = -32\text{ mA}$				2		
V_{OL}	$V_{CC} = 2.7\text{ V}$, $I_{OL} = 100\ \mu\text{A}$		0.2		0.2		V
	$V_{CC} = 2.7\text{ V}$, $I_{OL} = 24\text{ mA}$		0.5		0.5		
	$V_{CC} = 3\text{ V}$, $I_{OL} = 16\text{ mA}$		0.4		0.4		
	$V_{CC} = 3\text{ V}$, $I_{OL} = 32\text{ mA}$		0.5		0.5		
	$V_{CC} = 3\text{ V}$, $I_{OL} = 48\text{ mA}$		0.55				
	$V_{CC} = 3\text{ V}$, $I_{OL} = 64\text{ mA}$				0.55		
I_I	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}$ or GND		Control pins		± 1		μA
	$V_{CC} = 0$ or MAX^\ddagger , $V_I = 5.5\text{ V}$				10		
	$V_{CC} = 3.6\text{ V}$, $V_I = 5.5\text{ V}$				20		
	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}$		A or B ports §		1		
	$V_{CC} = 3.6\text{ V}$, $V_I = 0$				-5		
I_{off}	$V_{CC} = 0$, V_I or $V_O = 0$ to 4.5 V				± 100		μA
$I_{I(\text{hold})}$	$V_{CC} = 3\text{ V}$		A or B ports		75		μA
	$V_I = 0.8\text{ V}$				75		
	$V_I = 2\text{ V}$				-75		
I_{OZH}	$V_{CC} = 3.6\text{ V}$, $V_O = 3\text{ V}$		1		1		μA
I_{OZL}	$V_{CC} = 3.6\text{ V}$, $V_O = 0.5\text{ V}$		-1		-1		μA
I_{CC}	$V_{CC} = 3.6\text{ V}$, $I_O = 0$, $V_I = V_{CC}$ or GND		Outputs high		0.1		mA
			Outputs low		5		
			Outputs disabled		0.1		
ΔI_{CC}^\P	$V_{CC} = 3\text{ V}$ to 3.6 V , One input at $V_{CC} - 0.6\text{ V}$, Other inputs at V_{CC} or GND		0.2		0.2		mA
C_i	$V_I = 3\text{ V}$ or 0						pF
C_{io}	$V_O = 3\text{ V}$ or 0						pF

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ Unused pins at V_{CC} or GND

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

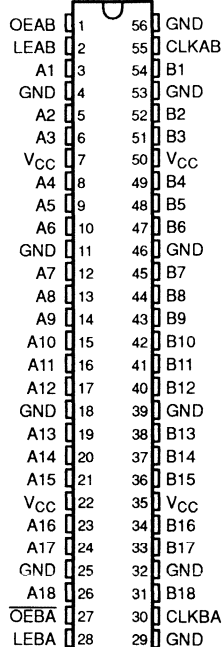


SN54LVT16501, SN74LVT16501 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS147 – MAY 1992 – REVISED JULY 1993

- State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Member of the Texas Instruments *Widebus™* Family
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- *UBT™* (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings

SN54LVT16501 ... WD PACKAGE
SN74LVT16501 ... DGG OR DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

The LVT16501 is an 18-bit universal bus transceiver designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

Data flow in each direction is controlled by output-enable (\overline{OEBA} and OEAB), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses \overline{OEBA} , LEBA, and CLKBA. The output enables are complementary (OEAB is active high, and \overline{OEBA} is active low).

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

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SN54LVT16501, SN74LVT16501
3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

SCBS147 – MAY 1992 – REVISED JULY 1993

description (continued)

The SN74LVT16501 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT16501 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVT16501 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE†

INPUTS				OUTPUT
OEAB	LEAB	CLKAB	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	H	X	B_0^{\ddagger}
H	L	L	X	B_0^{\S}

† A-to-B data flow is shown; B-to-A flow is similar but uses OEBA, LEBA, and CLKBA.

‡ Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low.

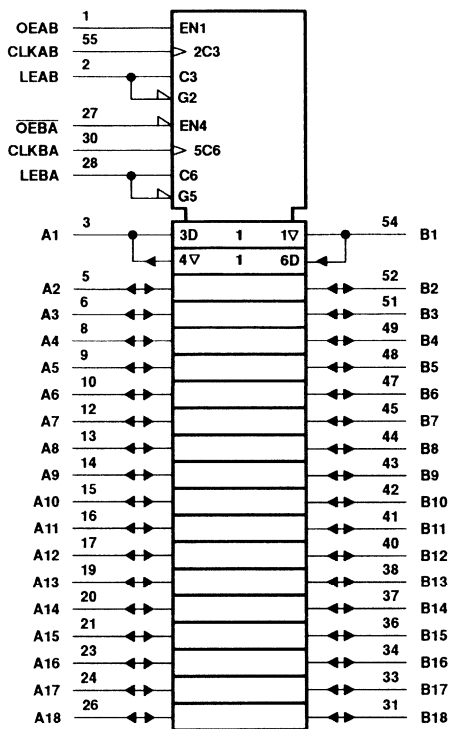
§ Output level before the indicated steady-state input conditions were established.

PRODUCT PREVIEW

SN54LVT16501, SN74LVT16501
 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS
 WITH 3-STATE OUTPUTS

SCBS147 – MAY 1992 – REVISED JULY 1993

logic symbol†



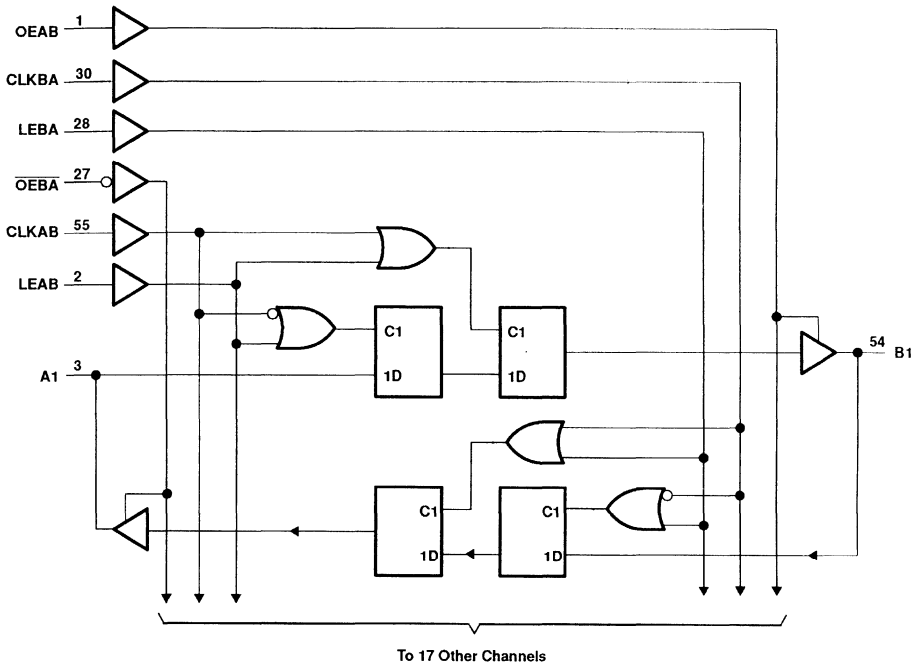
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

SN54LVT16501, SN74LVT16501
3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

SCBS147 – MAY 1992 – REVISED JULY 1993

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1)	-0.5 V to 7 V
Current into any output in the low state, I_O : SN54LVT16501	96 mA
SN74LVT16501	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT16501	48 mA
SN74LVT16501	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DGG package	1 W
DL package	1 W
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.



SN54LVT16501, SN74LVT16501
3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

SCBS147 – MAY 1992 – REVISED JULY 1993

recommended operating conditions

		SN54LVT16501		SN74LVT16501		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage		5.5		5.5	V
I _{OH}	High-level output current		-24		-32	mA
I _{OL}	Low-level output current		24		32	mA
I _{OL} †	Low-level output current		48		64	mA
Δt/Δv	Input transition rise or fall rate		10		10	ns/V
			Outputs enabled		10	
T _A	Operating free-air temperature	-55	125	-40	85	°C

† Current duty cycle ≤ 50%, f ≥ 1 kHz

PRODUCT PREVIEW

SN54LVT16501, SN74LVT16501
3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

SCBS147 – MAY 1992 – REVISED JULY 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54LVT16501		SN74LVT16501		UNIT
			MIN	MAX	MIN	MAX	
V_{IK}	$V_{CC} = 2.7\text{ V}$, $I_I = -18\text{ mA}$		-1.2		-1.2		V
V_{OH}	$V_{CC} = \text{MIN to MAX}^\ddagger$, $I_{OH} = -100\ \mu\text{A}$		$V_{CC} - 0.2$		$V_{CC} - 0.2$		V
	$V_{CC} = 2.7\text{ V}$, $I_{OH} = -8\text{ mA}$		2.4		2.4		
	$V_{CC} = 3\text{ V}$, $I_{OH} = -24\text{ mA}$		2				
	$V_{CC} = 3\text{ V}$, $I_{OH} = -32\text{ mA}$				2		
V_{OL}	$V_{CC} = 2.7\text{ V}$, $I_{OL} = 100\ \mu\text{A}$		0.2		0.2		V
	$V_{CC} = 2.7\text{ V}$, $I_{OL} = 24\text{ mA}$		0.5		0.5		
	$V_{CC} = 3\text{ V}$, $I_{OL} = 16\text{ mA}$		0.4		0.4		
	$V_{CC} = 3\text{ V}$, $I_{OL} = 32\text{ mA}$		0.5		0.5		
	$V_{CC} = 3\text{ V}$, $I_{OL} = 48\text{ mA}$		0.55				
	$V_{CC} = 3\text{ V}$, $I_{OL} = 64\text{ mA}$				0.55		
I_I	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}$ or GND		Control pins		± 1		μA
	$V_{CC} = 0$ or MAX^\ddagger , $V_I = 5.5\text{ V}$				10		
	$V_{CC} = 3.6\text{ V}$, $V_I = 5.5\text{ V}$				20		
	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}$		A or B ports§		1		
	$V_{CC} = 3.6\text{ V}$, $V_I = 0$				-5		
I_{off}	$V_{CC} = 0$, V_I or $V_O = 0$ to 4.5 V				± 100		μA
$I_I(\text{hold})$	$V_{CC} = 3\text{ V}$, $V_I = 0.8\text{ V}$		A or B ports		75		μA
	$V_{CC} = 3\text{ V}$, $V_I = 2\text{ V}$				-75		
I_{OZH}	$V_{CC} = 3.6\text{ V}$, $V_O = 3\text{ V}$				1		μA
I_{OZL}	$V_{CC} = 3.6\text{ V}$, $V_O = 0.5\text{ V}$				-1		μA
I_{CC}	$V_{CC} = 3.6\text{ V}$, $I_O = 0$, $V_I = V_{CC}$ or GND		Outputs high		0.1		mA
			Outputs low		5		
			Outputs disabled		0.1		
ΔI_{CC}^\ddagger	$V_{CC} = 3\text{ V to } 3.6\text{ V}$, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at V_{CC} or GND				0.2		mA
C_i	$V_I = 3\text{ V}$ or 0						pF
C_{IO}	$V_O = 3\text{ V}$ or 0						pF

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ Unused pins at V_{CC} or GND

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

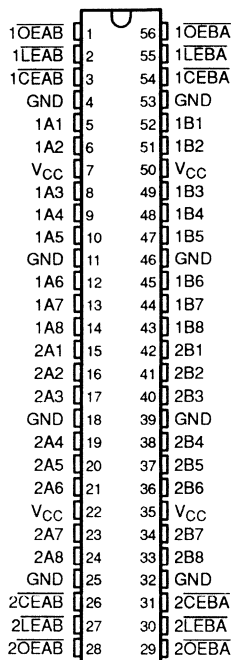


SN54LVT16543, SN74LVT16543 3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS148 – MAY 1992 – REVISED JULY 1993

- **State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **Member of the Texas Instruments *Widebus*[™] Family**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54LVT16543 . . . WD PACKAGE
SN74LVT16543 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The 1LVT16543 is a 16-bit registered transceiver designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. The device can be used as two 8-bit transceivers or one 16-bit transceiver. Separate latch-enable ($\overline{\text{LEAB}}$ or $\overline{\text{LEBA}}$) and output-enable ($\overline{\text{OEAB}}$ or $\overline{\text{OEBA}}$) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable ($\overline{\text{CEAB}}$) input must be low in order to enter data from A or to output data from B. If $\overline{\text{CEAB}}$ is low and $\overline{\text{LEAB}}$ is low, the A-to-B latches are transparent; a subsequent low-to-high transition of $\overline{\text{LEAB}}$ puts the A latches in the storage mode. With $\overline{\text{CEAB}}$ and $\overline{\text{OEAB}}$ both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the $\overline{\text{CEBA}}$, $\overline{\text{LEBA}}$, and $\overline{\text{OEBA}}$ inputs.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVT16543 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT16543 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LVT16543 is characterized for operation from -40°C to 85°C.

Widebus is a trademark of Texas Instruments Incorporated.

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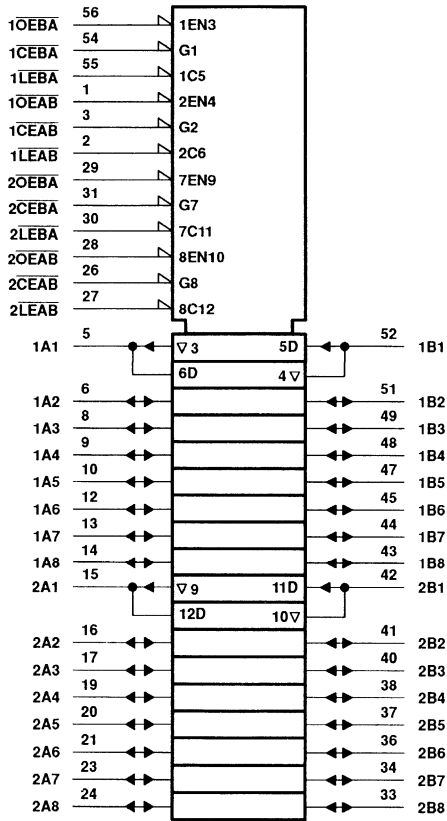
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PRODUCT PREVIEW

SN54LVT16543, SN74LVT16543
3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS
WITH 3-STATE OUTPUTS

SCBS148 - MAY 1992 - REVISED JULY 1993

logic symbol†

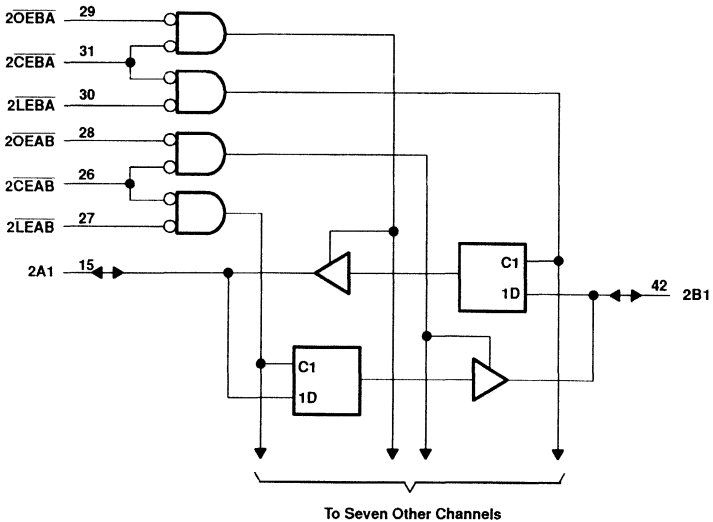
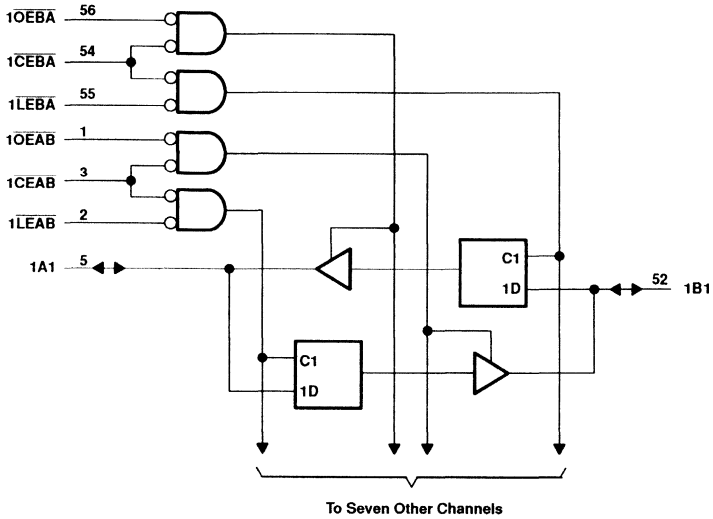


PRODUCT PREVIEW

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN54LVT16543, SN74LVT16543
 3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS
 WITH 3-STATE OUTPUTS
SCBS148 - MAY 1992 - REVISED JULY 1993

logic diagram (positive logic)



PRODUCT PREVIEW

SN54LVT16543, SN74LVT16543
3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS
WITH 3-STATE OUTPUTS

SCBS148 – MAY 1992 – REVISED JULY 1993

FUNCTION TABLE†
 (each 8-bit section)

INPUTS				OUTPUT B
CEAB	LEAB	OEAB	A	
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B_0^\ddagger
L	L	L	L	L
L	L	L	H	H

† A-to-B data flow is shown; B-to-A flow control is the same except that it uses \overline{CEBA} , \overline{LEBA} , and \overline{OEBA} .

‡ Output level before the indicated steady-state input conditions were established.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Current into any output in the low state, I_{OL} : SN54LVT16543	96 mA
SN74LVT16543	128 mA
Current into any output in the high state, I_{OH} (see Note 2): SN54LVT16543	48 mA
SN74LVT16543	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DGG package	1 W
DL package	1 W
Storage temperature range	–65°C to 150°C

§ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions

		SN54LVT16543		SN74LVT16543		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage	0.8		0.8		V
V_I	Input voltage	5.5		5.5		V
I_{OH}	High-level output current	–24		–32		mA
I_{OL}	Low-level output current	24		32		mA
I_{OL}^\ddagger	Low-level output current	48		64		mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

‡ Current duty cycle $\leq 50\%$, $f \geq 1$ kHz

PRODUCT PREVIEW



SN54LVT16543, SN74LVT16543
3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS
WITH 3-STATE OUTPUTS

SCBS148 - MAY 1992 - REVISED JULY 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54LVT16543		SN74LVT16543		UNIT	
			MIN	MAX	MIN	MAX		
V_{IK}	$V_{CC} = 2.7 \text{ V}$, $I_I = -18 \text{ mA}$		-1.2		-1.2		V	
V_{OH}	$V_{CC} = \text{MIN to MAX}^\dagger$, $I_{OH} = -100 \mu\text{A}$		$V_{CC} - 0.2$		$V_{CC} - 0.2$		V	
	$V_{CC} = 2.7 \text{ V}$, $I_{OH} = -8 \text{ mA}$		2.4		2.4			
	$V_{CC} = 3 \text{ V}$, $I_{OH} = -24 \text{ mA}$		2					
	$V_{CC} = 3 \text{ V}$, $I_{OH} = -32 \text{ mA}$				2			
V_{OL}	$V_{CC} = 2.7 \text{ V}$, $I_{OL} = 100 \mu\text{A}$		0.2		0.2		V	
	$V_{CC} = 2.7 \text{ V}$, $I_{OL} = 24 \text{ mA}$		0.5		0.5			
	$V_{CC} = 3 \text{ V}$, $I_{OL} = 16 \text{ mA}$		0.4		0.4			
	$V_{CC} = 3 \text{ V}$, $I_{OL} = 32 \text{ mA}$		0.5		0.5			
	$V_{CC} = 3 \text{ V}$, $I_{OL} = 48 \text{ mA}$		0.55					
	$V_{CC} = 3 \text{ V}$, $I_{OL} = 64 \text{ mA}$				0.55			
I_I	$V_{CC} = 3.6 \text{ V}$, $V_I = V_{CC} \text{ or GND}$		Control pins	± 1		± 1		μA
	$V_{CC} = 0 \text{ or MAX}^\ddagger$, $V_I = 5.5 \text{ V}$			10		10		
	$V_{CC} = 3.6 \text{ V}$, $V_I = 5.5 \text{ V}$		A or B ports §	20		20		
	$V_{CC} = 3.6 \text{ V}$, $V_I = V_{CC}$			5		5		
	$V_{CC} = 3.6 \text{ V}$, $V_I = 0$			-10		-10		
I_{off}	$V_{CC} = 0$, $V_I \text{ or } V_O = 0 \text{ to } 4.5 \text{ V}$				± 100		μA	
$I_{I(\text{hold})}$	$V_{CC} = 3 \text{ V}$	$V_I = 0.8 \text{ V}$	A or B ports	75		75		μA
		$V_I = 2 \text{ V}$		-75		-75		
I_{OZH}	$V_{CC} = 3.6 \text{ V}$, $V_O = 3 \text{ V}$		1		1		μA	
I_{OZL}	$V_{CC} = 3.6 \text{ V}$, $V_O = 0.5 \text{ V}$		-1		-1		μA	
I_{CC}	$V_{CC} = 3.6 \text{ V}$, $V_I = V_{CC} \text{ or GND}$, $I_O = 0$		Outputs high	0.1		0.1		mA
			Outputs low	5		5		
			Outputs disabled	0.1		0.1		
ΔI_{CC}^\ddagger	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$, One input at $V_{CC} - 0.6 \text{ V}$, Other inputs at V_{CC} or GND		0.2		0.2		mA	
C_I	$V_I = 3 \text{ V or } 0$						pF	
C_{IO}	$V_O = 3 \text{ V or } 0$						pF	

† All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ Unused pins at V_{CC} or GND

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

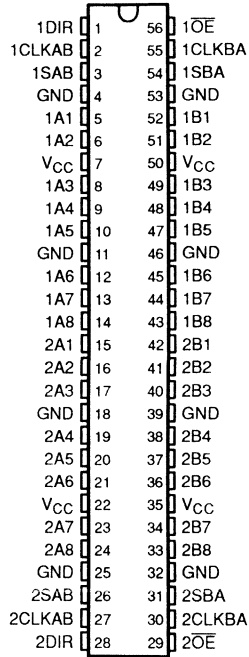
PRODUCT PREVIEW

SN54LVT16646, SN74LVT16646 3.3-V ABT 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS149 - MAY 1992 - REVISED JULY 1993

- **State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **Member of the Texas Instruments *Widebus™* Family**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54LVT16646 . . . WD PACKAGE
SN74LVT16646 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The LVT16646 is a 16-bit bus transceiver designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The device can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the LVT16646 .

Output-enable (\overline{OE}) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. The direction control (DIR) determines which bus receives data when \overline{OE} is low. In the isolation mode (\overline{OE} high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

Widebus is a trademark of Texas Instruments Incorporated.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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PRODUCT PREVIEW

SN54LVT16646, SN74LVT16646
3.3-V ABT 16-BIT BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

SCBS149 – MAY 1992 – REVISED JULY 1993

description (continued)

The SN74LVT16646 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT16646 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT16646 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION
OE	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	L	L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	L	X	H	X	Input	Output	Stored A data to B bus

† The data output functions may be enabled or disabled by various signals at the OE and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.

PRODUCT PREVIEW

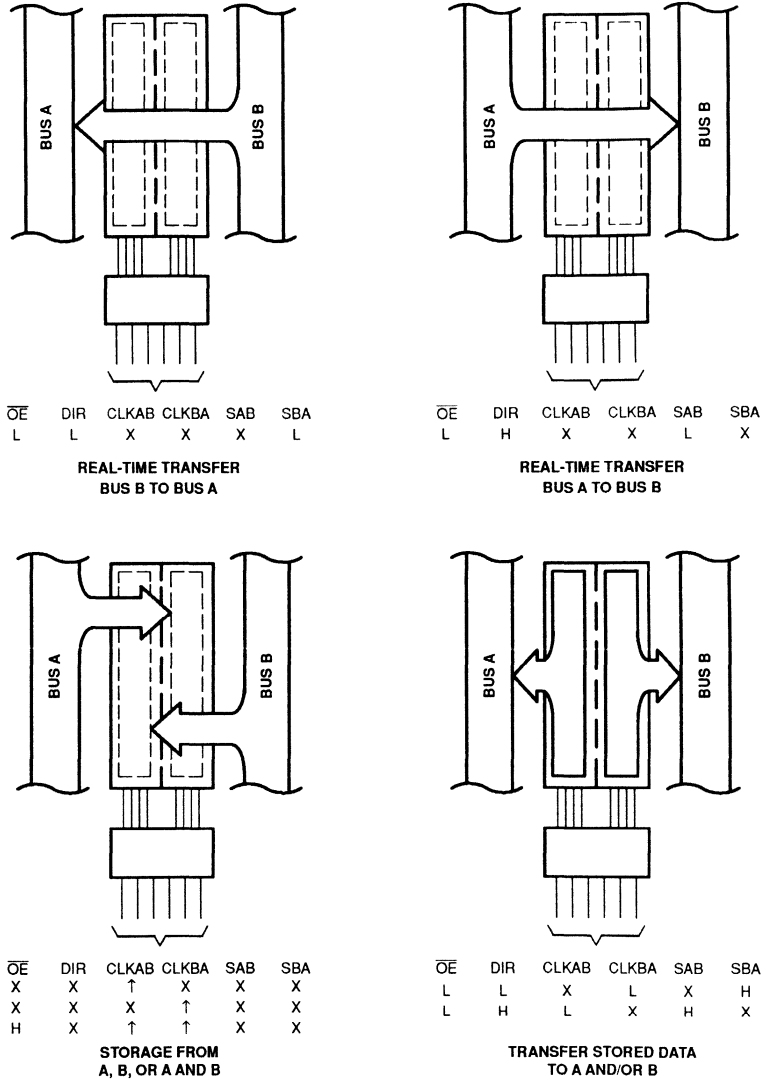


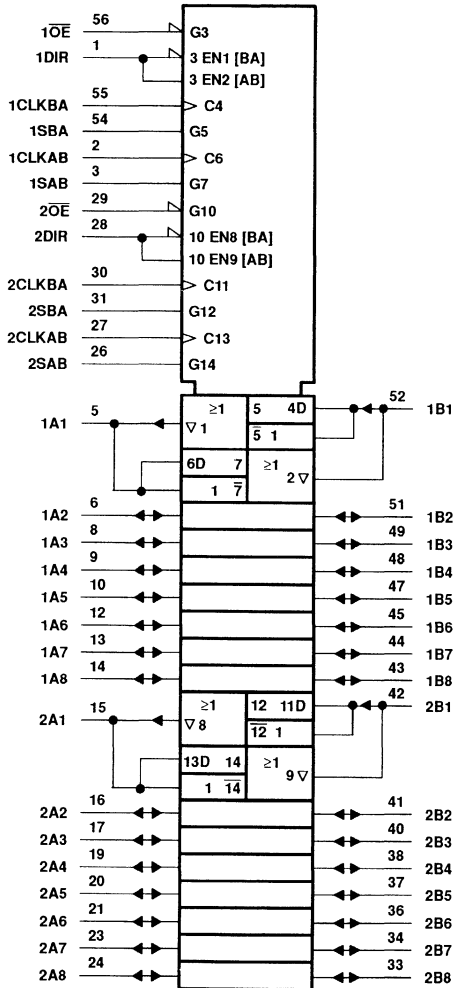
Figure 1. Bus-Management Functions

PRODUCT PREVIEW

SN54LVT16646, SN74LVT16646
3.3-V ABT 16-BIT BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

SCBS149 – MAY 1992 – REVISED JULY 1993

logic symbol†



PRODUCT PREVIEW

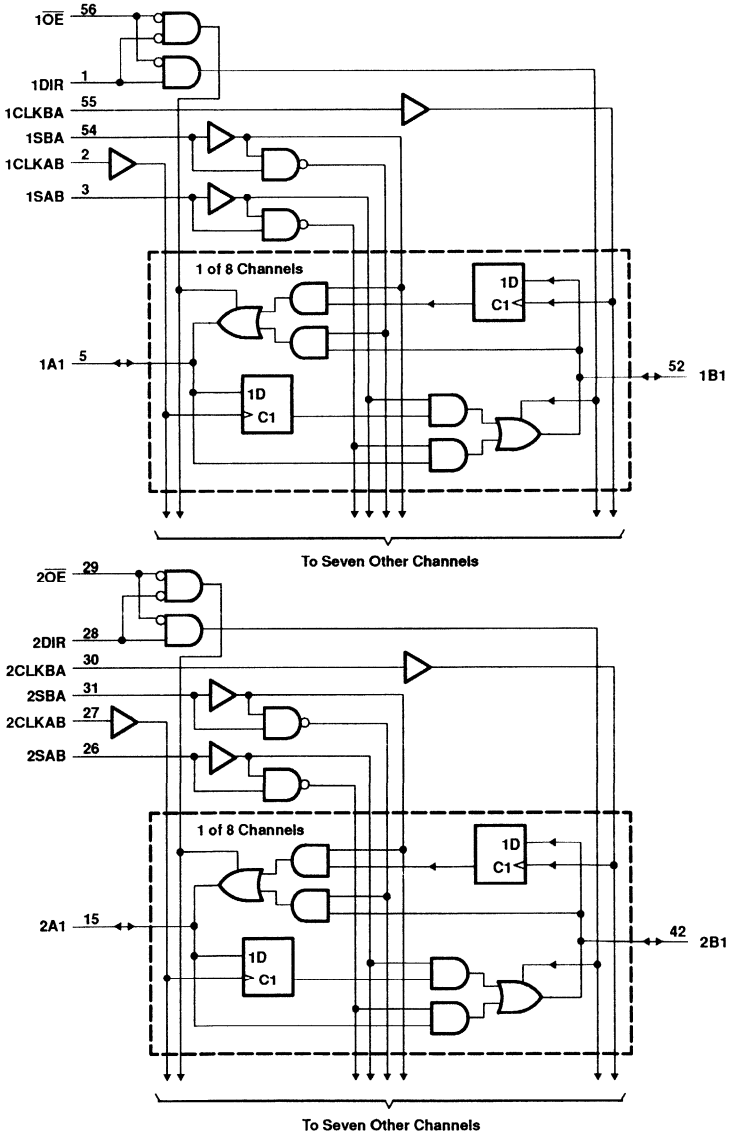
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



SN54LVT16646, SN74LVT16646
 3.3-V ABT 16-BIT BUS TRANSCEIVERS
 WITH 3-STATE OUTPUTS

SCBS149 - MAY 1992 - REVISED JULY 1993

logic diagram (positive logic)



PRODUCT PREVIEW

SN54LVT16646, SN74LVT16646
3.3-V ABT 16-BIT BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

SCBS149 – MAY 1992 – REVISED JULY 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1)	-0.5 V to 7 V
Current into any output in the low state, I_{OL} : SN54LVT16646	96 mA
SN74LVT16646	128 mA
Current into any output in the high state, I_{OH} (see Note 2): SN54LVT16646	48 mA
SN74LVT16646	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DGG package	1 W
DL package	1 W
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions

	SN54LVT16646		SN74LVT16646		UNIT
	MIN	MAX	MIN	MAX	
V_{CC} Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH} High-level input voltage	2		2		V
V_{IL} Low-level input voltage		0.8		0.8	V
V_I Input voltage		5.5		5.5	V
I_{OH} High-level output current		-24		-32	mA
I_{OL} Low-level output current		24		32	mA
I_{OL}^\ddagger Low-level output current		48		64	mA
$\Delta t/\Delta v$ Input transition rise or fall rate	Outputs enabled		10	10	ns/V
T_A Operating free-air temperature	-55	125	-40	85	°C

‡ Current duty cycle $\leq 50\%$, $f \geq 1$ kHz

PRODUCT PREVIEW



SN54LVT16646, SN74LVT16646
3.3-V ABT 16-BIT BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS
 SCBS149 – MAY 1992 – REVISED JULY 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54LVT16646		SN74LVT16646		UNIT
			MIN	MAX	MIN	MAX	
V_{IK}	$V_{CC} = 2.7\text{ V}$, $I_I = -18\text{ mA}$		-1.2		-1.2		V
V_{OH}	$V_{CC} = \text{MIN to MAX}^\ddagger$, $I_{OH} = -100\ \mu\text{A}$		$V_{CC} - 0.2$		$V_{CC} - 0.2$		V
	$V_{CC} = 2.7\text{ V}$, $I_{OH} = -8\text{ mA}$		2.4		2.4		
	$V_{CC} = 3\text{ V}$, $I_{OH} = -24\text{ mA}$		2				
V_{OL}	$V_{CC} = 3\text{ V}$, $I_{OH} = -32\text{ mA}$				2		V
	$V_{CC} = 2.7\text{ V}$, $I_{OL} = 100\ \mu\text{A}$		0.2		0.2		
	$V_{CC} = 2.7\text{ V}$, $I_{OL} = 24\text{ mA}$		0.5		0.5		
	$V_{CC} = 3\text{ V}$, $I_{OL} = 16\text{ mA}$		0.4		0.4		
	$V_{CC} = 3\text{ V}$, $I_{OL} = 32\text{ mA}$		0.5		0.5		
	$V_{CC} = 3\text{ V}$, $I_{OL} = 48\text{ mA}$		0.55				
I_I	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}$ or GND		Control pins		± 1		μA
	$V_{CC} = 0$ or MAX^\ddagger , $V_I = 5.5\text{ V}$		A or B ports§		10		
	$V_{CC} = 3.6\text{ V}$, $V_I = 5.5\text{ V}$				20		
	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}$				5		
	$V_{CC} = 3.6\text{ V}$, $V_I = 0$				-10		
I_{off}	$V_{CC} = 0$, V_I or $V_O = 0$ to 4.5 V				± 100		μA
$I_{I(\text{hold})}$	$V_{CC} = 3\text{ V}$		A or B ports		75		μA
	$V_I = 0.8\text{ V}$				75		
	$V_I = 2\text{ V}$				-75		
I_{OZH}	$V_{CC} = 3.6\text{ V}$, $V_O = 3\text{ V}$				1		μA
I_{OZL}	$V_{CC} = 3.6\text{ V}$, $V_O = 0.5\text{ V}$				-1		μA
I_{CC}	$V_{CC} = 3.6\text{ V}$, $I_O = 0$, $V_I = V_{CC}$ or GND		Outputs high		0.1		mA
			Outputs low		5		
			Outputs disabled		0.1		
ΔI_{CC}^\ddagger	$V_{CC} = 3\text{ V}$ to 3.6 V , One input at $V_{CC} - 0.6\text{ V}$, Other inputs at V_{CC} or GND				0.2		mA
C_i	$V_I = 3\text{ V}$ or 0						pF
C_{iO}	$V_O = 3\text{ V}$ or 0						pF

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ Unused pins at V_{CC} or GND

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

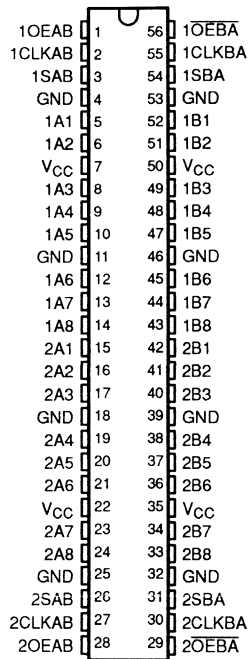
PRODUCT PREVIEW

SN54LVT16652, SN74LVT16652 3.3-V ABT 16-BIT BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCBS150 – MAY 1992 – REVISED JULY 1993

- **State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **Member of the Texas Instruments Widebus™ Family**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54LVT16652 . . . WD PACKAGE
SN74LVT16652 . . . DGG OR DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

The LVT16652 is a 16-bit bus transceiver designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. The device can be used as two 8-bit transceivers or one 16-bit transceiver.

Complementary output-enable (OEAB and $\overline{\text{OEBA}}$) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high input level selects stored data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the LVT16652.

Data on the A or B bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the levels on the select-control or output-enable inputs. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and OEBA. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus line are at high impedance, each set of bus lines remains at its last level configuration.

Widebus is a trademark of Texas Instruments Incorporated.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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SN54LVT16652, SN74LVT16652

3.3-V ABT 16-BIT BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCBS150 – MAY 1992 – REVISED JULY 1993

description (continued)

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVT16652 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT16652 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVT16652 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
L	H	L	L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	L	X	X	Input	Unspecified‡	Store A, hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers
L	X	L	↑	X	X	Unspecified‡	Input	Hold A, store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	L	X	H	X	Input	Output	Stored A data to B bus
H	L	L	L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

† The data output functions may be enabled or disabled by a variety of level combinations at the OEAB or OEBA inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition on the clock inputs.

‡ Select control = L; clocks can occur simultaneously.

Select control = H; clocks must be staggered in order to load both registers.

PRODUCT PREVIEW



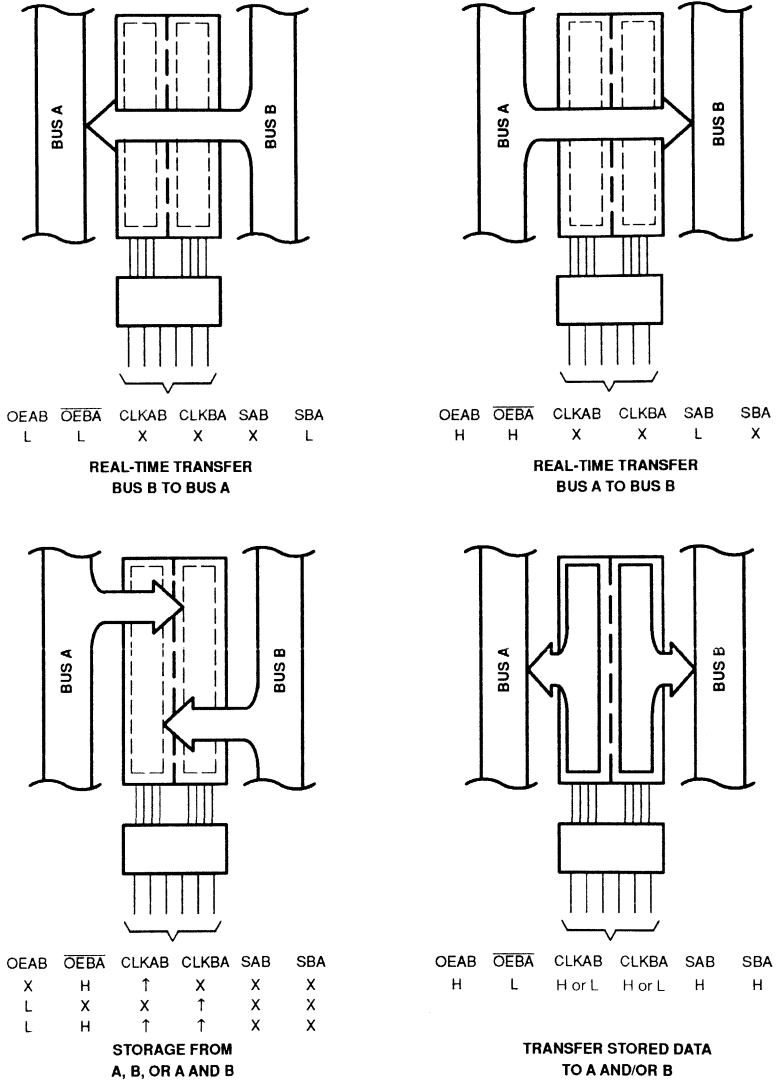


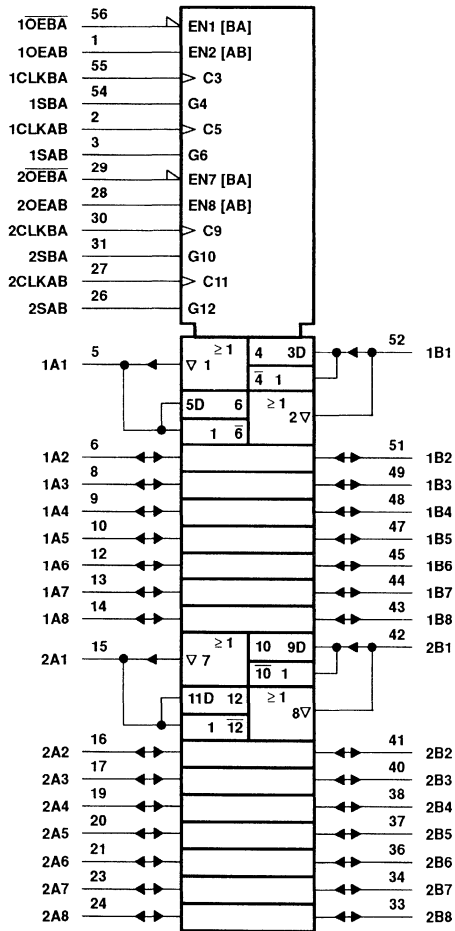
Figure 1. Bus-Management Functions

PRODUCT PREVIEW

SN54LVT16652, SN74LVT16652
3.3-V ABT 16-BIT BUS TRANSCEIVERS AND REGISTERS
WITH 3-STATE OUTPUTS

SCBS150 - MAY 1992 - REVISED JULY 1993

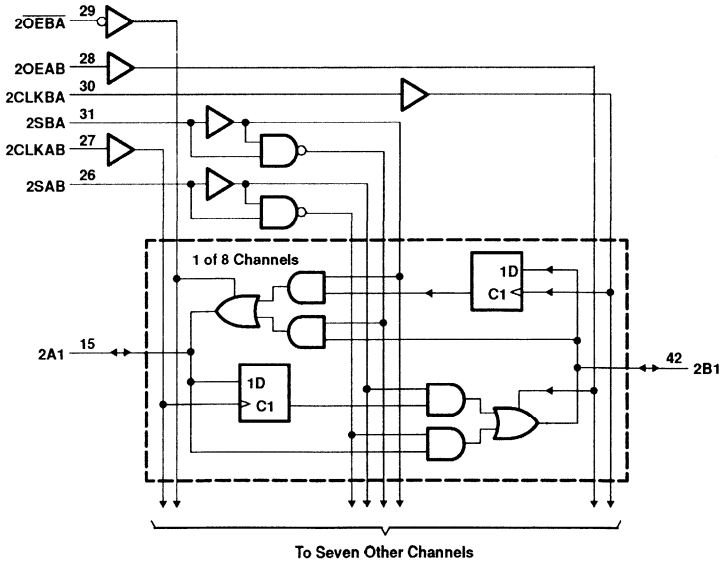
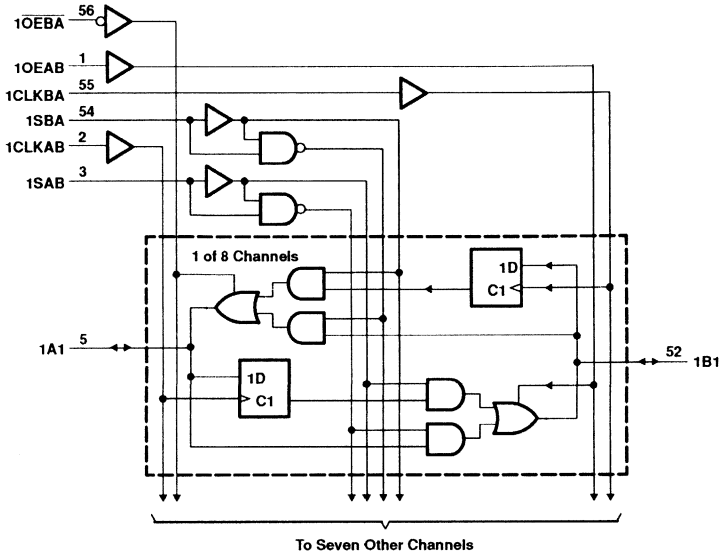
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

logic diagram (positive logic)



PRODUCT PREVIEW

SN54LVT16652, SN74LVT16652

3.3-V ABT 16-BIT BUS TRANSCEIVERS AND REGISTERS

WITH 3-STATE OUTPUTS

SCBS150 – MAY 1992 – REVISED JULY 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1)	-0.5 V to 7 V
Current into any output in the low state, I_O : SN54LVT16652	96 mA
SN74LVT16652	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT16652	48 mA
SN74LVT16652	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DGG package	1 W
DL package	1 W
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions

	SN54LVT16652		SN74LVT16652		UNIT
	MIN	MAX	MIN	MAX	
V_{CC} Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH} High-level input voltage	2		2		V
V_{IL} Low-level input voltage	0.8		0.8		V
V_I Input voltage	5.5		5.5		V
I_{OH} High-level output current	-24		-32		mA
I_{OL} Low-level output current	24		32		mA
I_{OL}^\ddagger Low-level output current	48		64		mA
$\Delta t/\Delta v$ Input transition rise or fall rate	Outputs enabled		10	10	ns/V
T_A Operating free-air temperature	-55	125	-40	85	°C

‡ Current duty cycle $\leq 50\%$, $f \geq 1$ kHz

PRODUCT PREVIEW



SN54LVT16652, SN74LVT16652
3.3-V ABT 16-BIT BUS TRANSCEIVERS AND REGISTERS
WITH 3-STATE OUTPUTS

SCBS150 – MAY 1992 – REVISED JULY 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54LVT16652		SN74LVT16652		UNIT
			MIN	MAX	MIN	MAX	
V_{IK}	$V_{CC} = 2.7\text{ V}$, $I_I = -18\text{ mA}$			-1.2		-1.2	V
V_{OH}	$V_{CC} = \text{MIN to MAX}^\ddagger$, $I_{OH} = -100\ \mu\text{A}$		$V_{CC} - 0.2$		$V_{CC} - 0.2$		V
	$V_{CC} = 2.7\text{ V}$, $I_{OH} = -8\text{ mA}$		2.4		2.4		
	$V_{CC} = 3\text{ V}$, $I_{OH} = -24\text{ mA}$		2				
	$V_{CC} = 3\text{ V}$, $I_{OH} = -32\text{ mA}$				2		
V_{OL}	$V_{CC} = 2.7\text{ V}$, $I_{OL} = 100\ \mu\text{A}$			0.2		0.2	V
	$V_{CC} = 2.7\text{ V}$, $I_{OL} = 24\text{ mA}$			0.5		0.5	
	$V_{CC} = 3\text{ V}$, $I_{OL} = 16\text{ mA}$			0.4		0.4	
	$V_{CC} = 3\text{ V}$, $I_{OL} = 32\text{ mA}$			0.5		0.5	
	$V_{CC} = 3\text{ V}$, $I_{OL} = 48\text{ mA}$			0.55			
	$V_{CC} = 3\text{ V}$, $I_{OL} = 64\text{ mA}$					0.55	
I_I	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}$ or GND		Control pins	± 1		± 1	μA
	$V_{CC} = 0$ or MAX^\ddagger , $V_I = 5.5\text{ V}$			10		10	
	$V_{CC} = 3.6\text{ V}$, $V_I = 5.5\text{ V}$		A or B ports §	20		20	
	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}$			5		5	
$V_{CC} = 3.6\text{ V}$, $V_I = 0$			-10		-10		
I_{off}	$V_{CC} = 0$, V_I or $V_O = 0$ to 4.5 V					± 100	μA
$I_I(\text{hold})$	$V_{CC} = 3\text{ V}$	$V_I = 0.8\text{ V}$	A or B ports	75		75	μA
		$V_I = 2\text{ V}$		-75		-75	
I_{OZH}	$V_{CC} = 3.6\text{ V}$, $V_O = 3\text{ V}$			1		1	μA
I_{OZL}	$V_{CC} = 3.6\text{ V}$, $V_O = 0.5\text{ V}$			-1		-1	μA
I_{CC}	$V_{CC} = 3.6\text{ V}$, $I_O = 0$, $V_I = V_{CC}$ or GND		Outputs high	0.1		0.1	mA
			Outputs low	5		5	
			Outputs disabled	0.1		0.1	
ΔI_{CC}^\P	$V_{CC} = 3\text{ V}$ to 3.6 V, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at V_{CC} or GND			0.2		0.2	mA
C_I	$V_I = 3\text{ V}$ or 0						pF
C_{IO}	$V_O = 3\text{ V}$ or 0						pF

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ Unused pins at V_{CC} or GND

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

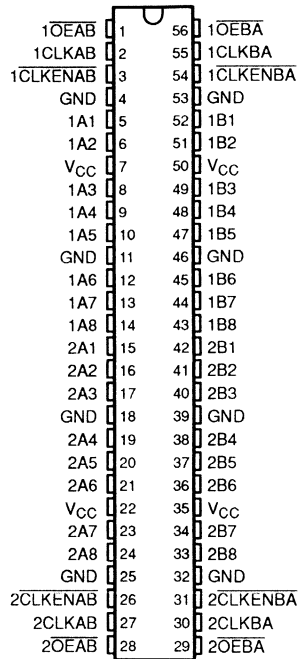
PRODUCT PREVIEW

SN54LVT16952, SN74LVT16952 3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS151 - MAY 1992 - REVISED JULY 1993

- **State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **Member of the Texas Instruments *Widebus*™ Family**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54LVT16952 . . . WD PACKAGE
SN74LVT16952 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The LVT16952 is a 16-bit registered transceiver designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. The device can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock (CLKAB or CLKBA) input provided that the clock-enable (CLKENAB or CLKENBA) input is low. Taking the output-enable (OEAB or OEBA) input low accesses the data on either port.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVT16952 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT16952 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVT16952 is characterized for operation from -40°C to 85°C .

Widebus is a trademark of Texas Instruments Incorporated.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



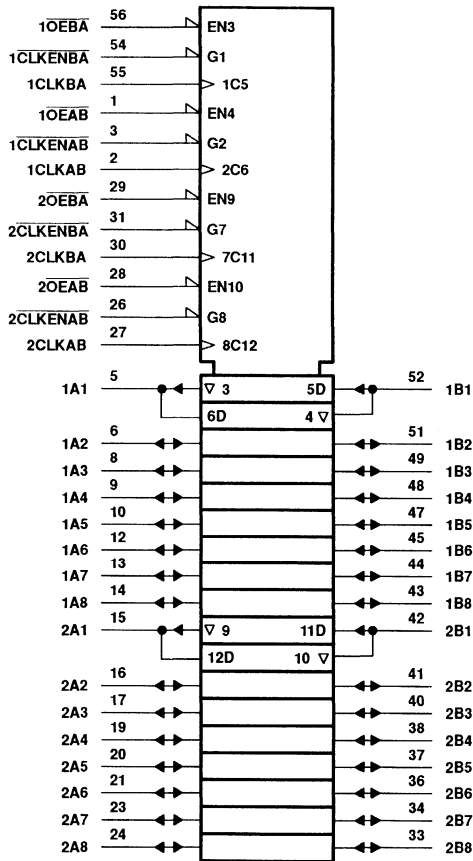
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PRODUCT PREVIEW

SN54LVT16952, SN74LVT16952
3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS
WITH 3-STATE OUTPUTS

SCBS151 - MAY 1992 - REVISED JULY 1993

logic symbol†

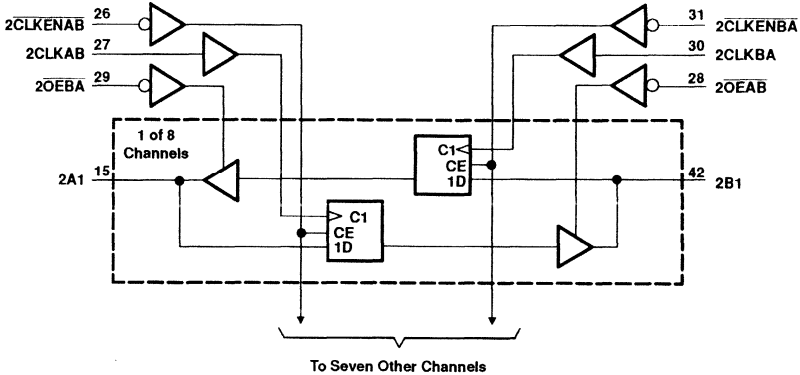
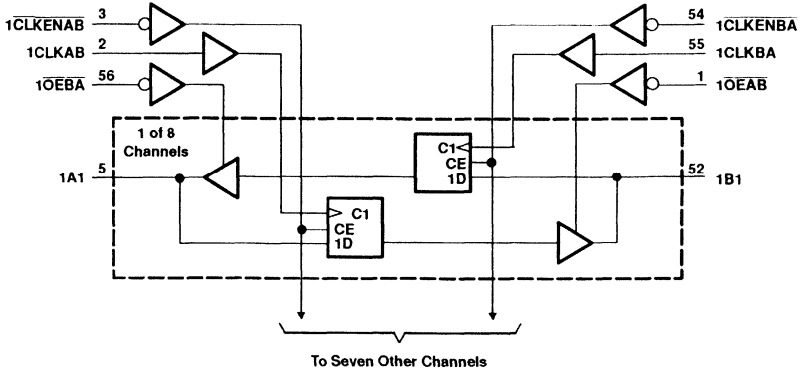


PRODUCT PREVIEW

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN54LVT16952, SN74LVT16952
3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS
WITH 3-STATE OUTPUTS
SCBS151 - MAY 1992 - REVISED JULY 1993

logic diagram (positive logic)



FUNCTION TABLE†

INPUTS				OUTPUT
CLKENAB	CLKAB	OEAB	A	B
H	X	L	X	B ₀ ‡
X	L	L	X	B ₀ ‡
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	Z

† A-to-B data flow is shown; B-to-A data flow is similar but uses CLKENBA, CLKBA, and OEBA.

‡ Level of B before the indicated steady-state input conditions were established.

PRODUCT PREVIEW

SN54LVT16952, SN74LVT16952
3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS
WITH 3-STATE OUTPUTS

SCBS151 – MAY 1992 – REVISED JULY 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Current into any output in the low state, I_{OL} : SN54LVT16952	96 mA
SN74LVT16952	128 mA
Current into any output in the high state, I_{OH} (see Note 2): SN54LVT16952	48 mA
SN74LVT16952	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DGG package	1 W
DL package	1 W
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions

		SN54LVT16952		SN74LVT16952		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage	0.8		0.8		V
V_I	Input voltage	5.5		5.5		V
I_{OH}	High-level output current	–24		–32		mA
I_{OL}	Low-level output current	24		32		mA
I_{OL}^\ddagger	Low-level output current	48		64		mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

‡ Current duty cycle $\leq 50\%$, $f \geq 1$ kHz

PRODUCT PREVIEW

SN54LVT16952, SN74LVT16952
3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS
WITH 3-STATE OUTPUTS

SCBS151 - MAY 1992 - REVISED JULY 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54LVT16952		SN74LVT16952		UNIT	
			MIN	MAX	MIN	MAX		
V_{IK}	$V_{CC} = 2.7\text{ V}$,	$I_I = -18\text{ mA}$		-1.2		-1.2	V	
V_{OH}	$V_{CC} = \text{MIN to MAX}^\dagger$,	$I_{OH} = -100\ \mu\text{A}$	$V_{CC} - 0.2$		$V_{CC} - 0.2$		V	
	$V_{CC} = 2.7\text{ V}$,	$I_{OH} = -8\text{ mA}$	2.4		2.4			
	$V_{CC} = 3\text{ V}$,	$I_{OH} = -24\text{ mA}$	2					
	$V_{CC} = 3\text{ V}$,	$I_{OH} = -32\text{ mA}$			2			
V_{OL}	$V_{CC} = 2.7\text{ V}$,	$I_{OL} = 100\ \mu\text{A}$		0.2		0.2	V	
	$V_{CC} = 2.7\text{ V}$,	$I_{OL} = 24\text{ mA}$		0.5		0.5		
	$V_{CC} = 3\text{ V}$,	$I_{OL} = 16\text{ mA}$		0.4		0.4		
	$V_{CC} = 3\text{ V}$,	$I_{OL} = 32\text{ mA}$		0.5		0.5		
	$V_{CC} = 3\text{ V}$,	$I_{OL} = 48\text{ mA}$		0.55				
	$V_{CC} = 3\text{ V}$,	$I_{OL} = 64\text{ mA}$				0.55		
I_I	$V_{CC} = 3.6\text{ V}$,	$V_I = V_{CC}$ or GND	Control pins	± 1		± 1	μA	
	$V_{CC} = 0$ or MAX^\ddagger ,	$V_I = 5.5\text{ V}$		10		10		
	$V_{CC} = 3.6\text{ V}$,	$V_I = 5.5\text{ V}$	A or B ports §	20		20		
	$V_{CC} = 3.6\text{ V}$,	$V_I = V_{CC}$		5		5		
	$V_{CC} = 3.6\text{ V}$,	$V_I = 0$		-10		-10		
I_{off}	$V_{CC} = 0$,	V_I or $V_O = 0$ to 4.5 V				± 100	μA	
$I_I(\text{hold})$	$V_{CC} = 3\text{ V}$	$V_I = 0.8\text{ V}$	A or B ports	75		75	μA	
		$V_I = 2\text{ V}$		-75		-75		
I_{OZH}	$V_{CC} = 3.6\text{ V}$,	$V_O = 3\text{ V}$		1		1	μA	
I_{OZL}	$V_{CC} = 3.6\text{ V}$,	$V_O = 0.5\text{ V}$		-1		-1	μA	
I_{CC}	$V_{CC} = 3.6\text{ V}$,	$V_I = V_{CC}$ or GND	$I_O = 0$,	Outputs high		0.1	0.1	mA
				Outputs low		5	5	
				Outputs disabled		0.1	0.1	
						0.1	0.1	
ΔI_{CC}^\P	$V_{CC} = 3\text{ V}$ to 3.6 V,	One input at $V_{CC} - 0.6\text{ V}$,		0.2		0.2	mA	
C_i	$V_I = 3\text{ V}$ or 0						pF	
C_{i0}	$V_O = 3\text{ V}$ or 0						pF	

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ Unused pins at V_{CC} or GND

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

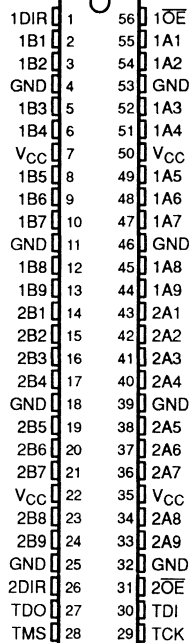


SN54LVT18245, SN74LVT18245
3.3-V ABT SCAN TEST DEVICES
WITH 18-BIT BUS TRANSCEIVERS

SCBS161 – AUGUST 1993

- Members of the Texas Instruments **SCOPE™** Family of Testability Products
- Members of the Texas Instruments **Widebus™** Family
- State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- **SCOPE™** Instruction Set
 - IEEE Standard 1149.1-1990 Required Instructions and P1149.1A CLAMP and HIGHZ
 - Parallel Signature Analysis at Inputs
 - Pseudo-Random Pattern Generation From Outputs
 - Sample Inputs/Toggle Outputs
 - Binary Count From Outputs
 - Device Identification
 - Even-Parity Opcodes
- Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings

SN54LVT18245 . . . WD PACKAGE
 SN74LVT18245 . . . DGG OR DL PACKAGE
 (TOP VIEW)



PRODUCT PREVIEW

description

The SN54LVT18245 and SN74LVT18245 scan test devices with 18-bit bus transceivers are members of the Texas Instruments SCOPE™ testability IC family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

Additionally, these devices are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

In the normal mode, these devices are 18-bit noninverting bus transceivers. They can be used either as two 9-bit transceivers or one 18-bit transceiver. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE™ bus transceivers.

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SN54LVT18245, SN74LVT18245
3.3-V ABT SCAN TEST DEVICES
WITH 18-BIT BUS TRANSCEIVERS

SCBS161 – AUGUST 1993

description (continued)

Data flow is controlled by the direction-control (DIR) and output-enable (\overline{OE}) inputs. Data transmission is allowed from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at DIR. The output-enable (\overline{OE}) can be used to disable the device so that the buses are effectively isolated.

In the test mode, the normal operation of the SCOPE™ bus transceivers is inhibited and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry can perform boundary scan test operations according to the protocol described in IEEE Standard 1149.1-1990.

Four dedicated test pins are used to observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVT18245 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

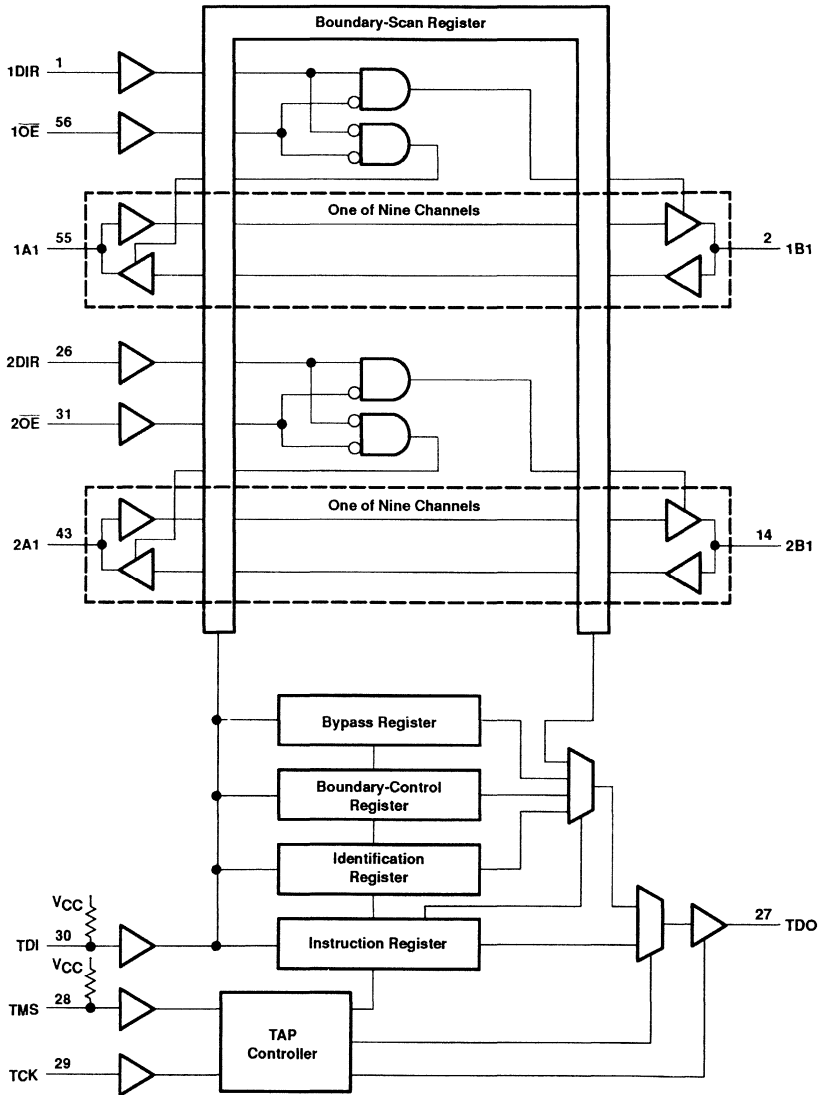
The SN54LVT18245 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVT18245 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(normal mode, each 9-bit section)

INPUTS		OPERATION
\overline{OE}	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

PRODUCT PREVIEW

functional block diagram



PRODUCT PREVIEW

SN54LVT18245, SN74LVT18245
3.3-V ABT SCAN TEST DEVICES
WITH 18-BIT BUS TRANSCEIVERS

SCBS161 – AUGUST 1993

Terminal Functions

PIN NAME	DESCRIPTION
GND	Ground
TCK	Test clock. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to the test clock. Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK.
TDI	Test data input. One of four terminals required by IEEE Standard 1149.1-1990. The test data input is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected.
TDO	Test data output. One of four terminals required by IEEE Standard 1149.1-1990. The test data output is the serial output for shifting data through the instruction register or selected data register.
TMS	Test mode select. One of four terminals required by IEEE Standard 1149.1-1990. The test mode select input directs the device through its test access port (TAP) controller states. An internal pullup forces TMS to a high level if left unconnected.
VCC	Supply voltage
1A1–1A9, 2A1–2A9	Normal-function A-bus I/O ports. See function table for normal-mode logic.
1B1–1B9, 2B1–2B9	Normal-function B-bus I/O ports. See function table for normal-mode logic.
1DIR, 2DIR	Normal-function direction controls. See function table for normal-mode logic.
1OE, 2OE	Normal-function output enables. See function table for normal-mode logic.

PRODUCT PREVIEW



SN54LVT18245, SN74LVT18245
3.3-V ABT SCAN TEST DEVICES
WITH 18-BIT BUS TRANSCEIVERS

SCBS161 – AUGUST 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Current into any output in the low state, I_O : SN54LVT18245	96 mA
SN74LVT18245	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT18245	48 mA
SN74LVT18245	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DGG package	1 W
DL package	0.95 W
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative voltage ratings can be exceeded if the input and output clamp-current ratings are observed.
 2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions

		SN54LVT18245		SN74LVT18245		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage	0.8		0.8		V
V_I	Input voltage	5.5		5.5		V
I_{OH}	High-level output current	–24		–32		mA
I_{OL}	Low-level output current	24		32		mA
I_{OL}^\ddagger	Low-level output current	48		64		mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

‡ Current duty cycle $\leq 50\%$, $f \geq 1$ kHz

PRODUCT PREVIEW

SN54LVT18245, SN74LVT18245
3.3-V ABT SCAN TEST DEVICES
WITH 18-BIT BUS TRANSCEIVERS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 3)

PARAMETER	TEST CONDITIONS		SN54LVT18245		SN74LVT18245		UNIT		
			MIN	TYP†	MAX	MIN		TYP†	MAX
V_{IK}	$V_{CC} = 2.7\text{ V}$,	$I_I = -18\text{ mA}$			-1.2		-1.2	V	
V_{OH}	$V_{CC} = \text{MIN to MAX}^\ddagger$, $I_{OH} = -100\ \mu\text{A}$		$V_{CC} - 0.2$		$V_{CC} - 0.2$			V	
	$V_{CC} = 2.7\text{ V}$,	$I_{OH} = -8\text{ mA}$	2.4		2.4				
	$V_{CC} = 3\text{ V}$,	$I_{OH} = -24\text{ mA}$	2						
	$V_{CC} = 3\text{ V}$,	$I_{OH} = -32\text{ mA}$			2				
V_{OL}	$V_{CC} = 2.7\text{ V}$,	$I_{OL} = 100\ \mu\text{A}$			0.2		0.2	V	
	$V_{CC} = 2.7\text{ V}$,	$I_{OL} = 24\text{ mA}$			0.5		0.5		
	$V_{CC} = 3\text{ V}$,	$I_{OL} = 16\text{ mA}$			0.4		0.4		
	$V_{CC} = 3\text{ V}$,	$I_{OL} = 32\text{ mA}$			0.5		0.5		
	$V_{CC} = 3\text{ V}$,	$I_{OL} = 48\text{ mA}$			0.55				
	$V_{CC} = 3\text{ V}$,	$I_{OL} = 64\text{ mA}$					0.55		
I_I	$V_{CC} = 3.6\text{ V}$,	$V_I = V_{CC}$ or GND	DIR, OE, TCK		± 1		± 1	μA	
	$V_{CC} = 0$ or MAX^\ddagger ,	$V_I = 5.5\text{ V}$			10		10		
	$V_{CC} = 3.6\text{ V}$,	$V_I = 5.5\text{ V}$	TDI, TMS		50		50		
	$V_{CC} = 3.6\text{ V}$,	$V_I = V_{CC}$			1		1		
	$V_{CC} = 3.6\text{ V}$,	$V_I = 0$	A or B ports§		-100		-100		
	$V_{CC} = 3.6\text{ V}$,	$V_I = 5.5\text{ V}$			20		20		
	$V_{CC} = 3.6\text{ V}$,	$V_I = V_{CC}$			1		1		
	$V_{CC} = 3.6\text{ V}$,	$V_I = 0$			-5		-5		
I_{off}	$V_{CC} = 0$,	V_I or $V_O = 0$ to 4.5 V					± 100	μA	
$I_I(\text{hold})$	$V_{CC} = 3\text{ V}$	$V_I = 0.8\text{ V}$	A or B ports		75		75	μA	
		$V_I = 2\text{ V}$			-75		-75		
I_{OZH}	$V_{CC} = 3.6\text{ V}$,	$V_O = 3\text{ V}$			1		1	μA	
I_{OZL}	$V_{CC} = 3.6\text{ V}$,	$V_O = 0.5\text{ V}$			-1		-1	μA	
I_{CC}	$V_{CC} = 3.6\text{ V}$,	$V_I = V_{CC}$ or GND	$I_O = 0$,	Outputs high			2	2	mA
				Outputs low			15	15	
				Outputs disabled			2	2	
ΔI_{CC}^\ddagger	$V_{CC} = 3\text{ V}$ to 3.6 V, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at V_{CC} or GND				0.2		0.2	mA	
C_I	$V_I = 3\text{ V}$ or 0				4		4	pF	
C_{iO}	$V_O = 3\text{ V}$ or 0				11		11	pF	
C_O	$V_O = 3\text{ V}$ or 0				8		8	pF	

NOTE 3: Product preview specifications are design goals only and are subject to change without notice.

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ Unused pins at V_{CC} or GND

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW



SN54LVT18245, SN74LVT18245
3.3-V ABT SCAN TEST DEVICES
WITH 18-BIT BUS TRANSCEIVERS
SCBS161 – AUGUST 1993

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Note 3 and Figure 1)

			SN54LVT18245				SN74LVT18245				UNIT
			$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	TCK					0	50			MHz
t_w	Pulse duration	TCK high or low					8.1				ns
t_{su}	Setup time	A, B, DIR, or $\overline{\text{OE}}$ before TCK \uparrow					7				ns
		TDI before TCK \uparrow					4.5				
		TMS before TCK \uparrow					3.6				
t_h	Hold time	A, B, DIR, or $\overline{\text{OE}}$ after TCK \uparrow					0				ns
		TDI after TCK \uparrow					0				
		TMS after TCK \uparrow					0.5				
t_d	Delay time	Power up to TCK \uparrow					50				ns
t_r	Rise time	V_{CC} power up					1				μs

NOTE 3: Product preview specifications are design goals only and are subject to change without notice.

PRODUCT PREVIEW

SN54LVT18245, SN74LVT18245
3.3-V ABT SCAN TEST DEVICES
WITH 18-BIT BUS TRANSCEIVERS

SCBS161 – AUGUST 1993

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Note 3 and Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT18245		SN74LVT18245		UNIT	
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		
			MIN	MAX	MAX	MIN		MAX
t_{PLH}	A or B	B or A				1.5	4.8	ns
t_{PHL}						1.5	5.4	
t_{PZH}	\overline{OE}	B or A				3	8.5	ns
t_{PZL}						3	9	
t_{PHZ}	\overline{OE}	B or A				3	9.5	ns
t_{PLZ}						3	9.5	

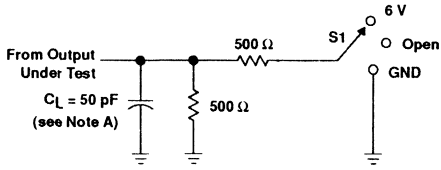
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Note 3 and Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT18245		SN74LVT18245		UNIT	
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		
			MIN	MAX	MAX	MIN		MAX
f_{max}	TCK↓					50		MHz
t_{PLH}	TCK↓	A or B				3	13.1	ns
t_{PHL}						3	12.8	
t_{PLH}	TCK↓	TDO				2	6.1	ns
t_{PHL}						2	6.5	
t_{PZH}	TCK↓	A or B				4	13.4	ns
t_{PZL}						4	13.6	
t_{PZH}	TCK↓	TDO				2	6.6	ns
t_{PZL}						2.5	6.9	
t_{PHZ}	TCK↓	A or B				3.5	13.6	ns
t_{PLZ}						2.5	12.7	
t_{PHZ}	TCK↓	TDO				2	7.2	ns
t_{PLZ}						1.5	6.3	

NOTE 3: Product preview specifications are design goals only and are subject to change without notice.

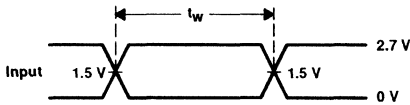
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

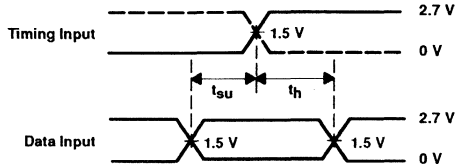


LOAD CIRCUIT FOR OUTPUTS

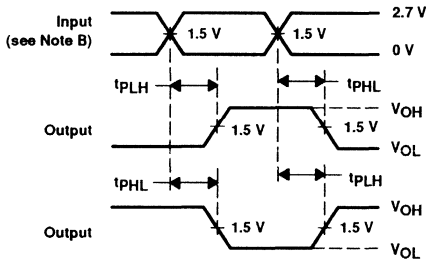
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



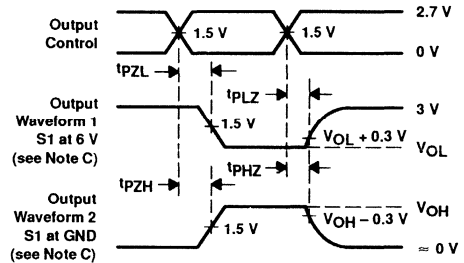
VOLTAGE WAVEFORMS
 PULSE DURATION



VOLTAGE WAVEFORMS
 SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
 PROPAGATION DELAY TIMES
 INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
 ENABLE AND DISABLE TIMES
 LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

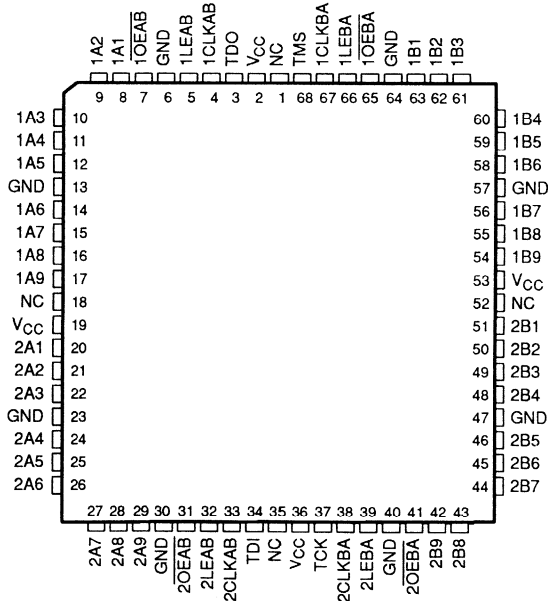


SN54LVT18502, SN74LVT18502 3.3-V ABT SCAN TEST DEVICES WITH 18-BIT UNIVERSAL BUS TRANSCEIVERS

SCBS162 – AUGUST 1993

- Members of the Texas Instruments *SCOPE™* Family of Testability Products
- Members of the Texas Instruments *Widebus™* Family
- State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- *UBT™* (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- *SCOPE™* Instruction Set
 - IEEE Standard 1149.1-1990 Required Instructions and P1149.1A CLAMP and HIGHZ
 - Parallel Signature Analysis at Inputs
 - Pseudo-Random Pattern Generation From Outputs
 - Sample Inputs/Toggle Outputs
 - Binary Count From Outputs
 - Device Identification
 - Even-Parity OpCodes
- Packaged in 64-Pin Plastic Thin Quad Flat Packages Using 0.5-mm Center-to-Center Spacings and 68-Pin Ceramic Quad Flat Packages Using 25-mil Center-to-Center Spacings

SN54LVT18502 . . . HV PACKAGE
(TOP VIEW)



NC – No internal connection

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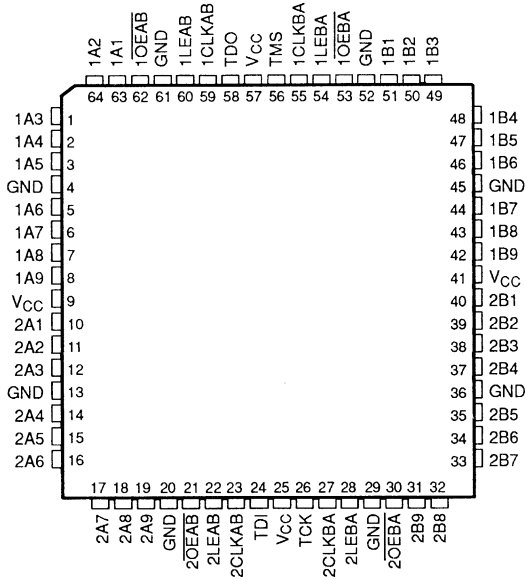
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PRODUCT PREVIEW

SN54LVT18502, SN74LVT18502
3.3-V ABT SCAN TEST DEVICES WITH
18-BIT UNIVERSAL BUS TRANSCEIVERS

SCBS162 – AUGUST 1993

SN74LVT18502 . . . PM PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

The SN54LVT18502 and SN74LVT18502 scan test devices with 18-bit universal bus transceivers are members of the Texas Instruments SCOPE™ testability IC family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

Additionally, these devices are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

In the normal mode, these devices are 18-bit universal bus transceivers that combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, or clocked modes. They can be used either as two 9-bit transceivers or one 18-bit transceiver. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE™ universal bus transceivers.

Data flow in each direction is controlled by output-enable (\overline{OEAB} and \overline{OEBA}), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A-bus data is latched while CLKAB is held at a static low or high logic level. Otherwise, if LEAB is low, A-bus data is stored on a low-to-high transition of CLKAB. When \overline{OEAB} is low, the B outputs are active. When \overline{OEAB} is high, the B outputs are in the high-impedance state. B-to-A data flow is similar to A-to-B data flow but uses the OEBA, LEBA, and CLKBA inputs.



description (continued)

In the test mode, the normal operation of the SCOPE™ universal bus transceivers is inhibited and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry performs boundary scan test operations according to the protocol described in IEEE Standard 1149.1-1990.

Four dedicated test pins are used to observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54LVT18502 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT18502 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE†
(normal mode, each register)

INPUTS				OUTPUT
OEAB	LEAB	CLKAB	A	B
L	L	L	X	B ₀ ‡
L	L	↑	L	L
L	L	↑	H	H
L	H	X	L	L
L	H	X	H	H
H	X	X	X	Z

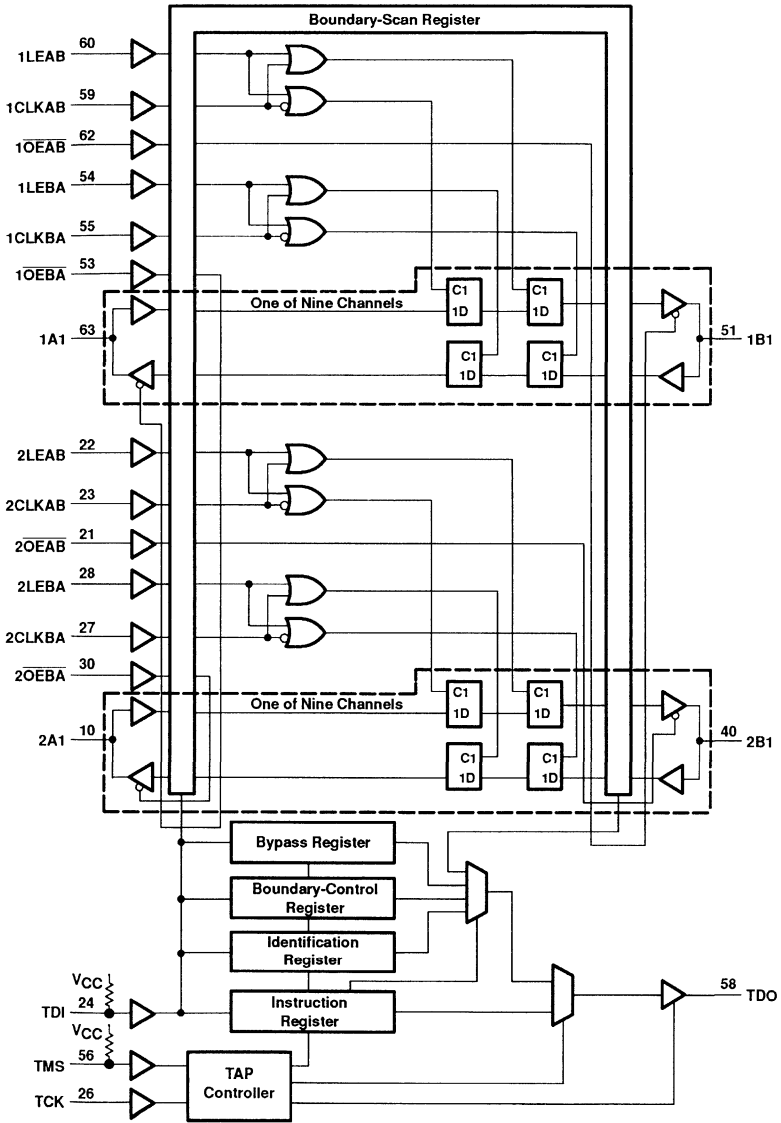
† A-to-B data flow is shown. B-to-A data flow is similar but uses OEBA, LEBA, and CLKBA.

‡ Output level before the indicated steady-state input conditions were established.

SN54LVT18502, SN74LVT18502
3.3-V ABT SCAN TEST DEVICES WITH
18-BIT UNIVERSAL BUS TRANSCEIVERS

SCBS162 – AUGUST 1993

functional block diagram



Pin numbers shown are for the PM package.

PRODUCT PREVIEW



SN54LVT18502, SN74LVT18502
3.3-V ABT SCAN TEST DEVICES WITH
18-BIT UNIVERSAL BUS TRANSCEIVERS

SCBS162 – AUGUST 1993

Terminal Functions

PIN NAME	DESCRIPTION
GND	Ground
TCK	Test clock. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to the test clock. Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK.
TDI	Test data input. One of four terminals required by IEEE Standard 1149.1-1990. The test data input is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected.
TDO	Test data output. One of four terminals required by IEEE Standard 1149.1-1990. The test data output is the serial output for shifting data through the instruction register or selected data register.
TMS	Test mode select. One of four terminals required by IEEE Standard 1149.1-1990. The test mode select input directs the device through its test access port (TAP) controller states. An internal pullup forces TMS to a high level if left unconnected.
V _{CC}	Supply voltage
1A1–1A9, 2A1–2A9	Normal-function A-bus I/O ports. See function table for normal-mode logic.
1B1–1B9, 2B1–2B9	Normal-function B-bus I/O ports. See function table for normal-mode logic.
1CLKAB, 1CLKBA, 2CLKAB, 2CLKBA	Normal-function clock inputs. See function table for normal-mode logic.
1LEAB, 1LEBA, 2LEAB, 2LEBA	Normal-function latch enables. See function table for normal-mode logic.
1OEAB, 1OEBA, 2OEAB, 2OEBA	Normal-function output enables. See function table for normal-mode logic.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1)	-0.5 V to 7 V
Current into any output in the low state, I_{OL} : SN54LVT18502	96 mA
SN74LVT18502	128 mA
Current into any output in the high state, I_{OH} (see Note 2): SN54LVT18502	48 mA
SN74LVT18502	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): PM package	885 mW
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings can be exceeded if the input and output clamp-current ratings are observed.
 2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions

		SN54LVT18502		SN74LVT18502		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage	0.8		0.8		V
V_I	Input voltage	5.5		5.5		V
I_{OH}	High-level output current	-24		-32		mA
I_{OL}	Low-level output current	24		32		mA
I_{OL}^\ddagger	Low-level output current	48		64		mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
T_A	Operating free-air temperature	-55	125	-40	85	°C

‡ Current duty cycle $\leq 50\%$, $f \geq 1$ kHz

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SN54LVT18502, SN74LVT18502
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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 3)

PARAMETER	TEST CONDITIONS		SN54LVT18502		SN74LVT18502		UNIT
			MIN	TYP†	MAX	MIN	
V_{IK}	$V_{CC} = 2.7\text{ V}$, $I_I = -18\text{ mA}$				-1.2		V
V_{OH}	$V_{CC} = \text{MIN to MAX}^\ddagger$, $I_{OH} = -100\ \mu\text{A}$		$V_{CC} - 0.2$		$V_{CC} - 0.2$		V
	$V_{CC} = 2.7\text{ V}$, $I_{OH} = -8\text{ mA}$		2.4		2.4		
	$V_{CC} = 3\text{ V}$, $I_{OH} = -24\text{ mA}$		2				
	$V_{CC} = 3\text{ V}$, $I_{OH} = -32\text{ mA}$				2		
V_{OL}	$V_{CC} = 2.7\text{ V}$, $I_{OL} = 100\ \mu\text{A}$		0.2		0.2		V
	$V_{CC} = 2.7\text{ V}$, $I_{OL} = 24\text{ mA}$		0.5		0.5		
	$V_{CC} = 3\text{ V}$, $I_{OL} = 16\text{ mA}$		0.4		0.4		
	$V_{CC} = 3\text{ V}$, $I_{OL} = 32\text{ mA}$		0.5		0.5		
	$V_{CC} = 3\text{ V}$, $I_{OL} = 48\text{ mA}$		0.55				
	$V_{CC} = 3\text{ V}$, $I_{OL} = 64\text{ mA}$				0.55		
I_I	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}$ or GND		CLK, LE, OE, TCK		± 1		μA
	$V_{CC} = 0$ or MAX ‡ , $V_I = 5.5\text{ V}$				10		
	$V_{CC} = 3.6\text{ V}$, $V_I = 5.5\text{ V}$				50		
	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}$		TDI, TMS		1		
	$V_{CC} = 3.6\text{ V}$, $V_I = 0$				-100		
	$V_{CC} = 3.6\text{ V}$, $V_I = 5.5\text{ V}$				20		
	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}$		A or B ports §		1		
	$V_{CC} = 3.6\text{ V}$, $V_I = 0$				-5		
I_{off}	$V_{CC} = 0$, V_I or $V_O = 0$ to 4.5 V				± 100		μA
$I_I(\text{hold})$	$V_{CC} = 3\text{ V}$	$V_I = 0.8\text{ V}$	A or B ports		75	75	μA
		$V_I = 2\text{ V}$			-75	-75	μA
I_{OZH}	$V_{CC} = 3.6\text{ V}$	$V_O = 3\text{ V}$			1	1	μA
I_{OZL}	$V_{CC} = 3.6\text{ V}$	$V_O = 0.5\text{ V}$			-1	-1	μA
I_{CC}	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}$ or GND	$I_O = 0$.	Outputs high		2	2	mA
			Outputs low		15	15	
			Outputs disabled		2	2	
ΔI_{CC}^\ddagger	$V_{CC} = 3\text{ V}$ to 3.6 V, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at V_{CC} or GND				0.2	0.2	mA
C_i	$V_I = 3\text{ V}$ or 0				4	4	pF
C_{iO}	$V_O = 3\text{ V}$ or 0				11	11	pF
C_O	$V_O = 3\text{ V}$ or 0				8	8	pF

NOTE 3: Product preview specifications are design goals only and are subject to change without notice.

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ Unused pins at V_{CC} or GND

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Note 3 and Figure 1)

			SN54LVT18502				SN74LVT18502				UNIT
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	CLKAB or CLKBA				0	100			MHz	
t_w	Pulse duration	CLKAB or CLKBA high or low				3.5				ns	
		LEAB or LEBA high				3.5					
t_{su}	Setup time	A before CLKAB \uparrow or B before CLKBA \uparrow				4				ns	
		A before LEAB \downarrow or B before LEBA \downarrow	CLK high			3.5					
			CLK low			2					
t_h	Hold time	A after CLKAB \uparrow or B after CLKBA \uparrow				0				ns	
		A after LEAB \downarrow or B after LEBA \downarrow				2					

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Note 3 and Figure 1)

			SN54LVT18502				SN74LVT18502				UNIT
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	TCK				0	50			MHz	
t_w	Pulse duration	TCK high or low				8				ns	
t_{su}	Setup time	A, B, CLK, LE, or $\overline{\text{OE}}$ before TCK \uparrow				4.5				ns	
		TDI before TCK \uparrow				7.5					
		TMS before TCK \uparrow				3					
t_h	Hold time	A, B, CLK, LE, or $\overline{\text{OE}}$ after TCK \uparrow				0.5				ns	
		TDI after TCK \uparrow				0.5					
		TMS after TCK \uparrow				0.5					
t_d	Delay time	Power up to TCK \uparrow				50				ns	
t_r	Rise time	V_{CC} power up				1				μs	

NOTE 3: Product preview specifications are design goals only and are subject to change without notice.

PRODUCT PREVIEW



SN54LVT18502, SN74LVT18502
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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Note 3 and Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT18502		SN74LVT18502			UNIT	
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			$V_{CC} = 2.7\text{ V}$
			MIN	MAX	MAX	MIN	MAX		MAX
f_{max}	CLKAB or CLKBA					100		MHz	
t_{PLH}	A or B	B or A				2	6	ns	
t_{PHL}						2	6		
t_{PLH}	CLKAB or CLKBA	B or A				2.5	6	ns	
t_{PHL}						2.5	6		
t_{PLH}	LEAB or LEBA	B or A				2.5	7	ns	
t_{PHL}						2.5	7		
t_{PZH}	\overline{OEAB} or \overline{OEBA}	B or A				2	7	ns	
t_{PZL}						2.5	8		
t_{PHZ}	\overline{OEAB} or \overline{OEBA}	B or A				3	8.8	ns	
t_{PLZ}						2.5	7.3		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Note 3 and Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT18502		SN74LVT18502			UNIT	
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			$V_{CC} = 2.7\text{ V}$
			MIN	MAX	MAX	MIN	MAX		MAX
f_{max}	TCK					50		MHz	
t_{PLH}	TCK↓	A or B				2.5	13.5	ns	
t_{PHL}						2.5	12.4		
t_{PLH}	TCK↓	TDO				2	5.6	ns	
t_{PHL}						2	6		
t_{PZH}	TCK↓	A or B				4.5	13.4	ns	
t_{PZL}						5	14		
t_{PZH}	TCK↓	TDO				2.5	6.8	ns	
t_{PZL}						3	7.5		
t_{PHZ}	TCK↓	A or B				4	16.3	ns	
t_{PLZ}						3.5	15.3		
t_{PHZ}	TCK↓	TDO				3	7.6	ns	
t_{PLZ}						3	7.6		

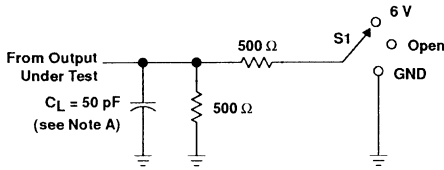
NOTE 3: Product preview specifications are design goals only and are subject to change without notice.

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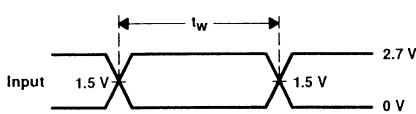
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PARAMETER MEASUREMENT INFORMATION

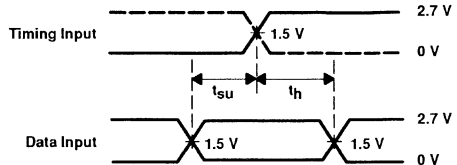


LOAD CIRCUIT FOR OUTPUTS

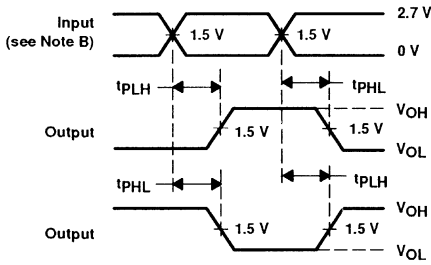
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



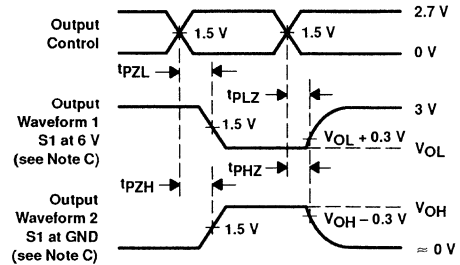
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

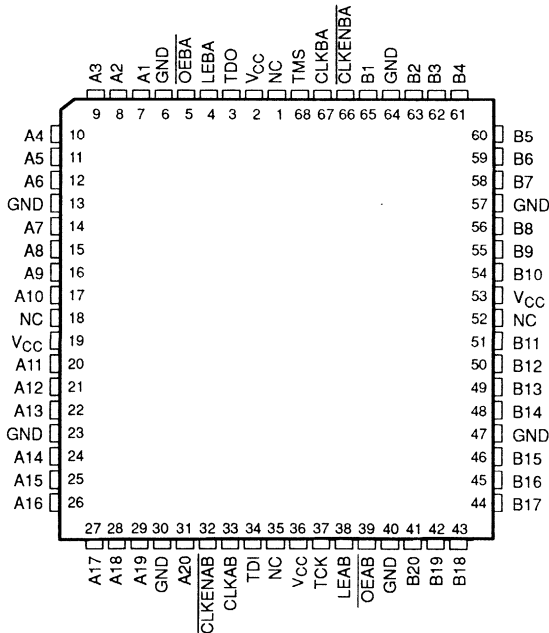
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SN54LVT18504, SN74LVT18504
3.3-V ABT SCAN TEST DEVICES WITH
20-BIT UNIVERSAL BUS TRANSCEIVERS

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- Members of the Texas Instruments **SCOPE™** Family of Testability Products
- Members of the Texas Instruments **Widebus™** Family
- State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- **UBT™** (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- **SCOPE™** Instruction Set
 - IEEE Standard 1149.1-1990 Required Instructions and P1149.1A CLAMP and HIGHZ
 - Parallel Signature Analysis at Inputs
 - Pseudo-Random Pattern Generation From Outputs
 - Sample Inputs/Toggle Outputs
 - Binary Count From Outputs
 - Device Identification
 - Even-Parity Opcodes
- Packaged in 64-Pin Plastic Thin Quad Flat Packages Using 0.5-mm Center-to-Center Spacings and 68-Pin Ceramic Quad Flat Packages Using 25-mil Center-to-Center Spacings

SN54LVT18504 . . . HV PACKAGE
(TOP VIEW)



NC – No internal connection

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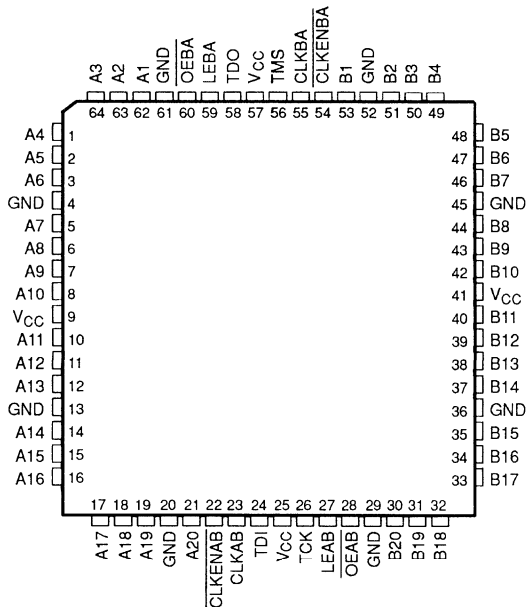
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SN74LVT18504 . . . PM PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

The SN54LVT18504 and SN74LVT18504 scan test devices with 20-bit universal bus transceivers are members of the Texas Instruments SCOPE™ testability IC family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

Additionally, these devices are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

In the normal mode, these devices are 20-bit universal bus transceivers that combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, or clocked modes. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE™ universal bus transceivers.

Data flow in each direction is controlled by output-enable (\overline{OEAB} and \overline{OEBA}), latch-enable (LEAB and LEBA), clock-enable ($\overline{CLKENAB}$ and $\overline{CLKENBA}$), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A-bus data is latched while $\overline{CLKENAB}$ is high and/or CLKAB is held at a static low or high logic level. Otherwise, if LEAB is low and $\overline{CLKENAB}$ is low, A-bus data is stored on a low-to-high transition of CLKAB. When \overline{OEAB} is low, the B outputs are active. When \overline{OEAB} is high, the B outputs are in the high-impedance state. B-to-A data flow is similar to A-to-B data flow but uses the \overline{OEBA} , LEBA, $\overline{CLKENBA}$, and CLKBA inputs.



description (continued)

In the test mode, the normal operation of the SCOPE™ universal bus transceivers is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled the test circuitry performs boundary scan test operations according to the protocol described in IEEE Standard 1149.1-1990.

Four dedicated test pins are used to observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54LVT18504 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT18504 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE†
 (normal mode, each register)

INPUTS					OUTPUT
OEAB	LEAB	CLKENAB	CLKAB	A	B
L	L	L	L	X	B ₀ ‡
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	H	X	X	B ₀ ‡
L	H	X	X	L	L
L	H	X	X	H	H
H	X	X	X	X	Z

† A-to-B data flow is shown. B-to-A data flow is similar but uses OEBA, LEBA, CLKENBA, and CLKBA.

‡ Output level before the indicated steady-state input conditions were established.

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Terminal Functions

PIN NAME	DESCRIPTION
A1 – A20	Normal-function A-bus I/O ports. See function table for normal-mode logic.
B1 – B20	Normal-function B-bus I/O ports. See function table for normal-mode logic.
CLKAB, CLKBA	Normal-function clock inputs. See function table for normal-mode logic.
CLKENAB, CLKENBA	Normal-function clock enables. See function table for normal-mode logic.
GND	Ground
LEAB, LEBA	Normal-function latch enables. See function table for normal-mode logic.
OEAB, OEBA	Normal-function output enables. See function table for normal-mode logic.
TCK	Test clock. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to the test clock. Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK.
TDI	Test data input. One of four terminals required by IEEE Standard 1149.1-1990. The test data input is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected.
TDO	Test data output. One of four terminals required by IEEE Standard 1149.1-1990. The test data output is the serial output for shifting data through the instruction register or selected data register.
TMS	Test mode select. One of four terminals required by IEEE Standard 1149.1-1990. The test mode select input directs the device through its test access port (TAP) controller states. An internal pullup forces TMS to a high level if left unconnected.
V _{CC}	Supply voltage

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1)	-0.5 V to 7 V
Current into any output in the low state, I_O : SN54LVT18504	96 mA
SN74LVT18504	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT18504	48 mA
SN74LVT18504	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): PM package	885 mW
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative voltage ratings can be exceeded if the input and output clamp current ratings are observed.
 2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions

		SN54LVT18504		SN74LVT18504		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage	0.8		0.8		V
V_I	Input voltage	5.5		5.5		V
I_{OH}	High-level output current	-24		-32		mA
I_{OL}	Low-level output current	24		32		mA
I_{OL}^\ddagger	Low-level output current	48		64		mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		ns/V
T_A	Operating free-air temperature	-55	125	-40	85	°C

‡ Current duty cycle $\leq 50\%$, $f \geq 1$ kHz

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 3)

PARAMETER	TEST CONDITIONS		SN54LVT18504			SN74LVT18504			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}	V _{CC} = 2.7 V, I _I = -18 mA		-1.2			-1.2			V
V _{OH}	V _{CC} = MIN to MAX‡, I _{OH} = -100 µA		V _{CC} - 0.2			V _{CC} - 0.2			V
	V _{CC} = 2.7 V, I _{OH} = -8 mA		2.4			2.4			
	V _{CC} = 3 V, I _{OH} = -24 mA		2						
	V _{CC} = 3 V, I _{OH} = -32 mA					2			
V _{OL}	V _{CC} = 2.7 V, I _{OL} = 100 µA		0.2			0.2			V
	V _{CC} = 2.7 V, I _{OL} = 24 mA		0.5			0.5			
	V _{CC} = 3 V, I _{OL} = 16 mA		0.4			0.4			
	V _{CC} = 3 V, I _{OL} = 32 mA		0.5			0.5			
	V _{CC} = 3 V, I _{OL} = 48 mA		0.55						
	V _{CC} = 3 V, I _{OL} = 64 mA					0.55			
I _I	V _{CC} = 3.6 V, V _I = V _{CC} or GND		CLK, CLKEN, LE, OE, TCK		±1			±1	
	V _{CC} = 0 or MAX‡, V _I = 5.5 V				10			10	
	V _{CC} = 3.6 V, V _I = 5.5 V				50			50	
	V _{CC} = 3.6 V, V _I = V _{CC}		TDI, TMS		1			1	
	V _{CC} = 3.6 V, V _I = 0				-100			-100	
	V _{CC} = 3.6 V, V _I = 5.5 V				20			20	
	V _{CC} = 3.6 V, V _I = V _{CC}		A or B ports§		1			1	
	V _{CC} = 3.6 V, V _I = 0				-5			-5	
I _{off}	V _{CC} = 0, V _I or V _O = 0 to 4.5 V					±100			µA
I _{I(hold)}	V _{CC} = 3 V		V _I = 0.8 V		75			75	
			V _I = 2 V		-75			-75	
I _{OZH}	V _{CC} = 3.6 V, V _O = 3 V					1			µA
I _{OZL}	V _{CC} = 3.6 V, V _O = 0.5 V					-1			µA
I _{CC}	V _{CC} = 3.6 V, V _I = V _{CC} or GND		I _O = 0,		Outputs high			2	
					Outputs low			15	
					Outputs disabled			2	
ΔI _{CC} ¶	V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND					0.2			mA
C _i	V _I = 3 V or 0					4			pF
C _{io}	V _O = 3 V or 0					11			pF
C _o	V _O = 3 V or 0					8			pF

NOTE 3: Product preview specifications are design goals only and are subject to change without notice.

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ Unused pins at V_{CC} or GND

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

SN54LVT18504, SN74LVT18504
3.3-V ABT SCAN TEST DEVICES WITH
20-BIT UNIVERSAL BUS TRANSCEIVERS

SCBS163 – AUGUST 1993

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Note 3 and Figure 1)

			SN54LVT18504				SN74LVT18504				UNIT
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{clock}	Clock frequency	CLKAB or CLKBA				0	100			MHz	
t _w	Pulse duration	CLKAB or CLKBA high or low				4				ns	
		LEAB or LEBA	CLK high or low			3.5					
t _{su}	Setup time	A before CLKAB↑ or B before CLKBA↑				4				ns	
		A before LEAB↓ or B before LEBA↓	CLK high			3.5					
			CLK low			2					
		CLKEN before CLK↑				4					
t _h	Hold time	A after CLKAB↑ or B after CLKBA↑				0				ns	
		A after LEAB↓ or B after LEBA↓				2					
		CLKEN after CLK↑				0					

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Note 3 and Figure 1)

			SN54LVT18504				SN74LVT18504				UNIT
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{clock}	Clock frequency	TCK				0	50			MHz	
t _w	Pulse duration	TCK high or low				8				ns	
t _{su}	Setup time	A, B, CLK, CLKEN, LE, or OE before TCK↑				4.5				ns	
		TDI before TCK↑				7.5					
		TMS before TCK↑				3					
t _h	Hold time	A, B, CLK, CLKEN, LE, or OE after TCK↑				0.5				ns	
		TDI after TCK↑				0.5					
		TMS after TCK↑				0.5					
t _d	Delay time	Power up to TCK↑				50				ns	
t _r	Rise time	V _{CC} power up				1				μs	

NOTE 3: Product preview specifications are design goals only and are subject to change without notice.

PRODUCT PREVIEW



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SN54LVT18504, SN74LVT18504
3.3-V ABT SCAN TEST DEVICES WITH
20-BIT UNIVERSAL BUS TRANSCEIVERS

SCBS163 - AUGUST 1993

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Note 3 and Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT18504		SN74LVT18504		UNIT	
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V	V _{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MAX	MIN		MAX
f _{max}	CLKAB or CLKBA					100		MHz
t _{PLH}	A or B	B or A				2	6	ns
t _{PHL}						2	6.5	
t _{PLH}	CLKAB or CLKBA	B or A				2.5	6.8	ns
t _{PHL}						2.5	6.5	
t _{PLH}	LEAB or LEBA	B or A				2.5	7.1	ns
t _{PHL}						2.5	7.2	
t _{PZH}	OEAB or OEBA	B or A				2	7	ns
t _{PZL}						2.5	8	
t _{PHZ}	OEAB or OEBA	B or A				3	8.8	ns
t _{PLZ}						2.5	7.3	

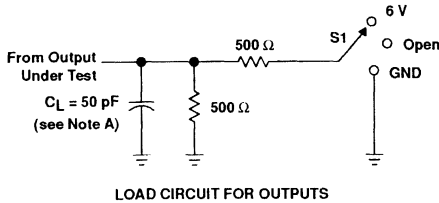
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Note 3 and Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT18504		SN74LVT18504		UNIT	
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V	V _{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MAX	MIN		MAX
f _{max}	TCK					50		MHz
t _{PLH}	TCK↓	A or B				2.5	13.5	ns
t _{PHL}						2.5	12.5	
t _{PLH}	TCK↓	TDO				2	5.6	ns
t _{PHL}						2	6.5	
t _{PZH}	TCK↓	A or B				4.5	13.8	ns
t _{PZL}						5	14.5	
t _{PZH}	TCK↓	TDO				2	7	ns
t _{PZL}						3	7.5	
t _{PHZ}	TCK↓	A or B				4	17	ns
t _{PLZ}						3.5	16	
t _{PHZ}	TCK↓	TDO				3	7.5	ns
t _{PLZ}						3	7.5	

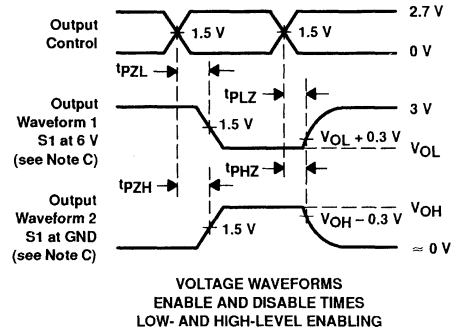
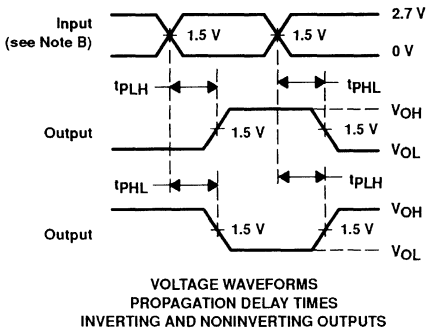
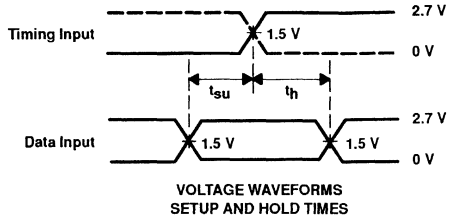
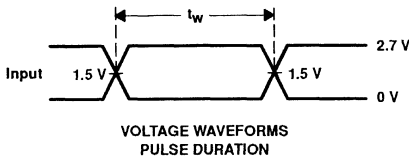
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PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

General Information

1

LVT Octals and Widebus™

2

LVC MSI, Octals and Widebus™

3

ALVC Widebus™

4

LV MSI and Octals

5

GTL Widebus™

6

CBT Bus Switches and 5-V/3-V Volt. Translators

7

Application Notes

8

LVT Characterization Information

9

Mechanical Data

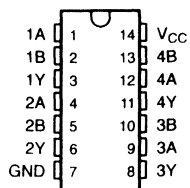
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SN74LVC00 QUADRUPLE 2-INPUT POSITIVE-NAND GATE

JANUARY 1993

- **Space-Saving Package Option: Shrink Small-Outline Package (DB)**
Features EIAJ 0.65-mm Lead Pitch
- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Designed to Facilitate Incident Wave Switching for Line Impedances of 50 Ω or Greater**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline and Thin Shrink Small-Outline Packages**

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This quadruple 2-input positive-NAND gate is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC00 performs the Boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN74LVC00 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LVC00 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

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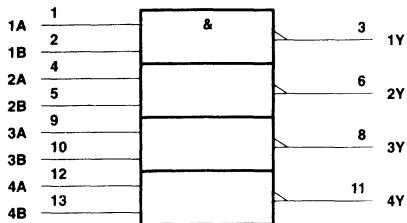
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PRODUCT PREVIEW

SN74LVC00 QUADRUPLE 2-INPUT POSITIVE-NAND GATE

JANUARY 1993

logic symbol†



logic diagram, each gate (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air):	
D package	0.7 W
DB package	0.4 W
PW package	0.4 W
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7$ V	-12	mA
		$V_{CC} = 3$ V	-24 [§]	
I_{OL}	Low-level output current	$V_{CC} = 2.7$ V	12	mA
		$V_{CC} = 3$ V	24 [§]	
$\Delta V/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	-40	85	°C

NOTE 3: Unused or floating inputs must be held high or low.

[§] Current duty cycle ≤ 50%, $f \geq 1$ kHz

PRODUCT PREVIEW

SN74LVC00
QUADRUPLE 2-INPUT POSITIVE-NAND GATE

JANUARY 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}^{\dagger}	MIN	TYP	MAX	UNIT
V_{IK}	$I_I = -18 \text{ mA}$	2.7 V			-1.2	V
V_{OH}	$I_{OH} = -100 \mu\text{A}$	MIN to MAX	$V_{CC} - 0.2$			V
	$I_{OH} = -12 \text{ mA}$	2.7 V	2.2			
	$I_{OH} = -24 \text{ mA}$	3 V	2.4			
V_{OL}	$I_{OL} = 100 \mu\text{A}$	MIN to MAX			0.2	V
	$I_{OL} = 12 \text{ mA}$	2.7 V			0.4	
	$I_{OL} = 24 \text{ mA}$	3 V			0.55	
I_I	$V_I = V_{CC} \text{ or GND}$	3.6 V			± 5	μA
I_{OZ}	$V_O = V_{CC} \text{ or GND}$	3.6 V			+10	μA
I_{CC}	$V_I = V_{CC} \text{ or GND}, I_O = 0$	3.6 V			20	μA
ΔI_{CC}	$V_{CC} = 3 \text{ V to } 3.6 \text{ V},$ Other inputs at $V_{CC} \text{ or GND}$	One input at $V_{CC} - 0.6 \text{ V},$			500	μA
C_i	$V_I = V_{CC} \text{ or GND}$	3.3 V		TBD		pF
C_o	$V_O = V_{CC} \text{ or GND}$	3.3 V		TBD		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

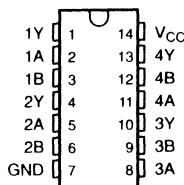
PRODUCT PREVIEW

SN74LVC02 QUADRUPLE 2-INPUT POSITIVE-NOR GATE

JANUARY 1993

- **Space-Saving Package Option: Shrink Small-Outline Package (DB) Features EIAJ 0.65-mm Lead Pitch**
- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Designed to Facilitate Incident Wave Switching for Line Impedances of 50 Ω or Greater**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline and Thin Shrink Small-Outline Packages**

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This quadruple 2-input positive-NOR gate is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC02 performs the Boolean functions $Y = \overline{A + B}$ or $Y = \overline{A} \cdot \overline{B}$ in positive logic.

The SN74LVC02 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LVC02 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

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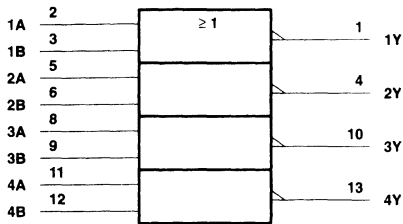


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SN74LVC02 QUADRUPLE 2-INPUT POSITIVE-NOR GATE

JANUARY 1993

logic symbol†



logic diagram, each gate (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air):	
D package	0.7 W
DB package	0.4 W
PW package	0.4 W
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7$ V	-12	mA
		$V_{CC} = 3$ V	-24§	
I_{OL}	Low-level output current	$V_{CC} = 2.7$ V	12	mA
		$V_{CC} = 3$ V	24§	
$\Delta V/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	-40	85	°C

NOTE 3: Unused or floating inputs must be held high or low.

§ Current duty cycle ≤ 50%, $f \geq 1$ kHz

PRODUCT PREVIEW

SN74LVC02
QUADRUPLE 2-INPUT POSITIVE-NOR GATE

JANUARY 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

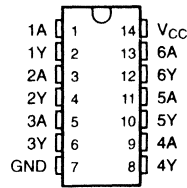
PARAMETER	TEST CONDITIONS	V _{CC} [†]	MIN	TYP	MAX	UNIT
V _{IK}	I _I = -18 mA	2.7 V			-1.2	V
V _{OH}	I _{OH} = -100 μA	MIN to MAX	V _{CC} - 0.2			V
	I _{OH} = -12 mA	2.7 V	2.2			
		3 V	2.4			
	I _{OH} = -24 mA	3 V	2			
V _{OL}	I _{OL} = 100 μA	MIN to MAX			0.2	V
	I _{OL} = 12 mA	2.7 V			0.4	
	I _{OL} = 24 mA	3 V			0.55	
I _I	V _I = V _{CC} or GND	3.6 V			±5	μA
I _{OZ}	V _O = V _{CC} or GND	3.6 V			±10	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V			20	μA
ΔI _{CC}	V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND				500	μA
C _i	V _I = V _{CC} or GND	3.3 V	TBD			pF
C _o	V _O = V _{CC} or GND	3.3 V	TBD			pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

- **Space-Saving Package Option: Shrink Small-Outline Package (DB)**
Features EIAJ 0.65-mm Lead Pitch
- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Designed to Facilitate Incident Wave Switching for Line Impedances of 50 Ω or Greater**
- **Typical V_{OLP} (Output Ground Bounce)**
< 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- **Typical V_{OHV} (Output V_{OH} Undershoot)**
> 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline and Thin Shrink Small-Outline Packages**

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This hex inverter is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC04 contains six independent inverters. The device performs the Boolean function $Y = \bar{A}$.

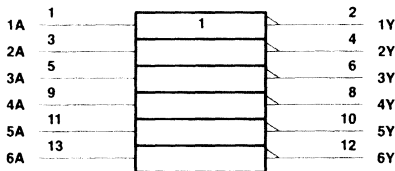
The SN74LVC04 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LVC04 is characterized for operation from -40°C to 85°C .

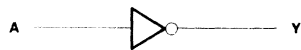
FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

logic symbol†



logic diagram, each inverter (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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SN74LVC04 HEX INVERTER

JANUARY 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air):	
D package	0.7 W
DB package	0.4 W
PW package	0.4 W
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7$ V		-12
		$V_{CC} = 3$ V		-24 [†]
I_{OL}	Low-level output current	$V_{CC} = 2.7$ V		12
		$V_{CC} = 3$ V		24 [†]
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	-40	85	°C

NOTE 3: Unused or floating inputs must be held high or low.

[†] Current duty cycle ≤ 50%, $f \geq 1$ kHz

PRODUCT PREVIEW

SN74LVC04 HEX INVERTER

JANUARY 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

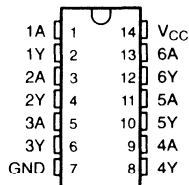
PARAMETER	TEST CONDITIONS	V_{CC}^{\dagger}	MIN	TYP	MAX	UNIT
V_{IK}	$I_I = -18 \text{ mA}$	2.7 V			-1.2	V
V_{OH}	$I_{OH} = -100 \mu\text{A}$	MIN to MAX	$V_{CC} - 0.2$			V
	$I_{OH} = -12 \text{ mA}$	2.7 V	2.2			
		3 V	2.4			
	$I_{OH} = -24 \text{ mA}$	3 V	2			
V_{OL}	$I_{OL} = 100 \mu\text{A}$	MIN to MAX			0.2	V
	$I_{OL} = 12 \text{ mA}$	2.7 V			0.4	
	$I_{OL} = 24 \text{ mA}$	3 V			0.55	
I_I	$V_I = V_{CC} \text{ or GND}$	3.6 V			± 5	μA
I_{OZ}	$V_O = V_{CC} \text{ or GND}$	3.6 V			± 10	μA
I_{CC}	$V_I = V_{CC} \text{ or GND},$ $I_O = 0$	3.6 V			20	μA
ΔI_{CC}	$V_{CC} = 3 \text{ V to } 3.6 \text{ V},$ Other inputs at $V_{CC} \text{ or GND}$ One input at $V_{CC} - 0.6 \text{ V},$				500	μA
C_i	$V_I = V_{CC} \text{ or GND}$	3.3 V		TBD		pF
C_o	$V_O = V_{CC} \text{ or GND}$	3.3 V		TBD		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

- **Space-Saving Package Option:**
Shrink Small-Outline Package (DB)
Features EIAJ 0.65-mm Lead Pitch
- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Designed to Facilitate Incident Wave Switching for Line Impedances of 50 Ω or Greater**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3 V, T_A = 25^\circ C$**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3 V, T_A = 25^\circ C$**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline and Thin Shrink Small-Outline Packages**

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This hex inverter is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVCU04 contains six independent inverters with unbuffered outputs. The device performs the Boolean function $Y = \bar{A}$.

The SN74LVCU04 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LVCU04 is characterized for operation from $-40^\circ C$ to $85^\circ C$.

FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

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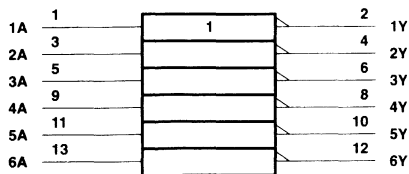


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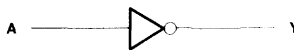
SN74LVCU04 HEX INVERTER

JANUARY 1993

logic symbol†



logic diagram, each inverter (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND pins	± 100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air):	
D package	0.7 W
DB package	0.4 W
PW package	0.4 W
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7$ V	-12	mA
		$V_{CC} = 3$ V	-24 [§]	
I_{OL}	Low-level output current	$V_{CC} = 2.7$ V	12	mA
		$V_{CC} = 3$ V	24 [§]	
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	-40	85	°C

NOTE 3: Unused or floating inputs must be held high or low.

[§] Current duty cycle $\leq 50\%$, $f \geq 1$ kHz

PRODUCT PREVIEW

SN74LVCU04 HEX INVERTER

JANUARY 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} [†]	MIN	TYP	MAX	UNIT
V _{IK}	I _I = -18 mA	2.7 V			-1.2	V
V _{OH}	I _{OH} = -100 μA	MIN to MAX				V
	I _{OH} = -12 mA	2.7 V				
		3 V				
	I _{OH} = -24 mA	3 V				
V _{OL}	I _{OL} = 100 μA	MIN to MAX				V
	I _{OL} = 12 mA	2.7 V				
	I _{OL} = 24 mA	3 V				
I _I	V _I = V _{CC} or GND	3.6 V			±5	μA
I _{OZ}	V _O = V _{CC} or GND	3.6 V			±10	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V			20	μA
ΔI _{CC}	V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND				500	μA
C _I	V _I = V _{CC} or GND	3.3 V		TBD		pF
C _O	V _O = V _{CC} or GND	3.3 V		TBD		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

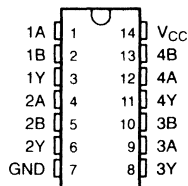
PRODUCT PREVIEW

SN74LVC08 QUADRUPLE 2-INPUT POSITIVE-AND GATE

JANUARY 1993

- **Space-Saving Package Option:**
Shrink Small-Outline Package (DB)
Features EIAJ 0.65-mm Lead Pitch
- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Designed to Facilitate Incident Wave Switching for Line Impedances of 50 Ω or Greater**
- **Typical V_{OLP} (Output Ground Bounce)**
< 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- **Typical V_{OHV} (Output V_{OH} Undershoot)**
> 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline and Thin Shrink Small-Outline Packages**

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This quadruple 2-input positive-AND gate is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC08 performs the Boolean functions $Y = A \cdot B$ or $Y = \overline{A + B}$ in positive logic.

The SN74LVC08 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LVC08 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

PRODUCT PREVIEW

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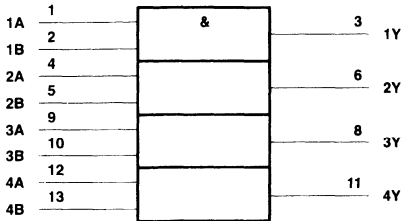
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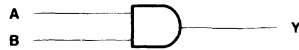
SN74LVC08 QUADRUPLE 2-INPUT POSITIVE-AND GATE

JANUARY 1993

logic symbol†



logic diagram, each gate (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air):	
D package	0.7 W
DB package	0.4 W
PW package	0.4 W
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7$ V	-12	mA
		$V_{CC} = 3$ V	-24 [§]	
I_{OL}	Low-level output current	$V_{CC} = 2.7$ V	12	mA
		$V_{CC} = 3$ V	24 [§]	
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	-40	85	°C

NOTE 3. Unused or floating inputs must be held high or low.

[§] Current duty cycle ≤ 50%, $f \geq 1$ kHz

PRODUCT PREVIEW

SN74LVC08
QUADRUPLE 2-INPUT POSITIVE-AND GATE

JANUARY 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} [†]	MIN	TYP	MAX	UNIT
V _{IK}	I _I = -18 mA	2.7 V			-1.2	V
V _{OH}	I _{OH} = -100 μA	MIN to MAX	V _{CC} - 0.2			V
	I _{OH} = -12 mA	2.7 V	2.2			
		3 V	2.4			
	I _{OH} = -24 mA	3 V	2			
V _{OL}	I _{OL} = 100 μA	MIN to MAX			0.2	V
	I _{OL} = 12 mA	2.7 V			0.4	
	I _{OL} = 24 mA	3 V			0.55	
I _I	V _I = V _{CC} or GND	3.6 V			±5	μA
I _{OZ}	V _O = V _{CC} or GND	3.6 V			±10	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V			20	μA
ΔI _{CC}	V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND				500	μA
C _I	V _I = V _{CC} or GND	3.3 V		TBD		pF
C _O	V _O = V _{CC} or GND	3.3 V		TBD		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

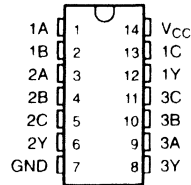
SN74LVC10

TRIPLE 3-INPUT POSITIVE-NAND GATE

JANUARY 1993

- **Space-Saving Package Option:**
Shrink Small-Outline Package (DB)
Features EIAJ 0.65-mm Lead Pitch
- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- **Designed to Facilitate Incident Wave Switching** for Line Impedances of 50 Ω or Greater
- **Typical V_{OLP} (Output Ground Bounce)**
< 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- **Typical V_{OHV} (Output V_{OH} Undershoot)**
> 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline and Thin Shrink Small-Outline Packages**

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This triple 3-input positive-NAND gate is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC10 performs the Boolean functions $Y = \overline{A \cdot B \cdot C}$ or $Y = A + B + C$ in positive logic.

The SN74LVC10 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LVC10 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each gate)

INPUTS			OUTPUT
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

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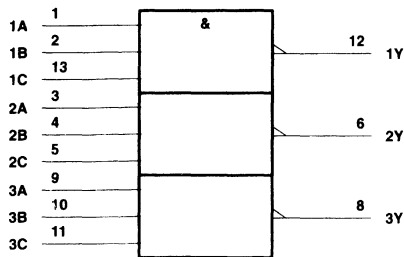
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PRODUCT PREVIEW

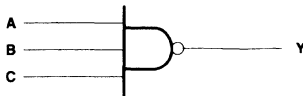
SN74LVC10 TRIPLE 3-INPUT POSITIVE-NAND GATE

JANUARY 1993

logic symbol†



logic diagram, each gate (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air):	
D package	0.7 W
DB package	0.4 W
PW package	0.4 W
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7$ V	-12	mA
		$V_{CC} = 3$ V	-24 [§]	
I_{OL}	Low-level output current	$V_{CC} = 2.7$ V	12	mA
		$V_{CC} = 3$ V	24 [§]	
$\Delta V/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	-40	85	°C

NOTE 3: Unused or floating inputs must be held high or low.

[§] Current duty cycle ≤ 50%, $f \geq 1$ kHz

PRODUCT PREVIEW

SN74LVC10 TRIPLE 3-INPUT POSITIVE-NAND GATE

JANUARY 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} [†]	MIN	TYP	MAX	UNIT
V _{IK}	I _I = -18 mA	2.7 V			-1.2	V
V _{OH}	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2			V
	I _{OH} = -12 mA	2.7 V	2.2			
	I _{OH} = -24 mA	3 V	2.4			
V _{OL}	I _{OL} = 100 μA	MIN to MAX			0.2	V
	I _{OL} = 12 mA	2.7 V			0.4	
	I _{OL} = 24 mA	3 V			0.55	
I _I	V _I = V _{CC} or GND	3.6 V			±5	μA
I _{OZ}	V _O = V _{CC} or GND	3.6 V			±10	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V			20	μA
ΔI _{CC}	V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V. Other inputs at V _{CC} or GND				500	μA
C _i	V _I = V _{CC} or GND	3.3 V	TBD			pF
C _o	V _O = V _{CC} or GND	3.3 V	TBD			pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

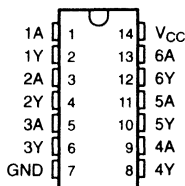
PRODUCT PREVIEW

SN74LVC14 HEX SCHMITT-TRIGGER INVERTER

MARCH 1993

- **Space-Saving Package Option:**
Shrink Small-Outline Package (DB)
Features EIAJ 0.65-mm Lead Pitch
- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Designed to Facilitate Incident Wave Switching for Line Impedances of 50 Ω or Greater**
- **Typical V_{OLP} (Output Ground Bounce)**
< 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- **Typical V_{OHV} (Output V_{OH} Undershoot)**
> 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline and Thin Shrink Small-Outline Packages**

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This hex Schmitt-trigger inverter is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC14 contains six independent inverters. The device performs the Boolean function $Y = \bar{A}$.

The SN74LVC14 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LVC14 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

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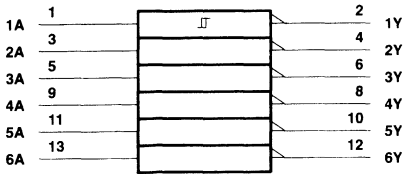
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PRODUCT PREVIEW

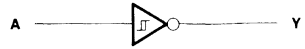
SN74LVC14 HEX SCHMITT-TRIGGER INVERTER

MARCH 1993

logic symbol†



logic diagram, each inverter (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air):		
D package	0.7 W
DB package	0.4 W
PW package	0.4 W
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7$ V	-12	mA
		$V_{CC} = 3$ V	-24§	
I_{OL}	Low-level output current	$V_{CC} = 2.7$ V	12	mA
		$V_{CC} = 3$ V	24§	
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	-40	85	°C

NOTE 3: Unused or floating inputs must be held high or low.

§ Current duty cycle ≤ 50%, $f \geq 1$ kHz

PRODUCT PREVIEW

SN74LVC14 HEX SCHMITT-TRIGGER INVERTER

MARCH 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} [†]	MIN	TYP	MAX	UNIT
V _{IK}	I _I = -18 mA	2.7 V			-1.2	V
V _{OH}	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2			V
	I _{OH} = -12 mA	2.7 V	2.2			
	I _{OH} = -24 mA	3 V	2.4			
V _{OL}	I _{OL} = 100 μA	MIN to MAX			0.2	V
	I _{OL} = 12 mA	2.7 V			0.4	
	I _{OL} = 24 mA	3 V			0.55	
I _I	V _I = V _{CC} or GND	3.6 V			±5	μA
I _{OZ}	V _O = V _{CC} or GND	3.6 V			±10	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V			20	μA
ΔI _{CC}	V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND				500	μA
C _i	V _I = V _{CC} or GND	3.3 V			TBD	pF
C _o	V _O = V _{CC} or GND	3.3 V			TBD	pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

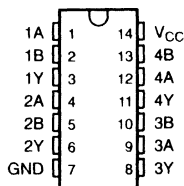
PRODUCT PREVIEW

SN74LVC32 QUADRUPLE 2-INPUT POSITIVE-OR GATE

JANUARY 1993

- **Space-Saving Package Option: Shrink Small-Outline Package (DB) Features EIAJ 0.65-mm Lead Pitch**
- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Designed to Facilitate Incident Wave Switching for Line Impedances of 50 Ω or Greater**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline and Thin Shrink Small-Outline Packages**

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This quadruple 2-input positive-OR gate is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC32 performs the Boolean functions $Y = A + B$ or $Y = \overline{A} \cdot \overline{B}$ in positive logic.

The SN74LVC32 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LVC32 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

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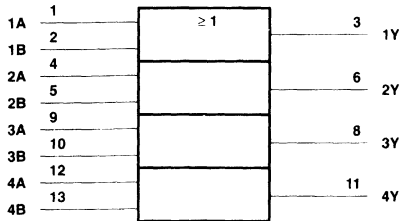
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PRODUCT PREVIEW

SN74LVC32 QUADRUPLE 2-INPUT POSITIVE-OR GATE

JANUARY 1993

logic symbol†



logic diagram, each gate (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air):	
D package	0.7 W
DB package	0.4 W
PW package	0.4 W
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7$ V		mA
		$V_{CC} = 3$ V		
I_{OL}	Low-level output current	$V_{CC} = 2.7$ V		mA
		$V_{CC} = 3$ V		
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	-40	85	°C

NOTE 3: Unused or floating inputs must be held high or low.

§ Current duty cycle $\leq 50\%$, $f \geq 1$ kHz

SN74LVC32 QUADRUPLE 2-INPUT POSITIVE-OR GATE

JANUARY 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} [†]	MIN	TYP	MAX	UNIT
V _{IK}	I _I = -18 mA	2.7 V			-1.2	V
V _{OH}	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2			V
	I _{OH} = -12 mA	2.7 V	2.2			
	I _{OH} = -24 mA	3 V	2.4			
V _{OL}	I _{OL} = 100 μA	MIN to MAX			0.2	V
	I _{OL} = 12 mA	2.7 V			0.4	
	I _{OL} = 24 mA	3 V			0.55	
I _I	V _I = V _{CC} or GND	3.6 V			±5	μA
I _{OZ}	V _O = V _{CC} or GND	3.6 V			±10	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V			20	μA
ΔI _{CC}	V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND				500	μA
C _i	V _I = V _{CC} or GND	3.3 V	TBD			pF
C _o	V _O = V _{CC} or GND	3.3 V	TBD			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

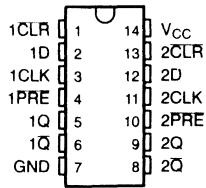
SN74LVC74

DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

JANUARY 1993

- **Space-Saving Package Option: Shrink Small-Outline Package (DB) Features EIAJ 0.65-mm Lead Pitch**
- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Designed to Facilitate Incident Wave Switching for Line Impedances of 50 Ω or Greater**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline and Thin Shrink Small-Outline Packages**

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This dual positive-edge-triggered D-type flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation.

A low level at the preset (PRE) or clear (CLR) inputs sets or resets the outputs regardless of the levels of the other inputs. When PRE and CLR are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input may be changed without affecting the levels at the outputs.

The SN74LVC74 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LVC74 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

INPUTS				OUTPUTS	
PRE	CLR	CLK	D	Q	\bar{Q}
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H [†]	H [†]
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	\bar{Q}_0

[†] This configuration is nonstable; that is, it will not persist when PRE or CLR returns to its inactive (high) level.

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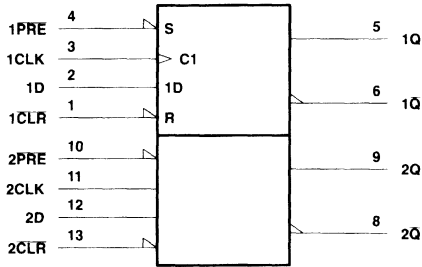
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PRODUCT PREVIEW

SN74LVC74
DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP
WITH CLEAR AND PRESET

JANUARY 1993

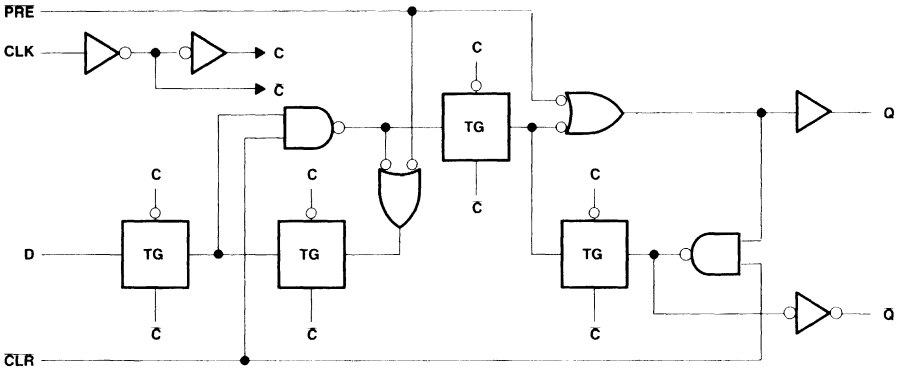
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each flip-flop (positive logic)

PRODUCT PREVIEW



SN74LVC74 DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

JANUARY 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air):	
D package	0.7 W
DB package	0.4 W
PW package	0.4 W
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7$ V		mA
		$V_{CC} = 3$ V		
I_{OL}	Low-level output current	$V_{CC} = 2.7$ V		mA
		$V_{CC} = 3$ V		
$\Delta V/\Delta t$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	-40	85	°C

NOTE 3: Unused or floating inputs must be held high or low.

[†] Current duty cycle ≤ 50%, $f \geq 1$ kHz

PRODUCT PREVIEW

SN74LVC74
DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP
WITH CLEAR AND PRESET

JANUARY 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} [†]	MIN	TYP	MAX	UNIT
V _{IK}	I _I = -18 mA	2.7 V			-1.2	V
V _{OH}	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2			V
	I _{OH} = -12 mA	2.7 V	2.2			
	I _{OH} = -24 mA	3 V	2.4			
V _{OL}	I _{OL} = 100 μA	MIN to MAX			0.2	V
	I _{OL} = 12 mA	2.7 V			0.4	
	I _{OL} = 24 mA	3 V			0.55	
I _I	V _I = V _{CC} or GND	3.6 V			+5	μA
I _{OZ}	V _O = V _{CC} or GND	3.6 V			+10	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V			20	μA
ΔI _{CC}	V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC} or GND, One input at V _{CC} - 0.6 V,				500	μA
C _i	V _I = V _{CC} or GND	3.3 V	TBD			pF
C _o	V _O = V _{CC} or GND	3.3 V	TBD			pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

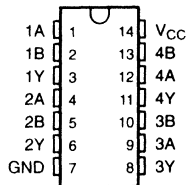
PRODUCT PREVIEW

SN74LVC86 QUADRUPLE 2-INPUT EXCLUSIVE-OR GATE

JANUARY 1993

- **Space-Saving Package Option:**
Shrink Small-Outline Package (DB)
Features EIAJ 0.65-mm Lead Pitch
- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- **Designed to Facilitate Incident Wave Switching** for Line Impedances of 50 Ω or Greater
- **Typical V_{OLP} (Output Ground Bounce)**
< 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- **Typical V_{OHV} (Output V_{OH} Undershoot)**
> 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline and Thin Shrink Small-Outline Packages**

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This quadruple 2-input exclusive-OR gate is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC86 performs the Boolean function $Y = A \oplus B = \bar{A}B + A\bar{B}$ in positive logic.

A common application is as a true/complement element. If one of the inputs is low, the other input will be reproduced in true form at the output. If one of the inputs is high, the signal on the other input will be reproduced inverted at the output.

The SN74LVC86 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LVC86 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

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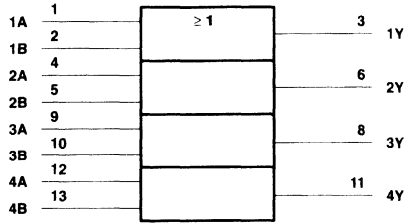
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PRODUCT PREVIEW

SN74LVC86 QUADRUPLE 2-INPUT EXCLUSIVE-OR GATE

JANUARY 1993

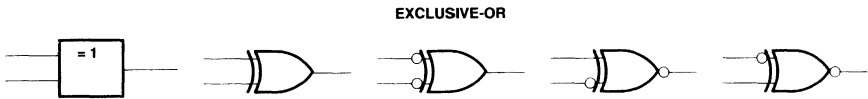
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

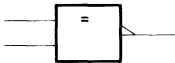
exclusive-OR logic

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.



These are five equivalent exclusive-OR symbols valid for an SN74LVC86 gate in positive logic; negation may be shown at any two ports.

LOGIC-IDENTITY ELEMENT



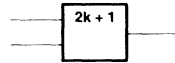
The output is active (low) if all inputs stand at the same logic level (i.e., $A = B$).

EVEN-PARITY ELEMENT



The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

ODD-PARITY ELEMENT



The output is active (high) if an odd number of outputs (i.e., only 1 of the 2) are active.

PRODUCT PREVIEW

SN74LVC86 QUADRUPLE 2-INPUT EXCLUSIVE-OR GATE

JANUARY 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air):	
D package	0.7 W
DB package	0.4 W
PW package	0.4 W
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7$ V		-12
		$V_{CC} = 3$ V		-24 [‡]
I_{OL}	Low-level output current	$V_{CC} = 2.7$ V		12
		$V_{CC} = 3$ V		24 [‡]
$\Delta V/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	-40	85	°C

NOTE 3: Unused or floating inputs must be held high or low.

[‡] Current duty cycle ≤ 50%, $f \geq 1$ kHz

PRODUCT PREVIEW

SN74LVC86 QUADRUPLE 2-INPUT EXCLUSIVE-OR GATE

JANUARY 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}^{\dagger}	MIN	TYP	MAX	UNIT
V_{IK}	$I_i = -18 \text{ mA}$	2.7 V			-1.2	V
V_{OH}	$I_{OH} = -100 \mu\text{A}$	MIN to MAX	$V_{CC} - 0.2$			V
	$I_{OH} = -12 \text{ mA}$	2.7 V	2.2			
		3 V	2.4			
V_{OL}	$I_{OH} = -24 \text{ mA}$	3 V	2			V
	$I_{OL} = 100 \mu\text{A}$	MIN to MAX			0.2	
	$I_{OL} = 12 \text{ mA}$	2.7 V			0.4	
	$I_{OL} = 24 \text{ mA}$	3 V			0.55	
I_I	$V_i = V_{CC}$ or GND	3.6 V			± 5	μA
I_{OZ}	$V_O = V_{CC}$ or GND	3.6 V			± 10	μA
I_{CC}	$V_i = V_{CC}$ or GND, $I_O = 0$	3.6 V			20	μA
ΔI_{CC}	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$, Other inputs at V_{CC} or GND One input at $V_{CC} - 0.6 \text{ V}$.				500	μA
C_i	$V_i = V_{CC}$ or GND	3.3 V		TBD		pF
C_o	$V_O = V_{CC}$ or GND	3.3 V		TBD		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

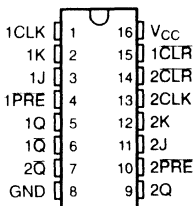
SN74LVC112

DUAL NEGATIVE-EDGE-TRIGGERED J-K FLIP-FLOP WITH CLEAR AND PRESET

JANUARY 1993

- **Space-Saving Package Option:**
Shrink Small-Outline Package (DB)
Features EIAJ 0.65-mm Lead Pitch
- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Designed to Facilitate Incident Wave Switching for Line Impedances of 50 Ω or Greater**
- **Typical V_{OLP} (Output Ground Bounce)**
< 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ$ C
- **Typical V_{OHV} (Output V_{OH} Undershoot)**
> 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ$ C
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline and Thin Shrink Small-Outline Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This dual negative-edge-triggered J-K flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation.

A low level at the preset (PRE) or clear (CLR) inputs sets or resets the outputs regardless of the levels of the other inputs. When PRE and CLR are inactive (high), data at the J and K inputs meeting the setup time requirements is transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. The SN74LVC112 can perform as a toggle flip-flop by tying J and K high.

The SN74LVC112 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LVC112 is characterized for operation from -40° C to 85° C.

FUNCTION TABLE

INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	\bar{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H [†]	H [†]
H	H	↓	L	L	Q_0	\bar{Q}_0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q_0	\bar{Q}_0

[†] This configuration is nonstable; that is, it will not persist when PRE or CLR returns to its inactive (high) level.

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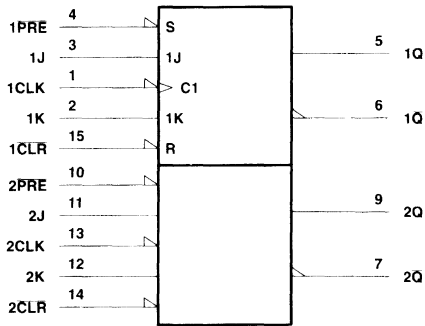
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PRODUCT PREVIEW

SN74LVC112
DUAL NEGATIVE-EDGE-TRIGGERED J-K FLIP-FLOP
WITH CLEAR AND PRESET

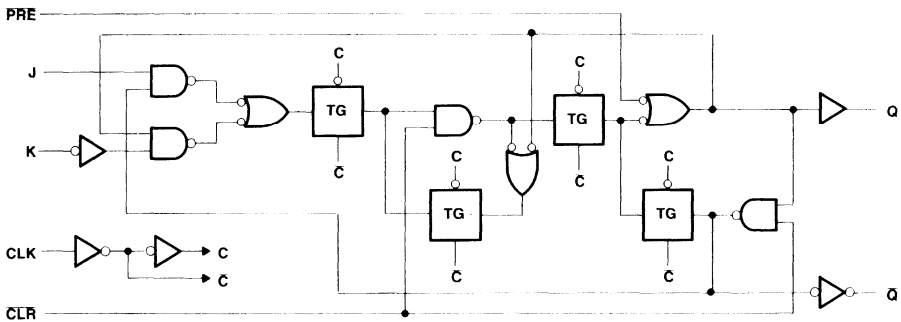
JANUARY 1993

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each flip-flop (positive logic)



PRODUCT PREVIEW

SN74LVC112
DUAL NEGATIVE-EDGE-TRIGGERED J-K FLIP-FLOP
WITH CLEAR AND PRESET

JANUARY 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air):	
DB package	0.4 W
DW package	0.85 W
PW package	0.4 W
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7$ V		mA
		$V_{CC} = 3$ V		
I_{OL}	Low-level output current	$V_{CC} = 2.7$ V		mA
		$V_{CC} = 3$ V		
$\Delta V/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	-40	85	°C

NOTE 3: Unused or floating inputs must be held high or low.

‡ Current duty cycle ≤ 50%, † ≥ 1 kHz

PRODUCT PREVIEW

SN74LVC112
DUAL NEGATIVE-EDGE-TRIGGERED J-K FLIP-FLOP
WITH CLEAR AND PRESET

JANUARY 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}^{\dagger}	MIN	TYP	MAX	UNIT
V_{IK}	$I_I = -18 \text{ mA}$	2.7 V			-1.2	V
V_{OH}	$I_{OH} = -100 \mu\text{A}$	MIN to MAX	$V_{CC} - 0.2$			V
	$I_{OH} = -12 \text{ mA}$	2.7 V	2.2			
		3 V	2.4			
	$I_{OH} = -24 \text{ mA}$	3 V	2			
V_{OL}	$I_{OL} = 100 \mu\text{A}$	MIN to MAX			0.2	V
	$I_{OL} = 12 \text{ mA}$				0.4	
	$I_{OL} = 24 \text{ mA}$				0.55	
I_I	$V_I = V_{CC} \text{ or GND}$	3.6 V			± 5	μA
I_{OZ}	$V_O = V_{CC} \text{ or GND}$	3.6 V			± 10	μA
I_{CC}	$V_I = V_{CC} \text{ or GND.}$	$I_O = 0$	3.6 V			20 μA
ΔI_{CC}	$V_{CC} = 3 \text{ V to } 3.6 \text{ V,}$ Other inputs at V_{CC} or GND	One input at $V_{CC} - 0.6 \text{ V.}$				500 μA
C_i	$V_I = V_{CC} \text{ or GND}$	3.3 V		TBD		pF
C_o	$V_O = V_{CC} \text{ or GND}$	3.3 V		TBD		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

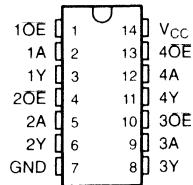
PRODUCT PREVIEW

SN74LVC125 QUADRUPLE BUS BUFFER GATE WITH 3-STATE OUTPUTS

JANUARY 1993

- **Space-Saving Package Option:**
Shrink Small-Outline Package (DB)
Features EIAJ 0.65-mm Lead Pitch
- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Designed to Facilitate Incident Wave Switching for Line Impedances of 50 Ω or Greater**
- **Typical V_{OLP} (Output Ground Bounce)**
< 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- **Typical V_{OHV} (Output V_{OH} Undershoot)**
> 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline and Thin Shrink Small-Outline Packages**

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This quadruple bus buffer gate is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC125 features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (OE) input is high.

The SN74LVC125 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LVC125 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
OE	A	Y
L	H	H
L	L	L
H	X	Z

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PRODUCT PREVIEW

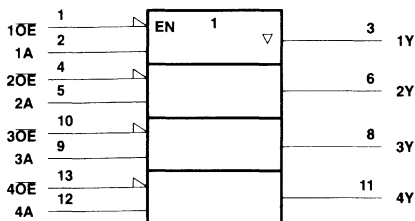
SN74LVC125

QUADRUPLE BUS BUFFER GATE

WITH 3-STATE OUTPUTS

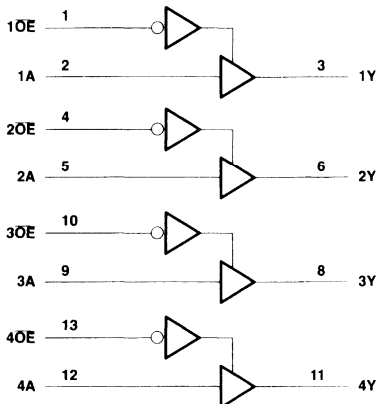
JANUARY 1993

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air):	
D package	0.7 W
DB package	0.4 W
PW package	0.4 W
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.

PRODUCT PREVIEW

SN74LVC125
QUADRUPLE BUS BUFFER GATE
WITH 3-STATE OUTPUTS

JANUARY 1993

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V _{CC}	Supply voltage	2.7	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V		V
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		V
V _I	Input voltage	0	V _{CC}	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2.7 V		-12
		V _{CC} = 3 V		-24 [†]
I _{OL}	Low-level output current	V _{CC} = 2.7 V		12
		V _{CC} = 3 V		24 [†]
Δt/Δv	Input transition rise or fall rate	0	10	ns/V
T _A	Operating free-air temperature	-40	85	°C

NOTE 3: Unused or floating inputs must be held high or low.

[†] Current duty cycle ≤ 50%, f ≥ 1 kHz

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} [‡]	MIN	TYP	MAX	UNIT
V _{IK}	I _I = -18 mA	2.7 V			-1.2	V
V _{OH}	I _{OH} = -100 μA	MIN to MAX	V _{CC} - 0.2			V
	I _{OH} = -12 mA	2.7 V	2.2			
		3 V	2.4			
	I _{OH} = -24 mA	3 V	2			
V _{OL}	I _{OL} = 100 μA	MIN to MAX			0.2	V
	I _{OL} = 12 mA	2.7 V			0.4	
	I _{OL} = 24 mA	3 V			0.55	
I _I	V _I = V _{CC} or GND	3.6 V			±5	μA
I _{OZ}	V _O = V _{CC} or GND	3.6 V			±10	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V			20	μA
ΔI _{CC}	V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC} or GND, One input at V _{CC} - 0.6 V,				500	μA
C _I	V _I = V _{CC} or GND	3.3 V		TBD		pF
C _O	V _O = V _{CC} or GND	3.3 V		TBD		pF

[‡] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

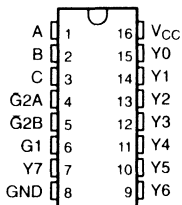
PRODUCT PREVIEW

SN74LVC138 3-LINE TO 8-LINE DECODER/DEMULTIPLEXER

MARCH 1993

- **Space-Saving Package Option:**
Shrink Small-Outline Package (DB)
Features EIAJ 0.65-mm Lead Pitch
- **EPIC™ (Enhanced-Performance Implanted CMOS)** Submicron Process
- **Designed to Facilitate Incident Wave Switching** for Line Impedances of 50 Ω or Greater
- **Typical V_{OLP} (Output Ground Bounce)**
< 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- **Typical V_{OHV} (Output V_{OH} Undershoot)**
> 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline and Thin Shrink Small-Outline Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This 3-line to 8-line decoder/demultiplexer is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC138 is designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, this decoder can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The conditions at the binary-select inputs and the three enable inputs select one of eight input lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The SN74LVC138 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LVC138 is characterized for operation from -40°C to 85°C .

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PRODUCT PREVIEW

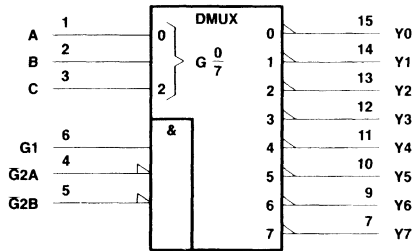
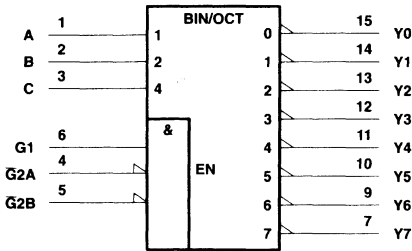
SN74LVC138 3-LINE TO 8-LINE DECODER/DEMULTIPLEXER

MARCH 1993

FUNCTION TABLE

ENABLE INPUTS			SELECT INPUTS			OUTPUTS							
G1	G2A	G2B	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	H	L	H	H	H	H	H	L	H	H
H	L	L	H	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

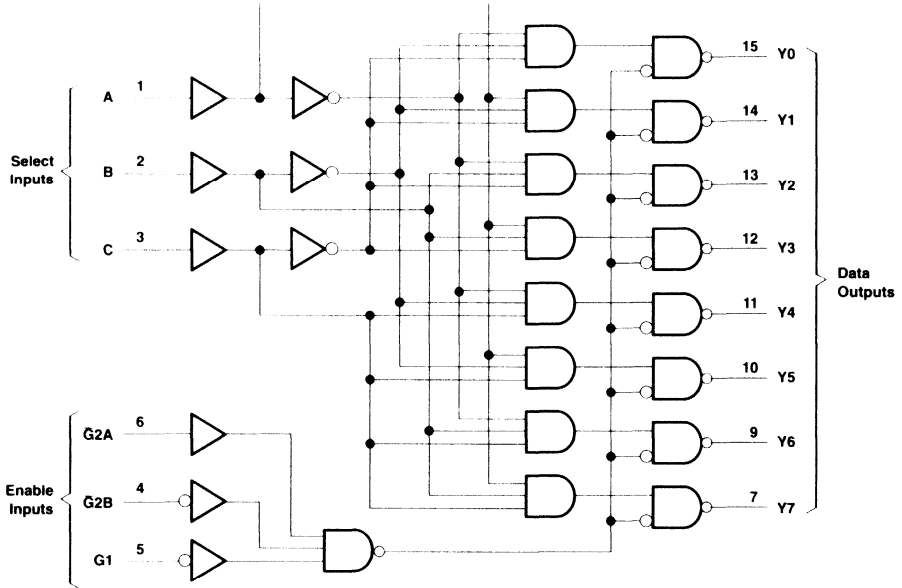
logic symbols (alternatives)†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air):	
DB package	0.4 W
DW package	0.85 W
PW package	0.4 W
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.

SN74LVC138

3-LINE TO 8-LINE DECODER/DEMULTIPLEXER

MARCH 1993

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V _{CC}	Supply voltage	2.7	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V		V
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		V
V _I	Input voltage	0	V _{CC}	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2.7 V		mA
		V _{CC} = 3 V		
I _{OL}	Low-level output current	V _{CC} = 2.7 V		mA
		V _{CC} = 3 V		
Δt/Δv	Input transition rise or fall rate	0	10	ns/V
T _A	Operating free-air temperature	-40	85	°C

NOTE 3: Unused or floating inputs must be held high or low.

† Current duty cycle ≤ 50%, f ≥ 1 kHz

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} †	MIN	TYP	MAX	UNIT
V _{IK}	I _I = -18 mA	2.7 V			-1.2	V
V _{OH}	I _{OH} = -100 μA	MIN to MAX	V _{CC} - 0.2			V
	I _{OH} = -12 mA	2.7 V	2.2			
	I _{OH} = -24 mA	3 V	2.4			
V _{OL}	I _{OL} = 100 μA	MIN to MAX			0.2	V
	I _{OL} = 12 mA	2.7 V			0.4	
	I _{OL} = 24 mA	3 V			0.55	
I _I	V _I = V _{CC} or GND	3.6 V			±5	μA
I _{OZ}	V _O = V _{CC} or GND	3.6 V			±10	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V			20	μA
ΔI _{CC}	V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND				500	μA
C _i	V _I = V _{CC} or GND	3.3 V		TBD		pF
C _o	V _O = V _{CC} or GND	3.3 V		TBD		pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW



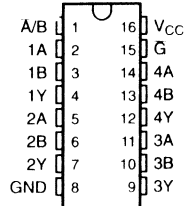
SN74LVC157

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

JANUARY 1993

- **Space-Saving Package Option:**
Shrink Small-Outline Package (DB)
Features EIAJ 0.65-mm Lead Pitch
- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Designed to Facilitate Incident Wave Switching for Line Impedances of 50 Ω or Greater**
- **Typical V_{OLP} (Output Ground Bounce)**
< 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ$ C
- **Typical V_{OHV} (Output V_{OH} Undershoot)**
> 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ$ C
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline and Thin Shrink Small-Outline Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This quadruple 2-line to 1-line data selector/multiplexer is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC157 contains inverters and drivers to supply full data selection to the four output gates. A separate strobe (G) input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. The SN74LVC157 provides true data.

The SN74LVC157 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LVC157 is characterized for operation from -40° C to 85° C.

FUNCTION TABLE

INPUTS				OUTPUT
G	A/B	A	B	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

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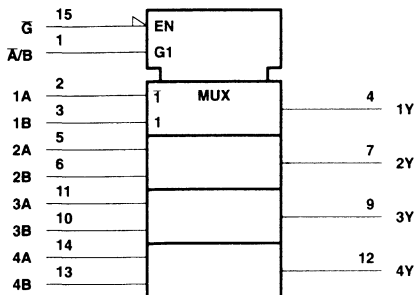
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PRODUCT PREVIEW

SN74LVC157 QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

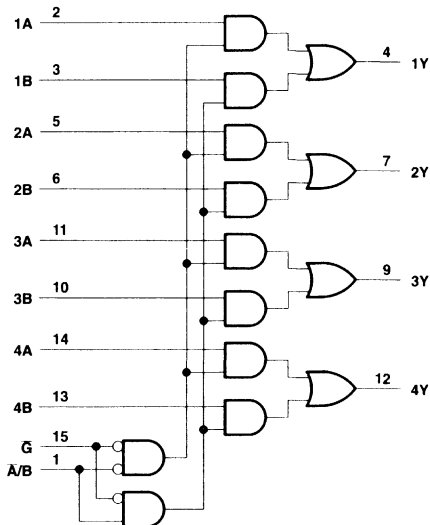
JANUARY 1993

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air):	
DB package	0.4 W
DW package	0.85 W
PW package	0.4 W
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.

SN74LVC157

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

JANUARY 1993

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V _{CC}	Supply voltage	2.7	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V		V
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		V
V _I	Input voltage	0	V _{CC}	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2.7 V		-12
		V _{CC} = 3 V		-24†
I _{OL}	Low-level output current	V _{CC} = 2.7 V		12
		V _{CC} = 3 V		24†
Δt/Δv	Input transition rise or fall rate	0	10	ns/V
T _A	Operating free-air temperature	-40	85	°C

NOTE 3: Unused or floating inputs must be held high or low.

† Current duty cycle ≤ 50%, f > 1 kHz

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} †	MIN	TYP	MAX	UNIT
V _{IK}	I _I = -18 mA	2.7 V			-1.2	V
V _{OH}	I _{OH} = -100 μA	MIN to MAX	V _{CC} - 0.2			V
	I _{OH} = -12 mA	2.7 V	2.2			
	I _{OH} = -24 mA	3 V	2.4			
V _{OL}	I _{OL} = 100 μA	3 V	2			V
	I _{OL} = 12 mA	MIN to MAX			0.2	
	I _{OL} = 24 mA	2.7 V			0.4	
I _I	V _I = V _{CC} or GND	3 V			±5	μA
I _{OZ}	V _O = V _{CC} or GND	3 V			±10	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3 V			20	μA
ΔI _{CC}	V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC} or GND, One input at V _{CC} - 0.6 V.				500	μA
C _i	V _I = V _{CC} or GND	3 V	TBD			pF
C _o	V _O = V _{CC} or GND	3 V	TBD			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

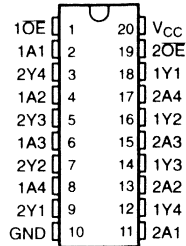
PRODUCT PREVIEW

SN74LVC240 OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

JANUARY 1993

- **Space-Saving Package Option:**
Shrink Small-Outline Package (DB)
Features EIAJ 0.65-mm Lead Pitch
- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Designed to Facilitate Incident Wave Switching for Line Impedances of 50 Ω or Greater**
- **Typical V_{OLP} (Output Ground Bounce)**
< 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- **Typical V_{OHV} (Output V_{OH} Undershoot)**
> 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline and Thin Shrink Small-Outline Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal buffer/driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC240 is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The SN74LVC240 is organized as two 4-bit buffers/line drivers with separate output-enable (OE) inputs. When OE is low, the device passes data from the A inputs to the Y outputs. When OE is high, the outputs are in the high-impedance state.

The SN74LVC240 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LVC240 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
OE	A	Y
L	H	L
L	L	H
H	X	Z

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PRODUCT PREVIEW

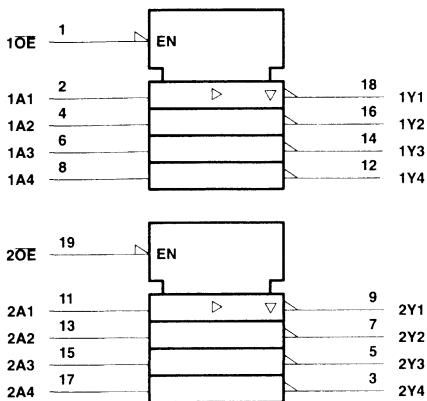
SN74LVC240

OCTAL BUFFER/DRIVER

WITH 3-STATE OUTPUTS

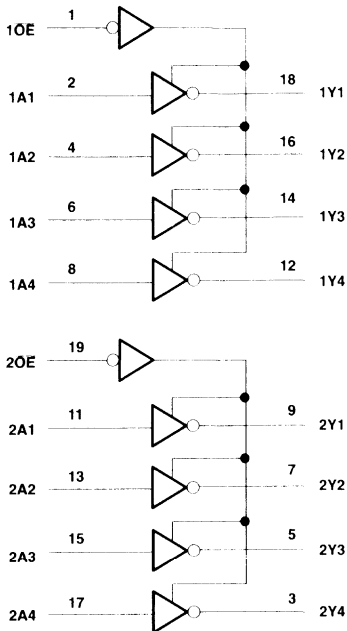
JANUARY 1993

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND pins	± 100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air):	
DB package	0.5 W
DW package	0.85 W
PW package	0.5 W
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.

PRODUCT PREVIEW

SN74LVC240
OCTAL BUFFER/DRIVER
WITH 3-STATE OUTPUTS
 JANUARY 1993

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7$ V		-12
		$V_{CC} = 3$ V		-24†
I_{OL}	Low-level output current	$V_{CC} = 2.7$ V		12
		$V_{CC} = 3$ V		24†
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	-40	85	°C

NOTE 3: Unused or floating inputs must be held high or low.

† Current duty cycle < 50%, $f > 1$ kHz

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC} †	MIN	TYP	MAX	UNIT
V_{IK}	$I_i = -18$ mA	2.7 V			-1.2	V
V_{OH}	$I_{OH} = -100$ μ A	MIN to MAX	$V_{CC} - 0.2$			V
	$I_{OH} = -12$ mA	2.7 V	2.2			
	$I_{OH} = -24$ mA	3 V	2.4			
V_{OL}	$I_{OL} = 100$ μ A	MIN to MAX			0.2	V
	$I_{OL} = 12$ mA	2.7 V			0.4	
	$I_{OL} = 24$ mA	3 V			0.55	
I_i	$V_i = V_{CC}$ or GND	3.6 V			+5	μ A
I_{OZ}	$V_O = V_{CC}$ or GND	3.6 V			+10	μ A
I_{CC}	$V_i = V_{CC}$ or GND, $I_O = 0$	3.6 V			20	μ A
ΔI_{CC}	$V_{CC} = 3$ V to 3.6 V, Other inputs at V_{CC} or GND, One input at $V_{CC} - 0.6$ V.				500	μ A
C_i	$V_i = V_{CC}$ or GND	3.3 V		TBD		pF
C_o	$V_O = V_{CC}$ or GND	3.3 V		TBD		pF

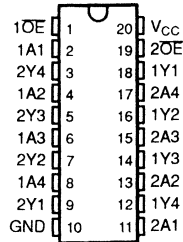
† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

SN74LVC244
OCTAL BUFFERS/LINE DRIVERS
WITH 3-STATE OUTPUTS
NOVEMBER 1993

- **EPIC™ (Enhanced-Performance Implanted CMOS) Sub-Micron Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3 V, T_A = 25^\circ C$**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3 V, T_A = 25^\circ C$**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB) and Thin Shrink Small-Outline (PW) Packages**

DW, DB OR PW PACKAGE
(TOP VIEW)



description

This octal bus transceiver is designed for 2.7 V to 3.6 V V_{CC} operation.

The SN74LVC244 is organized as two 4-bit line drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

The SN74LVC244 is characterized for operation from $-40^\circ C$ to $85^\circ C$.

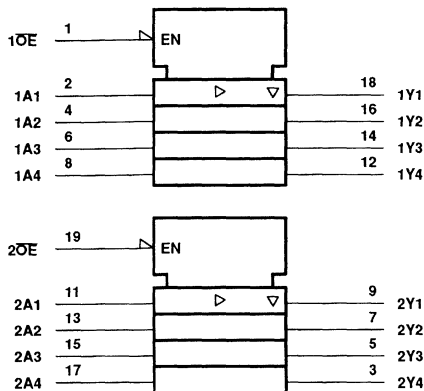
FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
\overline{OE}	A	Y
L	H	H
L	L	L
H	X	Z

PRODUCT PREVIEW

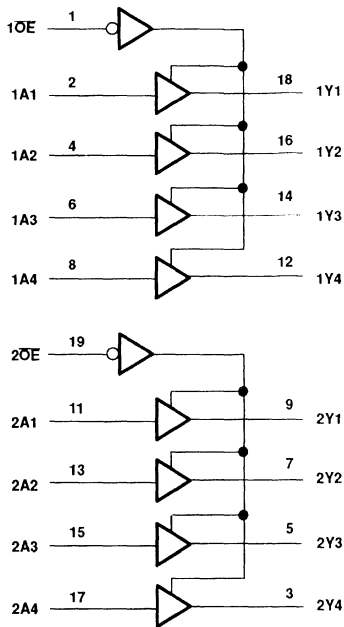
SN74LVC244
OCTAL BUFFERS/LINE DRIVERS
WITH 3-STATE OUTPUTS
 NOVEMBER 1993

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 4.6 V
Output voltage range, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND pins	± 100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air):	
DB package	0.65 W
DW package	0.85 W
PW package	0.6 W
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

SN74LVC244
OCTAL BUFFERS/LINE DRIVERS
WITH 3-STATE OUTPUTS
NOVEMBER 1993

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	2.7		3.6	V
V _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V		2	V
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	V
V _I	Input voltage	0		V _{CC}	V
V _O	Output voltage	0		V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2.7 V		-12	mA
		V _{CC} = 3 V		-24	
I _{OL}	Low-level output current	V _{CC} = 2.7 V		12	mA
		V _{CC} = 3 V		24	
ΔV/ΔV	Input transition rise or fall rate	0		10	ns/V
T _A	Operating free-air temperature	-40		85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = -40 TO 85°C			UNIT
			MIN	TYP	MAX	
V _{OH}	I _{OH} = -100 μA	V _{CC} [†]	V _{CC} - 0.2			V
	I _{OH} = -12 mA	2.7 V	2.2			
	I _{OH} = -12 mA	3 V	2.4			
	I _{OH} = -24 mA	3 V	2			
V _{OL}	I _{OL} = 100 μA	V _{CC} [†]	0.2			V
	I _{OL} = 12 mA	2.7 V	0.4			
	I _{OL} = 24 mA	3 V	0.55			
I _I	V _I = V _{CC} or GND	3.6 V	±5			μA
I _{OZ}	V _O = V _{CC} or GND	3.6 V	±10			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V	20			μA
ΔI _{CC}	V _{CC} = 3 V to 3.6 V, one input at V _{CC} - 0.6 V, other inputs at V _{CC} or GND		500			μA
C _I	Control inputs V _I = V _{CC} or GND	3.3 V	TBD			pF
C _O	A or B ports V _O = V _{CC} or GND	3.3 V	TBD			pF

[†] V_{CC} = Min to Max

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

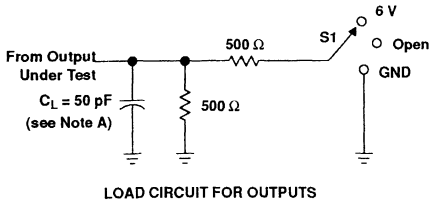
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V	UNIT
			MIN	TYP [†]	MAX	
t _{pd}	A	Y	1.5	7	8	ns
t _{gn}	OE	Y	1.5	8	9.2	ns
t _{dls}			7.5	7.5	8.5	

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

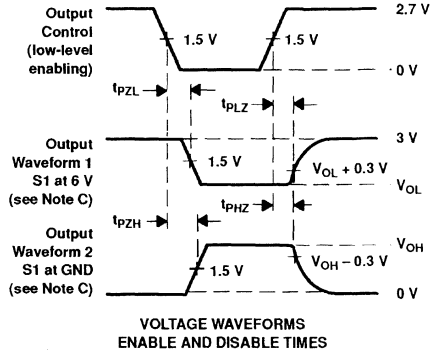
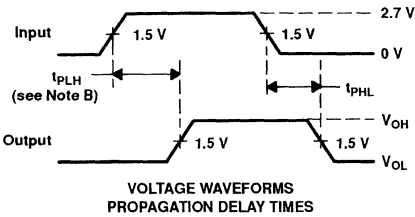
PARAMETER		TEST CONDITIONS		TYP	UNIT
C _{pd}	Power dissipation capacitance	Outputs enabled	C _L = 50 pF, f = 10 MHz	TBD	pF
		Outputs disabled		TBD	pF

PRODUCT PREVIEW

SN74LVC244
OCTAL BUFFERS/LINE DRIVERS
WITH 3-STATE OUTPUTS
 NOVEMBER 1993



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

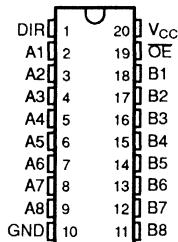
PRODUCT PREVIEW

SN74LVC245
OCTAL BUS TRANSCEIVER
WITH 3-STATE OUTPUTS

NOVEMBER 1993

- **EPIC™ (Enhanced-Performance Implanted CMOS) Sub-Micron Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB) and Thin Shrink Small-Outline (PW) Packages**

DW, DB OR PW PACKAGE
(TOP VIEW)



description

This octal bus transceiver is designed for 2.7 V to 3.6 V V_{CC} operation.

The 74LVC245 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so the buses are effectively isolated.

The 74LVC245 is characterized for operation from -40°C to 85°C .

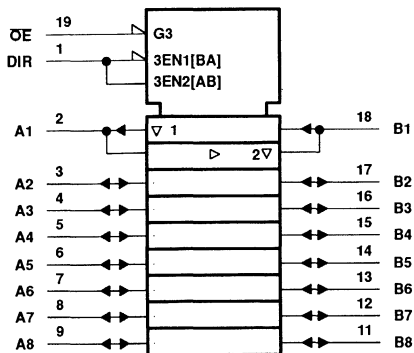
FUNCTION TABLE

INPUTS		OPERATION
\overline{OE}	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

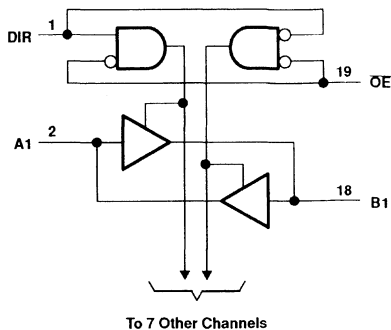
PRODUCT PREVIEW

SN74LVC245
OCTAL BUS TRANSCEIVER
WITH 3-STATE OUTPUTS
 NOVEMBER 1993

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1)	-0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND pins	± 100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DB package	0.65 W
..... DW package	0.85 W
..... PW package	0.6 W
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

PRODUCT PREVIEW

SN74LVC245
OCTAL BUS TRANSCEIVER
WITH 3-STATE OUTPUTS
 NOVEMBER 1993

recommended operating conditions (see Note 2)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2.7		3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2			V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$			0.8	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7\text{ V}$			-12	mA
		$V_{CC} = 3\text{ V}$			-24	
		$V_{CC} = 2.7\text{ V}$			12	
I_{OL}	Low-level output current	$V_{CC} = 2.7\text{ V}$			24	mA
		$V_{CC} = 3\text{ V}$				
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	ns/V
T_A	Operating free-air temperature		-40		85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = -40\text{ TO }85^\circ\text{C}$			UNIT
			MIN	TYP	MAX	
V_{OH}	$I_{OH} = -100\ \mu\text{A}$	V_{CC}^\dagger	$V_{CC} - 0.2$			V
	$I_{OH} = -12\ \text{mA}$	2.7 V	2.2			
	$I_{OH} = -12\ \text{mA}$	3 V	2.4			
	$I_{OH} = -24\ \text{mA}$	3 V	2			
V_{OL}	$I_{OL} = 100\ \mu\text{A}$	V_{CC}^\dagger			0.2	V
	$I_{OL} = 12\ \text{mA}$	2.7 V			0.4	
	$I_{OL} = 24\ \text{mA}$	3 V			0.55	
I_I	$V_I = V_{CC}\text{ or GND}$	3.6 V			±5	μA
I_{OZ}	$V_O = V_{CC}\text{ or GND}$	3.6 V			±10	μA
I_{CC}	$V_I = V_{CC}\text{ or GND}, I_O = 0$	3.6 V			20	μA
ΔI_{CC}	$V_{CC} = 3\text{ V to }3.6\text{ V}$, one input at $V_{CC} - 0.6\text{ V}$, other inputs at $V_{CC}\text{ or GND}$				500	μA
C_i	Control inputs $V_I = V_{CC}\text{ or GND}$	3.3 V			3.5	pF
C_{io}	A or B ports $V_O = V_{CC}\text{ or GND}$	3.3 V			4	pF

$^\dagger V_{CC} = \text{Min to Max}$

‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

switching characteristics over recommended operating free-air temperature range, $C_L = 50\ \text{pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			$V_{CC} = 2.7\text{ V}$		UNIT
			MIN	TYP	MAX	MAX		
t_{pd}	A or B	B or A	1.5		7	8	ns	
t_{en}	OE	A or B	1.5		9	10	ns	
t_{dis}			1.5		8	9		

operating characteristics, $V_{CC} = 3.3\text{ V}, T_A = 25^\circ\text{C}$

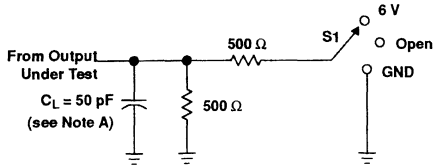
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	25	pF
		Outputs disabled	2	pF

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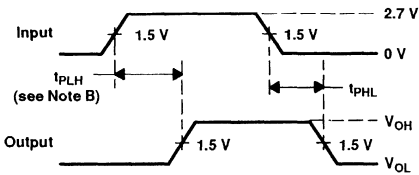
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

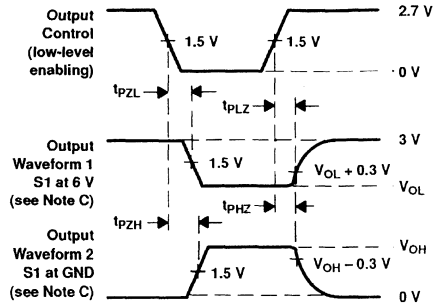


LOAD CIRCUIT FOR OUTPUTS

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_o = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

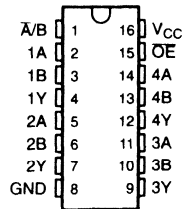
SN74LVC257

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

JANUARY 1993

- **Space-Saving Package Option:**
Shrink Small-Outline Package (DB)
Features EIAJ 0.65-mm Lead Pitch
- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Designed to Facilitate Incident Wave Switching for Line Impedances of 50 Ω or Greater**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline and Thin Shrink Small-Outline Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This quadruple 2-line to 1-line data selector/multiplexer is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC257 is designed to multiplex signals from 4-bit data sources to 4-output data lines in bus-organized systems. The 3-state outputs will not load the data lines when the output-enable ($\overline{\text{OE}}$) input is at a high logic level.

The SN74LVC257 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LVC257 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

OE	INPUTS			OUTPUT
	A/B	A	B	
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

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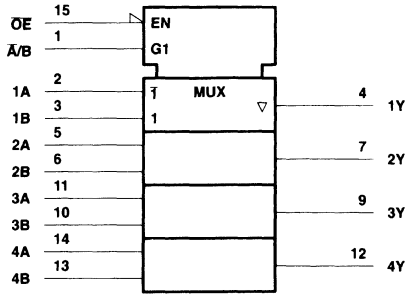


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PRODUCT PREVIEW

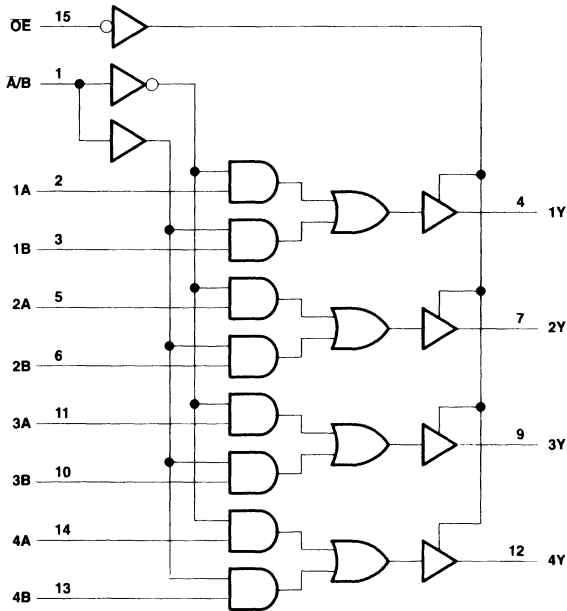
SN74LVC257
QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER
WITH 3-STATE OUTPUTS
 JANUARY 1993

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

SN74LVC257

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

JANUARY 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air):	
DB package	0.5 W
DW package	0.85 W
PW package	0.5 W
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7$ V		-12
		$V_{CC} = 3$ V		-24 [‡]
I_{OL}	Low-level output current	$V_{CC} = 2.7$ V		12
		$V_{CC} = 3$ V		24 [‡]
$\Delta V/\Delta V$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	-40	85	°C

NOTE 3. Unused or floating inputs must be held high or low.

[‡] Current duty cycle ≤ 50%, $f \geq 1$ kHz

PRODUCT PREVIEW

SN74LVC257
QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER
WITH 3-STATE OUTPUTS

JANUARY 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} [†]	MIN	TYP	MAX	UNIT
V _{IK}	I _I = -18 mA	2.7 V			-1.2	V
V _{OH}	I _{OH} = -100 μA	MIN to MAX	V _{CC} - 0.2			V
	I _{OH} = -12 mA	2.7 V	2.2			
		3 V	2.4			
	I _{OH} = -24 mA	3 V	2			
V _{OL}	I _{OL} = 100 μA	MIN to MAX			0.2	V
	I _{OL} = 12 mA	2.7 V			0.4	
	I _{OL} = 24 mA	3 V			0.55	
I _I	V _I = V _{CC} or GND	3.6 V			±5	μA
I _{OZ} [‡]	V _O = V _{CC} or GND	3.6 V			±10	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V			20	μA
ΔI _{CC}	V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC} or GND, One input at V _{CC} - 0.6 V.				500	μA
C _i	V _I = V _{CC} or GND	3.3 V		TBD		pF
C _o	V _O = V _{CC} or GND	3.3 V		TBD		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

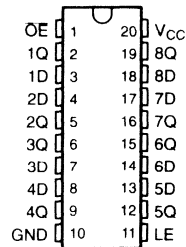
PRODUCT PREVIEW

SN74LVC373 OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

JANUARY 1993

- **Space-Saving Package Option:**
Shrink Small-Outline Package (DB)
Features EIAJ 0.65-mm Lead Pitch
- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Designed to Facilitate Incident Wave Switching for Line Impedances of 50 Ω or Greater**
- **Typical V_{OLP} (Output Ground Bounce)**
< 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- **Typical V_{OHV} (Output V_{OH} Undershoot)**
> 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline and Thin Shrink Small-Outline Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal transparent D-type latch is designed for 2.7-V to 3.6-V V_{CC} operation.

While the latch-enable (LE) input is high, the Q outputs will follow the data (D) inputs. When the latch enable is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable (OE) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (OE) input does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74LVC373 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LVC373 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each latch)

INPUTS			OUTPUT
OE	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

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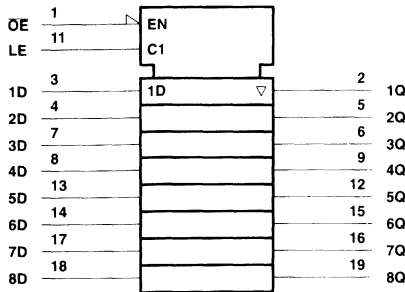


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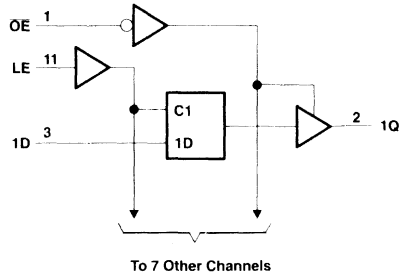
PRODUCT PREVIEW

SN74LVC373
OCTAL TRANSPARENT D-TYPE LATCH
WITH 3-STATE OUTPUTS
 JANUARY 1993

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND pins	± 100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air):	
DB package	0.5 W
DW package	0.85 W
PW package	0.5 W
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V	2	V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V	0.8	V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7$ V	-12	mA
		$V_{CC} = 3$ V	-24 [§]	
I_{OL}	Low-level output current	$V_{CC} = 2.7$ V	12	mA
		$V_{CC} = 3$ V	24 [§]	
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	-40	85	°C

NOTE 3: Unused or floating inputs must be held high or low.

[§] Current duty cycle $\leq 50\%$, $f \geq 1$ kHz

PRODUCT PREVIEW



SN74LVC373
OCTAL TRANSPARENT D-TYPE LATCH
WITH 3-STATE OUTPUTS
JANUARY 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} [†]	MIN	TYP	MAX	UNIT
V _{IK}	I _I = -18 mA	2.7 V			-1.2	V
V _{OH}	I _{OH} = -100 μA	MIN to MAX	V _{CC} - 0.2			V
	I _{OH} = -12 mA	2.7 V	2.2			
	I _{OH} = -24 mA	3 V	2.4			
V _{OL}	I _{OL} = 100 μA	MIN to MAX			0.2	V
	I _{OL} = 12 mA	2.7 V			0.4	
	I _{OL} = 24 mA	3 V			0.55	
I _I	V _I = V _{CC} or GND	3.6 V			±5	μA
I _{OZ}	V _O = V _{CC} or GND	3.6 V			±10	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V			20	μA
ΔI _{CC}	V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND				500	μA
C _i	V _I = V _{CC} or GND	3.3 V			TBD	pF
C _o	V _O = V _{CC} or GND	3.3 V			TBD	pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

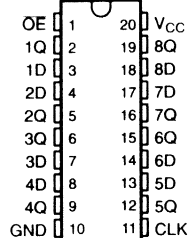
SN74LVC374

OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

JANUARY 1993

- **Space-Saving Package Option:**
Shrink Small-Outline Package (DB)
Features EIAJ 0.65-mm Lead Pitch
- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Designed to Facilitate Incident Wave Switching for Line Impedances of 50 Ω or Greater**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline and Thin Shrink Small-Outline Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal edge-triggered D-type flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC374 features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels that were set up at the data (D) inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components. The output-enable (\overline{OE}) input does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74LVC374 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LVC374 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
\overline{OE}	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

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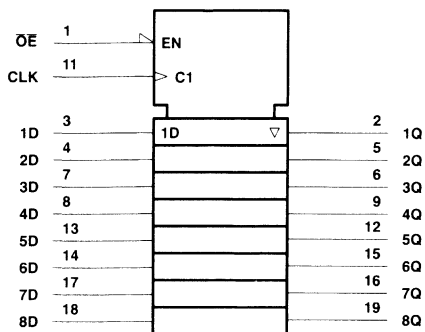
PRODUCT PREVIEW

SN74LVC374

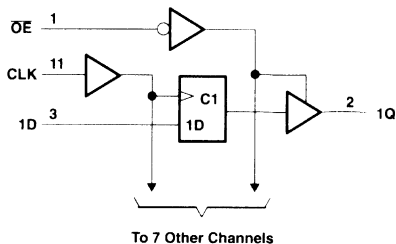
OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

JANUARY 1993

logic symbol



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND pins	± 100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air):	
DB package	0.5 W
DW package	0.85 W
PW package	0.5 W
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.

PRODUCT PREVIEW

SN74LVC374
OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP
WITH 3-STATE OUTPUTS

JANUARY 1993

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$		V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7\text{ V}$	-12	mA
		$V_{CC} = 3\text{ V}$	-24†	
I_{OL}	Low-level output current	$V_{CC} = 2.7\text{ V}$	12	mA
		$V_{CC} = 3\text{ V}$	24†	
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	-40	85	°C

NOTE 3: Unused or floating inputs must be held high or low.

† Current duty cycle $\leq 50\%$, $f \geq 1\text{ kHz}$

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}^\dagger	MIN	TYP	MAX	UNIT
V_{IK}	$I_I = -18\text{ mA}$	2.7 V			-1.2	V
V_{OH}	$I_{OH} = -100\ \mu\text{A}$	MIN to MAX	$V_{CC} - 0.2$			V
	$I_{OH} = -12\text{ mA}$	2.7 V	2.2			
	$I_{OH} = -24\text{ mA}$	3 V	2.4			
V_{OL}	$I_{OL} = 100\ \mu\text{A}$	MIN to MAX			0.2	V
	$I_{OL} = 12\text{ mA}$	2.7 V			0.4	
	$I_{OL} = 24\text{ mA}$	3 V			0.55	
I_I	$V_I = V_{CC}\text{ or GND}$	3.6 V			+5	μA
I_{OZ}	$V_O = V_{CC}\text{ or GND}$	3.6 V			+10	μA
I_{CC}	$V_I = V_{CC}\text{ or GND}, I_O = 0$	3.6 V			20	μA
ΔI_{CC}	$V_{CC} = 3\text{ V to }3.6\text{ V},$ Other inputs at V_{CC} or GND	One input at $V_{CC} - 0.6\text{ V},$			500	μA
C_I	$V_I = V_{CC}\text{ or GND}$	3.3 V		TBD		pF
C_O	$V_O = V_{CC}\text{ or GND}$	3.3 V		TBD		pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

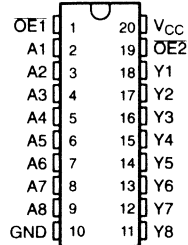
SN74LVC540

OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

JANUARY 1993

- **Space-Saving Package Option:**
Shrink Small-Outline Package (DB)
Features EIAJ 0.65-mm Lead Pitch
- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Designed to Facilitate Incident Wave Switching for Line Impedances of 50 Ω or Greater**
- **Typical V_{OLP} (Output Ground Bounce)**
< 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- **Typical V_{OHV} (Output V_{OH} Undershoot)**
> 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline and Thin Shrink Small-Outline Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal buffer/driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC540 is ideal for driving bus lines or buffer memory address registers. The device features inputs and outputs on opposite sides of the package to facilitate printed-circuit-board layout.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all corresponding outputs are in the high-impedance state.

The SN74LVC540 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LVC540 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

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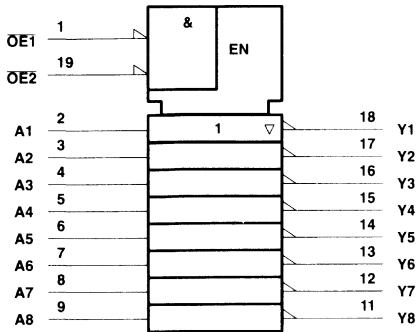
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PRODUCT PREVIEW

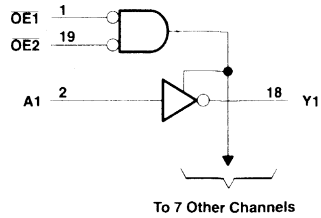
SN74LVC540
OCTAL BUFFER/DRIVER
WITH 3-STATE OUTPUTS

JANUARY 1993

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air):	
DB package	0.5 W
DW package	0.85 W
PW package	0.5 W
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.

PRODUCT PREVIEW

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$		V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7\text{ V}$	-12	mA
		$V_{CC} = 3\text{ V}$	-24†	
I_{OL}	Low-level output current	$V_{CC} = 2.7\text{ V}$	12	mA
		$V_{CC} = 3\text{ V}$	24†	
$\Delta t/v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	-40	85	C

NOTE 3. Unused or floating inputs must be held high or low.

† Current duty cycle < 50%, $f > 1\text{ kHz}$

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC} †	MIN	TYP	MAX	UNIT
V_{IK}	$I_I = -18\text{ mA}$	2.7 V			-1.2	V
V_{OH}	$I_{OH} = -100\ \mu\text{A}$	MIN to MAX	$V_{CC} - 0.2$			V
	$I_{OH} = -12\text{ mA}$	2.7 V	2.2			
	$I_{OH} = -24\text{ mA}$	3 V	2.4			
V_{OL}	$I_{OL} = 100\ \mu\text{A}$	MIN to MAX			0.2	V
	$I_{OL} = 12\text{ mA}$	2.7 V			0.4	
	$I_{OL} = 24\text{ mA}$	3 V			0.55	
I_I	$V_I = V_{CC}\text{ or GND}$	3.6 V			±5	μA
I_{OZ}	$V_O = V_{CC}\text{ or GND}$	3.6 V			±10	μA
I_{CC}	$V_I = V_{CC}\text{ or GND}, I_O = 0$	3.6 V			20	μA
ΔI_{CC}	$V_{CC} = 3\text{ V to }3.6\text{ V},$ Other inputs at V_{CC} or GND	One input at $V_{CC} - 0.6\text{ V},$			500	μA
C_I	$V_I = V_{CC}\text{ or GND}$	3.3 V		TBD		pF
C_O	$V_O = V_{CC}\text{ or GND}$	3.3 V		TBD		pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

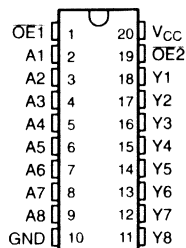
PRODUCT PREVIEW

SN74LVC541 OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

JANUARY 1993

- **Space-Saving Package Option: Shrink Small-Outline Package (DB) Features EIAJ 0.65-mm Lead Pitch**
- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Designed to Facilitate Incident Wave Switching for Line Impedances of 50 Ω or Greater**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline and Thin Shrink Small-Outline Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal buffer/driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC541 is ideal for driving bus lines or buffer memory address registers. The device features inputs and outputs on opposite sides of the package to facilitate printed-circuit-board layout.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all eight outputs are in the high-impedance state.

The SN74LVC541 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LVC541 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

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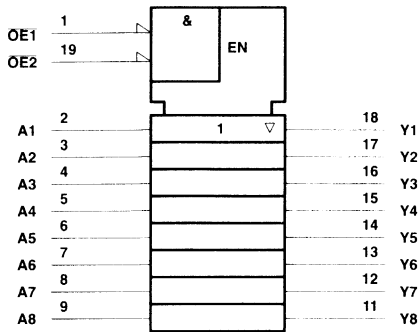
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PRODUCT PREVIEW

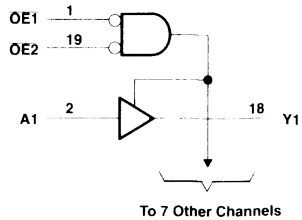
SN74LVC541
OCTAL BUFFER/DRIVER
WITH 3-STATE OUTPUTS

JANUARY 1993

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND pins	± 100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air):	
DB package	0.5 W
DW package	0.85 W
PW package	0.5 W
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.

PRODUCT PREVIEW

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V _{CC}	Supply voltage	2.7	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V		V
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		V
V _I	Input voltage	0	V _{CC}	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2.7 V		-12
		V _{CC} = 3 V		-24 [†]
I _{OL}	Low-level output current	V _{CC} = 2.7 V		12
		V _{CC} = 3 V		24 [†]
ΔV/Δv	Input transition rise or fall rate	0	10	ns/V
T _A	Operating free-air temperature	-40	85	C

NOTE 3: Unused or floating inputs must be held high or low.

[†] Current duty cycle ≤ 50%, f ≥ 1 kHz

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} [‡]	MIN	TYP	MAX	UNIT
V _{IK}	I _I = -18 mA	2.7 V			-1.2	V
V _{OH}	I _{OH} = -100 μA	MIN to MAX	V _{CC} - 0.2			V
	I _{OH} = -12 mA	2.7 V	2.2			
		3 V	2.4			
		3 V	2			
V _{OL}	I _{OL} = 100 μA	MIN to MAX			0.2	V
	I _{OL} = 12 mA	2.7 V			0.4	
	I _{OL} = 24 mA	3 V			0.55	
I _I	V _I = V _{CC} or GND	3.6 V			±5	μA
I _{OZ}	V _O = V _{CC} or GND	3.6 V			±10	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V			20	μA
ΔI _{CC}	V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC} or GND, One input at V _{CC} - 0.6 V.				500	μA
C _I	V _I = V _{CC} or GND	3.3 V	TBD			pF
C _O	V _O = V _{CC} or GND	3.3 V	TBD			pF

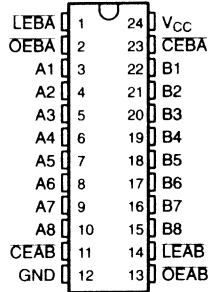
[‡] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

SN74LVC543
OCTAL REGISTERED TRANSCEIVER
WITH 3-STATE OUTPUTS

JANUARY 1993

- **Space-Saving Package Option:**
Shrink Small-Outline Package (DB)
Features EIAJ 0.65-mm Lead Pitch
- **EPIC™ (Enhanced-Performance Implanted CMOS)** Submicron Process
- **Designed to Facilitate Incident Wave Switching for Line Impedances of 50 Ω or Greater**
- **Typical V_{OLP} (Output Ground Bounce)**
 $< 0.8\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$
- **Typical V_{OHV} (Output V_{OH} Undershoot)**
 $> 2\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline and Thin Shrink Small-Outline Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal registered transceiver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC543 contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch-enable (LEAB or LEBA) and output-enable (OEAB or OEBA) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable (CEAB) input must be low in order to enter data from A or to output data from B. If CEAB is low and LEAB is low, the A-to-B latches are transparent; a subsequent low-to-high transition of LEAB puts the A latches in the storage mode. With CEAB and OEAB both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the CEBA, LEBA, and OEBA inputs.

The SN74LVC543 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LVC543 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE†

INPUTS				OUTPUT B
CEAB	LEAB	OEAB	A	
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B_0^\ddagger
L	L	L	L	L
L	L	L	H	H

† A-to-B data flow is shown; B-to-A flow control is the same except that it uses CEBA, LEBA, and OEBA.

‡ Output level before the indicated steady-state input conditions were established.

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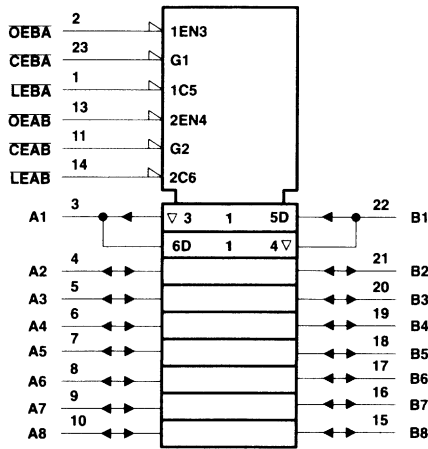
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PRODUCT PREVIEW

SN74LVC543
OCTAL REGISTERED TRANSCEIVER
WITH 3-STATE OUTPUTS

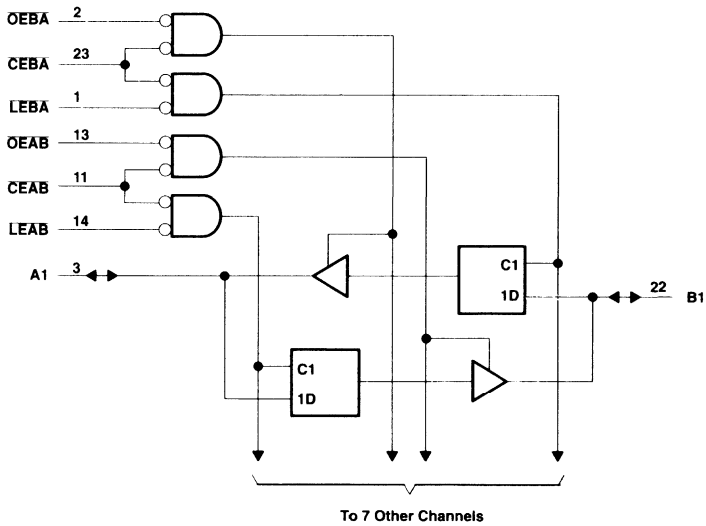
JANUARY 1993

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

SN74LVC543
OCTAL REGISTERED TRANSCEIVER
WITH 3-STATE OUTPUTS

JANUARY 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1)	-0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air):	
DB package	0.5 W
DW package	0.85 W
PW package	0.5 W
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7$ V	-12	mA
		$V_{CC} = 3$ V	-24 [‡]	
I_{OL}	Low-level output current	$V_{CC} = 2.7$ V	12	mA
		$V_{CC} = 3$ V	24 [‡]	
$\Delta V/\Delta t$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	-40	85	°C

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.
[‡] Current duty cycle ≤ 50%. $f \geq 1$ kHz

PRODUCT PREVIEW

SN74LVC543
OCTAL REGISTERED TRANSCEIVER
WITH 3-STATE OUTPUTS

JANUARY 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC} [†]	MIN	TYP	MAX	UNIT
V _{IK}		I _I = -18 mA	2.7 V			-1.2	V
V _{OH}		I _{OH} = -100 μA	MIN to MAX	V _{CC} - 0.2			V
		I _{OH} = -12 mA	2.7 V	2.2			
			3 V	2.4			
			3 V	2			
V _{OL}		I _{OL} = 100 μA	MIN to MAX			0.2	V
		I _{OL} = 12 mA		2.7 V		0.4	
		I _{OL} = 24 mA		3 V		0.55	
I _I		V _I = V _{CC} or GND	3.6 V			±5	μA
I _{OZ} [‡]		V _O = V _{CC} or GND	3.6 V			±10	μA
I _{CC}		V _I = V _{CC} or GND, I _O = 0	3.6 V			20	μA
ΔI _{CC}		V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND				500	μA
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V		TBD		pF
C _{io}	A or B ports	V _O = V _{CC} or GND	3.3 V		TBD		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

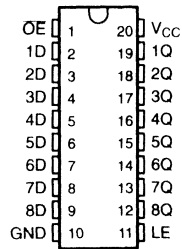
[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

PRODUCT PREVIEW

SN74LVC573
OCTAL TRANSPARENT D-TYPE LATCH
WITH 3-STATE OUTPUTS
JANUARY 1993

- **Space-Saving Package Option: Shrink Small-Outline Package (DB) Features EIAJ 0.65-mm Lead Pitch**
- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Designed to Facilitate Incident Wave Switching for Line Impedances of 50 Ω or Greater**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline and Thin Shrink Small-Outline Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal transparent D-type latch is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC573 features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When the latch enable is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable (OE) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (OE) input does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74LVC573 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LVC573 is characterized for operation from -40°C to 85°C .

PRODUCT PREVIEW

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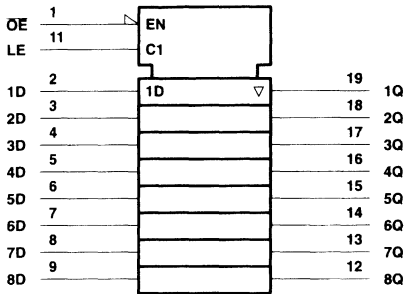
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SN74LVC573
OCTAL TRANSPARENT D-TYPE LATCH
WITH 3-STATE OUTPUTS
 JANUARY 1993

FUNCTION TABLE
 (each latch)

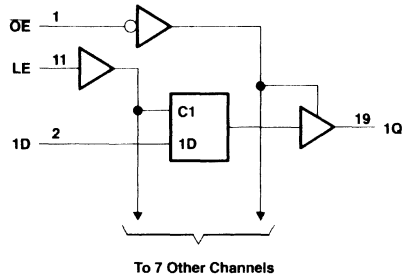
INPUTS			OUTPUT
OE	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q ₀
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air):	
DB package	0.5 W
DW package	0.85 W
PW package	0.5 W
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.

SN74LVC573
OCTAL TRANSPARENT D-TYPE LATCH
WITH 3-STATE OUTPUTS
 JANUARY 1993

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V _{CC}	Supply voltage	2.7	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V		V
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		V
V _I	Input voltage	0	V _{CC}	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2.7 V		-12
		V _{CC} = 3 V		-24†
I _{OL}	Low-level output current	V _{CC} = 2.7 V		12
		V _{CC} = 3 V		24†
Δt/Δv	Input transition rise or fall rate	0	10	ns/V
T _A	Operating free-air temperature	-40	85	°C

NOTE 3. Unused or floating inputs must be held high or low.

† Current duty cycle ≤ 50%, f ≥ 1 kHz

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} †	MIN	TYP	MAX	UNIT
V _{IK}	I _I = -18 mA	2.7 V	MIN to MAX		-1.2	V
V _{OH}	I _{OH} = -100 μA	2.7 V	V _{CC} - 0.2			V
	I _{OH} = -12 mA	2.7 V	2.2			
	I _{OH} = -24 mA	3 V	2.4			
V _{OL}	I _{OL} = 100 μA	3 V	2		0.2	V
	I _{OL} = 12 mA	3 V			0.4	
	I _{OL} = 24 mA	3 V			0.55	
I _I	V _I = V _{CC} or GND	3.6 V			±5	μA
I _{OZ}	V _O = V _{CC} or GND	3.6 V			±10	μA
I _{CC}	V _I = V _{CC} or GND. I _O = 0	3.6 V			20	μA
ΔI _{CC}	V _{CC} = 3 V to 3.6 V. Other inputs at V _{CC} or GND. One input at V _{CC} - 0.6 V.				500	μA
C _I	V _I = V _{CC} or GND	3.3 V			TBD	pF
C _O	V _O = V _{CC} or GND	3.3 V			TBD	pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

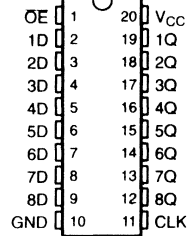
SN74LVC574

OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

JANUARY 1993

- **Space-Saving Package Option:
Shrink Small-Outline Package (DB)
Features EIAJ 0.65-mm Lead Pitch**
- **EPIC™ (Enhanced-Performance Implanted
CMOS) Submicron Process**
- **Designed to Facilitate Incident Wave
Switching for Line Impedances of 50 Ω or
Greater**
- **Typical V_{OLP} (Output Ground Bounce)
< 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **Typical V_{OHV} (Output V_{OH} Undershoot)
> 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **ESD Protection Exceeds 2000 V Per
MIL-STD-883C, Method 3015; Exceeds
200 V Using Machine Model (C = 200 pF,
R = 0)**
- **Latch-Up Performance Exceeds 250 mA
Per JEDEC Standard JESD-17**
- **Package Options Include Plastic
Small-Outline and Thin Shrink
Small-Outline Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal edge-triggered D-type flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC574 features 3-state outputs designed specifically for driving highly capacitive or relatively low impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels that were set up at the data (D) inputs.

A buffered output-enable (OE) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (\overline{OE}) input does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74LVC574 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LVC574 is characterized for operation from -40°C to 85°C .

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PRODUCT PREVIEW

SN74LVC574

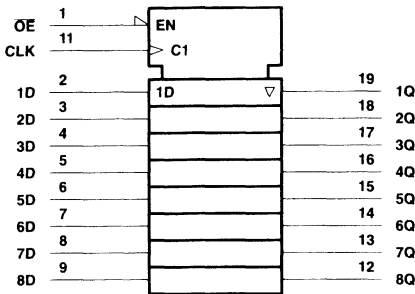
OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

JANUARY 1993

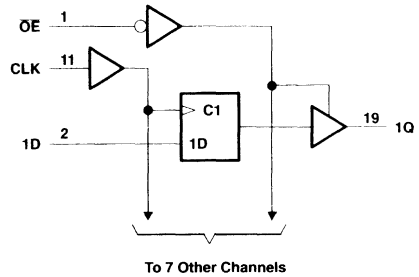
FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
OE	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q ₀
H	X	X	Z

logic symbol†



logic diagram (positive logic)



PRODUCT PREVIEW

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air):	
DB package	0.5 W
DW package	0.85 W
PW package	0.5 W
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.

SN74LVC574
OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP
WITH 3-STATE OUTPUTS
 JANUARY 1993

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$		V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High level output current	$V_{CC} = 2.7\text{ V}$	-12	mA
		$V_{CC} = 3\text{ V}$	-24†	
I_{OL}	Low-level output current	$V_{CC} = 2.7\text{ V}$	12	mA
		$V_{CC} = 3\text{ V}$	24†	
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	-40	85	°C

NOTE 3: Unused or floating inputs must be held high or low.

† Current duty cycle $\leq 50\%$, $f \geq 1\text{ kHz}$

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC} †	MIN	TYP	MAX	UNIT
V_{IK}	$I_I = -18\text{ mA}$	2.7 V			-1.2	V
V_{OH}	$I_{OH} = -100\ \mu\text{A}$	MIN to MAX	$V_{CC} - 0.2$			V
	$I_{OH} = -12\text{ mA}$	2.7 V	2.2			
		3 V	2.4			
	$I_{OH} = -24\text{ mA}$	3 V	2			
V_{OL}	$I_{OL} = 100\ \mu\text{A}$	MIN to MAX			0.2	V
	$I_{OL} = 12\text{ mA}$	2.7 V			0.4	
	$I_{OL} = 24\text{ mA}$	3 V			0.55	
I_I	$V_I = V_{CC}\text{ or GND}$	3.6 V			± 5	μA
I_{OZ}	$V_O = V_{CC}\text{ or GND}$	3.6 V			± 10	μA
I_{CC}	$V_I = V_{CC}\text{ or GND}$, $I_O = 0$	3.6 V			20	μA
ΔI_{CC}	$V_{CC} = 3\text{ V to }3.6\text{ V}$, Other inputs at $V_{CC}\text{ or GND}$	One input at $V_{CC} - 0.6\text{ V}$.			500	μA
C_i	$V_I = V_{CC}\text{ or GND}$	3.3 V		TBD		pF
C_o	$V_O = V_{CC}\text{ or GND}$	3.3 V		TBD		pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

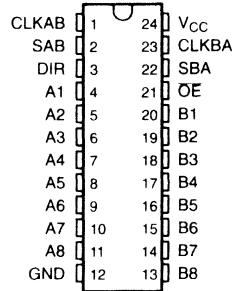
SN74LVC646

OCTAL BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

JANUARY 1993

- **Space-Saving Package Option:**
Shrink Small-Outline Package (DB)
Features EIAJ 0.65-mm Lead Pitch
- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Designed to Facilitate Incident Wave Switching for Line Impedances of 50 Ω or Greater**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline and Thin Shrink Small-Outline Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal bus transceiver and register is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC646 consists of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the SN74LVC646.

Output-enable (OE) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both.

The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The direction control (DIR) determines which bus receives data when OE is low. In the isolation mode (OE high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

The SN74LVC646 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LVC646 is characterized for operation from -40°C to 85°C .

PRODUCT PREVIEW

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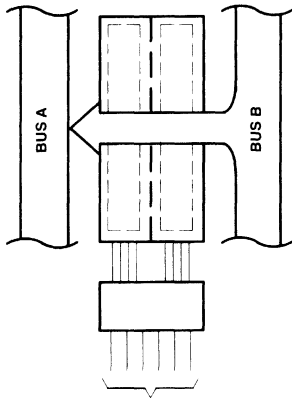


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SN74LVC646
OCTAL BUS TRANSCEIVER AND REGISTER
WITH 3-STATE OUTPUTS

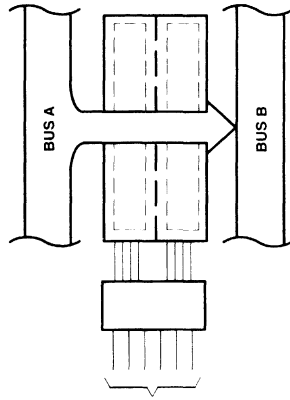
JANUARY 1993

PRODUCT PREVIEW



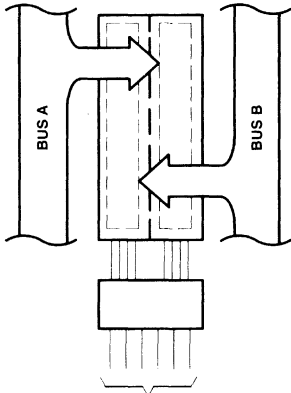
21	3	1	23	2	22
OE	DIR	CLKAB	CLKBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



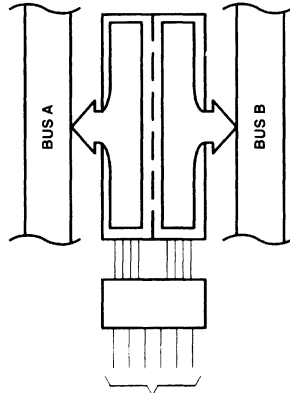
21	3	1	23	2	22
OE	DIR	CLKAB	CLKBA	SAB	SBA
L	L	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



21	3	1	23	2	22
OE	DIR	CLKAB	CLKBA	SAB	SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B



21	3	1	23	2	22
OE	DIR	CLKAB	CLKBA	SAB	SBA
L	L	X	L	X	H
L	H	L	X	H	X

TRANSFER STORED DATA
TO A AND/OR B

Figure 1. Bus-Management Functions

SN74LVC646

OCTAL BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

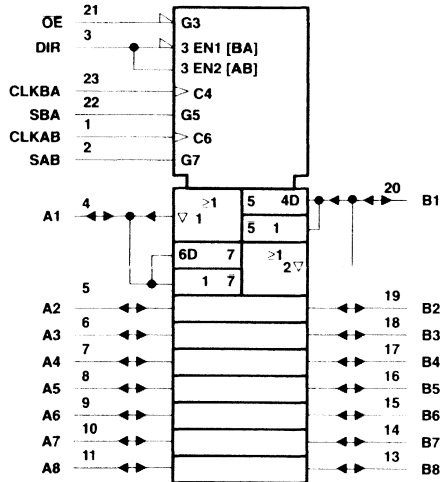
JANUARY 1993

FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION
OE	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	↑	X	X	X	Input	Unspecified [†]	Store A, B unspecified [†]
X	X	X	↑	X	X	Unspecified [†]	Input	Store B, A unspecified [†]
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	L	L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	L	X	H	X	Input	Output	Stored A data to B bus

[†] The data output functions may be enabled or disabled by various signals at the OE and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.

logic symbol[†]

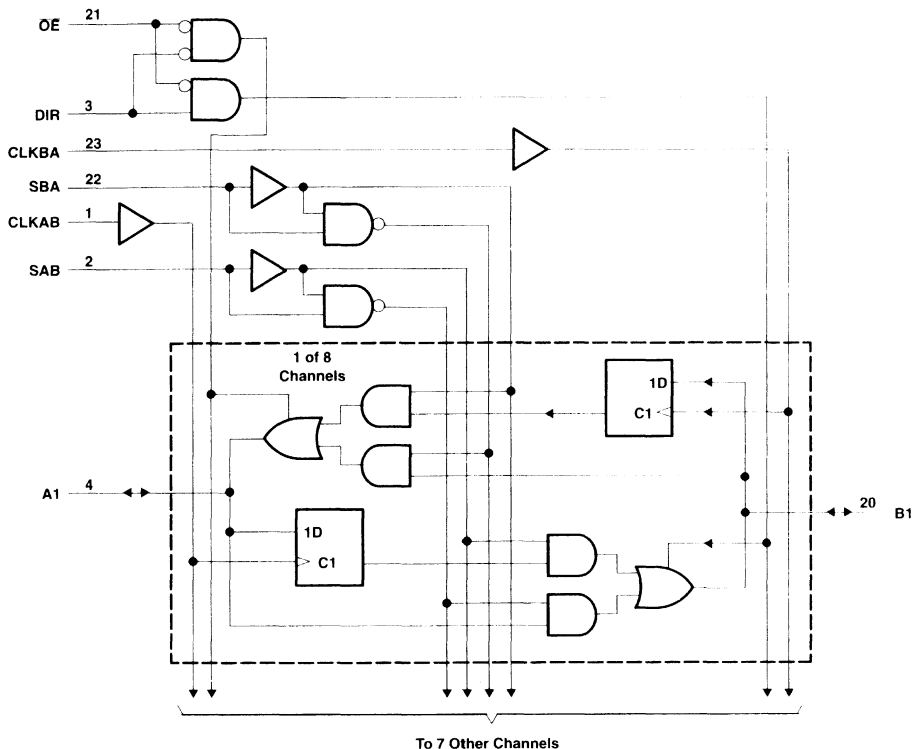


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

SN74LVC646
OCTAL BUS TRANSCEIVER AND REGISTER
WITH 3-STATE OUTPUTS
 JANUARY 1993

logic diagram (positive logic)



PRODUCT PREVIEW

SN74LVC646 OCTAL BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

JANUARY 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1)	-0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air):	
DB package	0.5 W
DW package	0.85 W
PW package	0.5 W
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7$ V		mA
		$V_{CC} = 3$ V		
I_{OL}	Low-level output current	$V_{CC} = 2.7$ V		mA
		$V_{CC} = 3$ V		
$t_{r/f}$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	-40	85	°C

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.

[†] Current duty cycle = 50%, $f > 1$ kHz

PRODUCT PREVIEW

SN74LVC646
OCTAL BUS TRANSCEIVER AND REGISTER
WITH 3-STATE OUTPUTS

JANUARY 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}^{\dagger}	MIN	TYP	MAX	UNIT
V_{IK}		$I_I = -18 \text{ mA}$	2.7 V			-1.2	V
V_{OH}		$I_{OH} = -100 \mu\text{A}$	MIN to MAX	$V_{CC} - 0.2$			V
		$I_{OH} = -12 \text{ mA}$	2.7 V	2.2			
		$I_{OH} = -24 \text{ mA}$	3 V	2.4			
V_{OL}		$I_{OL} = 100 \mu\text{A}$	MIN to MAX			0.2	V
		$I_{OL} = 12 \text{ mA}$	2.7 V			0.4	
		$I_{OL} = 24 \text{ mA}$	3 V			0.55	
I_I		$V_I = V_{CC} \text{ or GND}$	3.6 V			± 5	μA
I_{OZ}^{\ddagger}		$V_O = V_{CC} \text{ or GND}$	3.6 V			+10	μA
I_{CC}		$V_I = V_{CC} \text{ or GND}, I_O = 0$	3.6 V			20	μA
ΔI_{CC}		$V_{CC} = 3 \text{ V to } 3.6 \text{ V},$ Other inputs at $V_{CC} \text{ or GND}$				500	μA
C_i	Control inputs	$V_I = V_{CC} \text{ or GND}$	3.3 V		TBD		pF
C_{IO}	A or B ports	$V_O = V_{CC} \text{ or GND}$	3.3 V		TBD		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

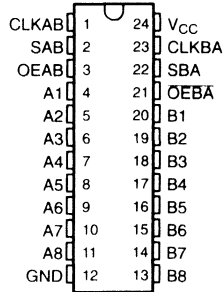
PRODUCT PREVIEW

SN74LVC652 OCTAL BUS TRANSCIVER AND REGISTER WITH 3-STATE OUTPUTS

JANUARY 1993

- **Space-Saving Package Option:**
Shrink Small-Outline Package (DB)
Features EIAJ 0.65-mm Lead Pitch
- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Designed to Facilitate Incident Wave Switching for Line Impedances of 50 Ω or Greater**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline and Thin Shrink Small-Outline Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal bus transceiver and register is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC652 consists of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers.

Output-enable (OEAB and OEBA) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input selects real-time data, and a high input selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the SN74LVC652.

Data on the A or B data bus, or both, can be stored in the internal D-type flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the select- or enable-control pins. When SAB and SBA are in the real-time transfer mode, it is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and OEBA. In this configuration each output reinforces its input. Therefore, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last state.

The SN74LVC652 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LVC652 is characterized for operation from -40°C to 85°C .

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PRODUCT PREVIEW

SN74LVC652
OCTAL BUS TRANSCEIVER AND REGISTER
WITH 3-STATE OUTPUTS

JANUARY 1993

PRODUCT PREVIEW

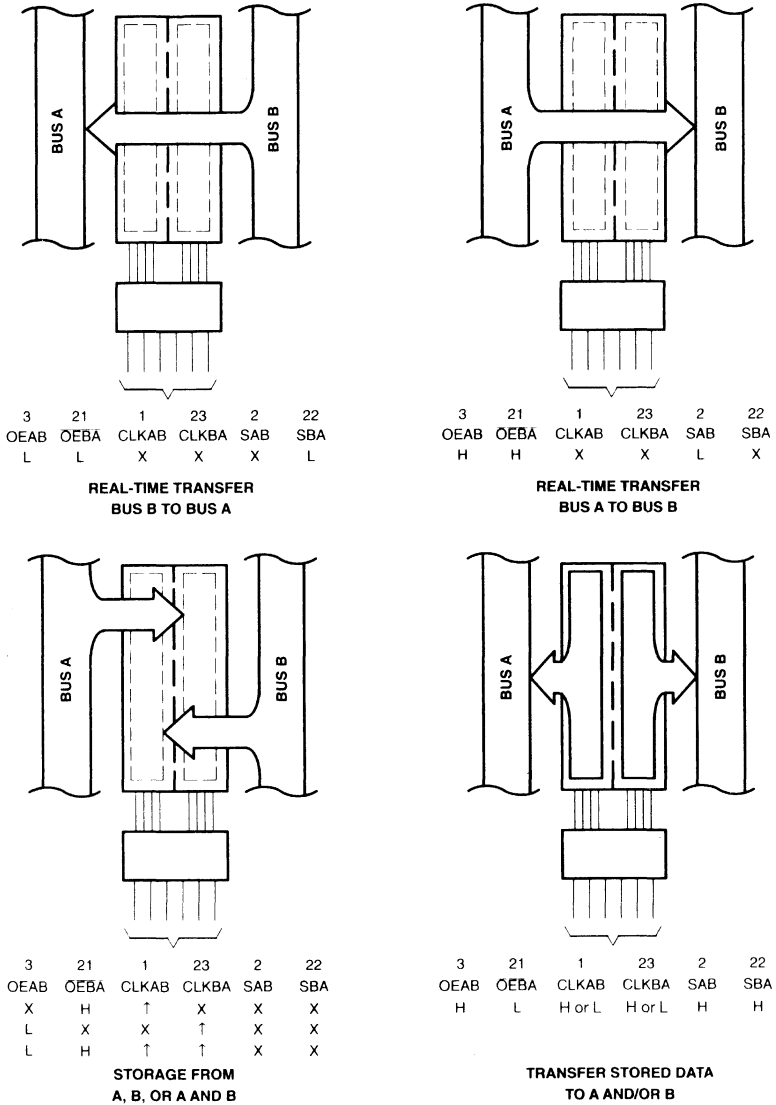


Figure 1. Bus-Management Functions

SN74LVC652 OCTAL BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

JANUARY 1993

FUNCTION TABLE

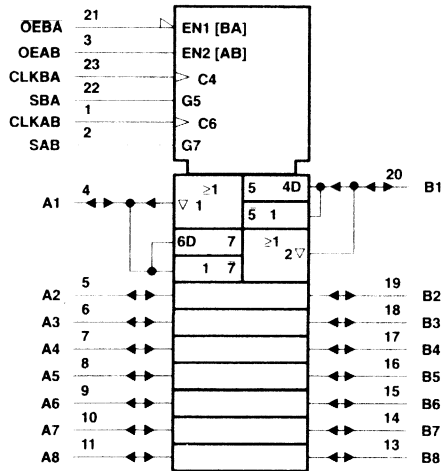
INPUTS						DATA I/O†		OPERATION OR FUNCTION
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
L	H	L	L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	L	X	X	Input	Unspecified‡	Store A, hold B
H	H	↑	↑	X†	X	Input	Output	Store A in both registers
L	X	L	↑	X	X	Unspecified‡	Input	Hold A, store B
L	L	↑	↑	X	X†	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	L	X	H	X	Input	Output	Stored A data to B bus
H	L	L	L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

† The data output functions may be enabled or disabled by a variety of level combinations at the OEAB or OEBA inputs. Data input functions are always enabled, i.e., data at the bus pins is stored on every low-to-high transition on the clock inputs.

‡ Select control = L, clocks can occur simultaneously.

Select control = H, clocks must be staggered in order to load both registers.

logic symbols§



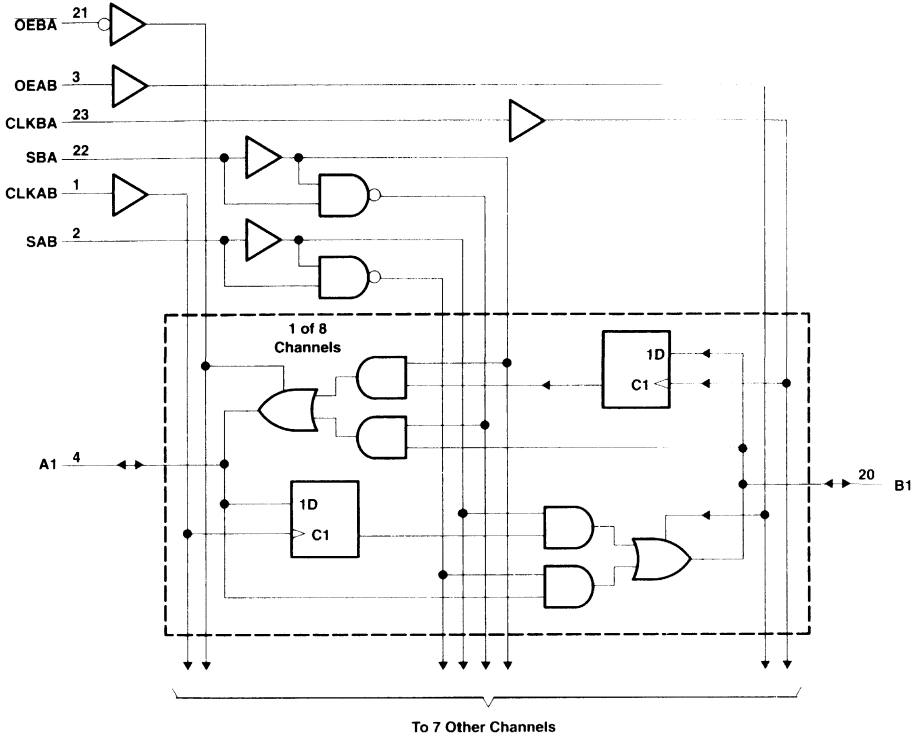
§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

SN74LVC652
OCTAL BUS TRANSCEIVER AND REGISTER
WITH 3-STATE OUTPUTS

JANUARY 1993

logic diagram (positive logic)



PRODUCT PREVIEW

SN74LVC652
OCTAL BUS TRANSCEIVER AND REGISTER
WITH 3-STATE OUTPUTS

JANUARY 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1)	-0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air):	
DB package	0.5 W
DW package	0.85 W
PW package	0.5 W
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES 1 The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2 This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7$ V		-12
		$V_{CC} = 3$ V		-24 [‡]
I_{OL}	Low-level output current	$V_{CC} = 2.7$ V		12
		$V_{CC} = 3$ V		24 [‡]
t_{R}/t_{F}	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	-40	85	°C

NOTE 3. Unused or floating pins (input or I/O) must be held high or low.
[‡] Current duty cycle < 50%, $f > 1$ kHz

PRODUCT PREVIEW

SN74LVC652 OCTAL BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

JANUARY 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} [†]	MIN	TYP	MAX	UNIT
V _{IK}	I _I = -18 mA	2.7 V			-1.2	V
V _{OH}	I _{OH} = -100 μA	MIN to MAX	V _{CC} - 0.2			V
	I _{OH} = -12 mA	2.7 V	2.2			
		3 V	2.4			
V _{OL}	I _{OH} = -24 mA	3 V	2			V
	I _{OL} = 100 μA	MIN to MAX			0.2	
		I _{OL} = 12 mA	2.7 V			
	I _{OL} = 24 mA	3 V			0.55	
I _I	V _I = V _{CC} or GND	3.6 V			1.5	μA
I _{OZ} [‡]	V _O = V _{CC} or GND	3.6 V			+10	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V			20	μA
ΔI _{CC}	V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND				500	μA
C _i	Control inputs, V _I = V _{CC} or GND	3.3 V			TBD	pF
C _o	A or B ports, V _O = V _{CC} or GND	3.3 V			TBD	pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

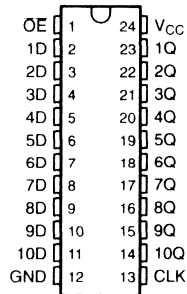
PRODUCT PREVIEW

SN74LVC821 10-BIT BUS-INTERFACE FLIP-FLOP WITH 3-STATE OUTPUTS

MARCH 1993

- **Space-Saving Package Option: Shrink Small-Outline Package (DB) Features EIAJ 0.65-mm Lead Pitch**
- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Designed to Facilitate Incident Wave Switching for Line Impedances of 50 Ω or Greater**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline and Thin Shrink Small-Outline Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This 10-bit bus-interface flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC821 features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

The ten flip-flops are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the device provides true data at the Q outputs.

A buffered output-enable (\overline{OE}) input can be used to place the ten outputs in either a normal logic state (high or low level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (\overline{OE}) input does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74LVC821 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LVC821 is characterized for operation from -40°C to 85°C .

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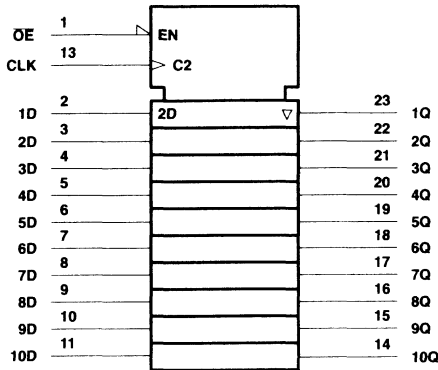
PRODUCT PREVIEW

SN74LVC821
10-BIT BUS-INTERFACE FLIP-FLOP
WITH 3-STATE OUTPUTS
 MARCH 1993

FUNCTION TABLE
 (each flip-flop)

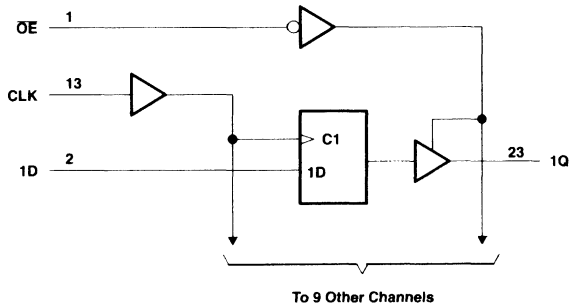
INPUTS			OUTPUT
OE	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q ₀
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

SN74LVC821
10-BIT BUS-INTERFACE FLIP-FLOP
WITH 3-STATE OUTPUTS

MARCH 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DB package	0.5 W
DW package	0.85 W
PW package	0.5 W
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7$ V	-12	mA
		$V_{CC} = 3$ V	-24 [†]	
I_{OL}	Low-level output current	$V_{CC} = 2.7$ V	12	mA
		$V_{CC} = 3$ V	24 [†]	
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	-40	85	°C

NOTE 3: Unused or floating inputs must be held high or low.

[†] Current duty cycle ≤ 50%, $f > 1$ kHz

PRODUCT PREVIEW

SN74LVC821
10-BIT BUS-INTERFACE FLIP-FLOP
WITH 3-STATE OUTPUTS

MARCH 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} [†]	MIN	TYP	MAX	UNIT
V _{IK}	I _I = -18 mA	2.7 V			-1.2	V
V _{OH}	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2			V
	I _{OH} = -12 mA	2.7 V	2.2			
		3 V	2.4			
	I _{OH} = -24 mA	3 V	2			
V _{OL}	I _{OL} = 100 μA	MIN to MAX			0.2	V
	I _{OL} = 12 mA				0.4	
	I _{OL} = 24 mA				0.55	
I _I	V _I = V _{CC} or GND	3.6 V			±5	μA
I _{OZ}	V _O = V _{CC} or GND	3.6 V			±10	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V			20	μA
ΔI _{CC}	V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC} or GND, One input at V _{CC} - 0.6 V.				500	μA
C _i	V _I = V _{CC} or GND	3.3 V		TBD		pF
C _o	V _O = V _{CC} or GND	3.3 V		TBD		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

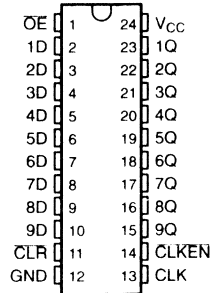
PRODUCT PREVIEW

SN74LVC823 9-BIT BUS-INTERFACE FLIP-FLOP WITH 3-STATE OUTPUTS

MARCH 1993

- **Space-Saving Package Option: Shrink Small-Outline Package (DB)**
Features EIAJ 0.65-mm Lead Pitch
- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Designed to Facilitate Incident Wave Switching for Line Impedances of 50 Ω or Greater**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3 V, T_A = 25^\circ C$**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3 V, T_A = 25^\circ C$**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ($C = 200 pF, R = 0$)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline and Thin Shrink Small-Outline Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This 9-bit bus-interface flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC823 features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

With the clock-enable (CLKEN) input low, the nine D-type edge-triggered flip-flops enter data on low-to-high transitions of the clock. Taking CLKEN high will disable the clock buffer, thus latching the outputs. The SN74LVC823 has noninverting data (D) inputs. Taking the clear (CLR) input low causes the nine Q outputs to go low independently of the clock.

A buffered output-enable (OE) input can be used to place the nine outputs in either a normal logic state (high or low level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (OE) input does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74LVC823 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LVC823 is characterized for operation from $-40^\circ C$ to $85^\circ C$.

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PRODUCT PREVIEW

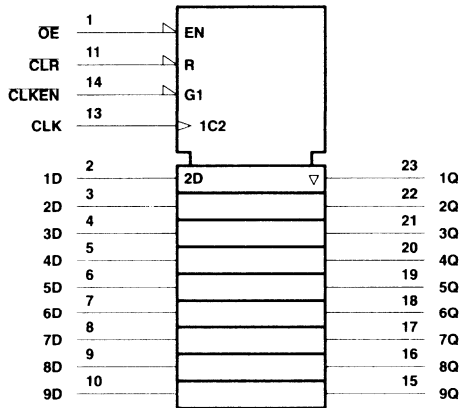
SN74LVC823
9-BIT BUS-INTERFACE FLIP-FLOP
WITH 3-STATE OUTPUTS

MARCH 1993

FUNCTION TABLE
 (each flip-flop)

INPUTS					OUTPUT
OE	CLR	CLKEN	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	H	X	X	Q ₀
H	X	X	X	X	Z

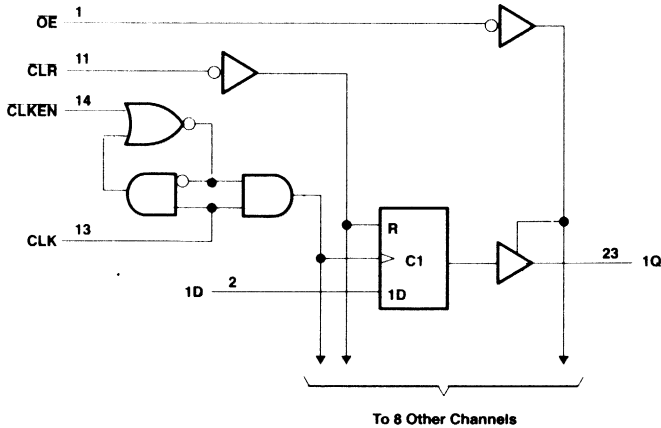
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air):	
DB package	0.5 W
DW package	0.85 W
PW package	0.5 W
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.

PRODUCT PREVIEW

SN74LVC823
9-BIT BUS-INTERFACE FLIP-FLOP
WITH 3-STATE OUTPUTS
 MARCH 1993

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$		V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7\text{ V}$		-12
		$V_{CC} = 3\text{ V}$		-24†
I_{OL}	Low-level output current	$V_{CC} = 2.7\text{ V}$		12
		$V_{CC} = 3\text{ V}$		24†
$\Delta V/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	-40	85	C

NOTE 3: Unused or floating inputs must be held high or low.
 † Current duty cycle $\leq 50\%$, $f \geq 1\text{ kHz}$

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}^\ddagger	MIN	TYP	MAX	UNIT
V_{IK}	$I_I = -18\text{ mA}$	2.7 V			-1.2	V
V_{OH}	$I_{OH} = -100\ \mu\text{A}$	MIN to MAX	$V_{CC} - 0.2$			V
	$I_{OH} = -12\text{ mA}$	2.7 V	2.2			
		3 V	2.4			
	$I_{OH} = -24\text{ mA}$	3 V	2			
V_{OL}	$I_{OL} = 100\ \mu\text{A}$	MIN to MAX			0.2	V
	$I_{OL} = 12\text{ mA}$	2.7 V			0.4	
	$I_{OL} = 24\text{ mA}$	3 V			0.55	
I_I	$V_I = V_{CC}$ or GND	3.6 V			+5	μA
I_{OZ}	$V_O = V_{CC}$ or GND	3.6 V			+10	μA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			20	μA
ΔI_{CC}	$V_{CC} = 3\text{ V to }3.6\text{ V}$, Other inputs at V_{CC} or GND	One input at $V_{CC} - 0.6\text{ V}$,			500	μA
C_i	$V_I = V_{CC}$ or GND	3.3 V		TBD		pF
C_o	$V_O = V_{CC}$ or GND	3.3 V		TBD		pF

‡ For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

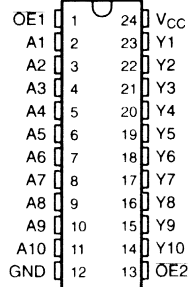
PRODUCT PREVIEW

SN74LVC827 10-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

MARCH 1993

- **Space-Saving Package Option:**
Shrink Small-Outline Package (DB)
Features EIAJ 0.65-mm Lead Pitch
- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Designed to Facilitate Incident Wave Switching for Line Impedances of 50 Ω or Greater**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline and Thin Shrink Small-Outline Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This 10-bit buffer/driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC827 provides a high-performance bus interface for wide data paths or buses carrying parity.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE}1$ or $\overline{OE}2$) input is high, all ten outputs are in the high-impedance state. The SN74LVC827 provides true data at its outputs.

The SN74LVC827 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LVC827 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}1$	$\overline{OE}2$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

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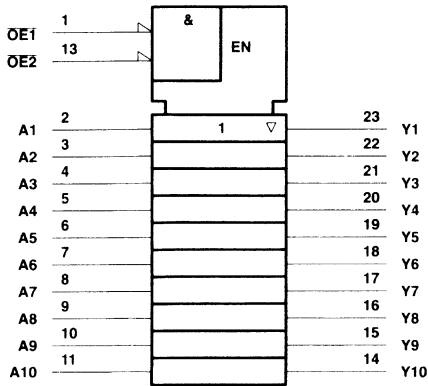


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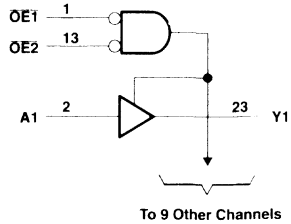
PRODUCT PREVIEW

SN74LVC827
10-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS
 MARCH 1993

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND pins	± 100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air):	
DB package	0.5 W
DW package	0.85 W
PW package	0.5 W
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.

PRODUCT PREVIEW

SN74LVC827
10-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS
MARCH 1993

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V _{CC}	Supply voltage	2.7	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V		V
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		V
V _I	Input voltage	0	V _{CC}	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2.7 V		-12
		V _{CC} = 3 V		-24†
I _{OL}	Low-level output current	V _{CC} = 2.7 V		12
		V _{CC} = 3 V		24†
Δt/Δv	Input transition rise or fall rate	0	10	ns/V
T _A	Operating free-air temperature	-40	85	°C

NOTE 3: Unused or floating inputs must be held high or low.

† Current duty cycle ≤ 50%, f ≤ 1 kHz

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} †	MIN	TYP	MAX	UNIT
V _{IK}	I _I = -18 mA	2.7 V			-1.2	V
V _{OH}	I _{OH} = -100 μA	MIN to MAX	V _{CC} - 0.2			V
	I _{OH} = -12 mA	2.7 V	2.2			
		3 V	2.4			
		3 V	2			
V _{OL}	I _{OL} = 100 μA	MIN to MAX	0.2			V
	I _{OL} = 12 mA	2.7 V	0.4			
	I _{OL} = 24 mA	3 V	0.55			
I _I	V _I = V _{CC} or GND	3.6 V			±5	μA
I _{OZ}	V _O = V _{CC} or GND	3.6 V			±10	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V			20	μA
ΔI _{CC}	V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND				500	μA
C _I	V _I = V _{CC} or GND	3.3 V		TBD		pF
C _O	V _O = V _{CC} or GND	3.3 V		TBD		pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

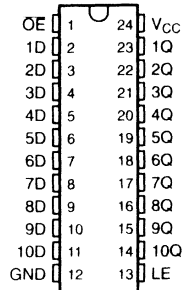
SN74LVC841

10-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS

MARCH 1993

- **Space-Saving Package Option:**
Shrink Small-Outline Package (DB)
Features EIAJ 0.65-mm Lead Pitch
- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Designed to Facilitate Incident Wave Switching for Line Impedances of 50 Ω or Greater**
- **Typical V_{OLP} (Output Ground Bounce)**
< 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- **Typical V_{OHV} (Output V_{OH} Undershoot)**
> 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline and Thin Shrink Small-Outline Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

This 10-bit bus-interface D-type latch is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC841 is designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The ten latches are transparent D-type latches. The device has noninverting data (D) inputs and provides true data at its outputs.

A buffered output-enable (OE) input can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (OE) input does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74LVC841 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LVC841 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

INPUTS			OUTPUT
OE	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

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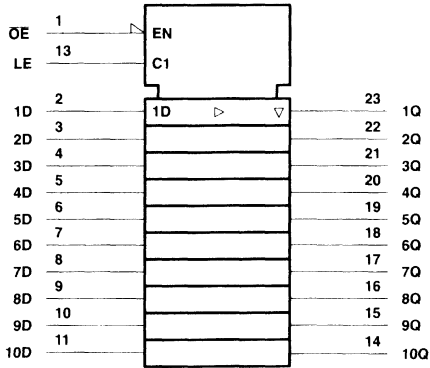


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SN74LVC841
10-BIT BUS-INTERFACE D-TYPE LATCH
WITH 3-STATE OUTPUTS

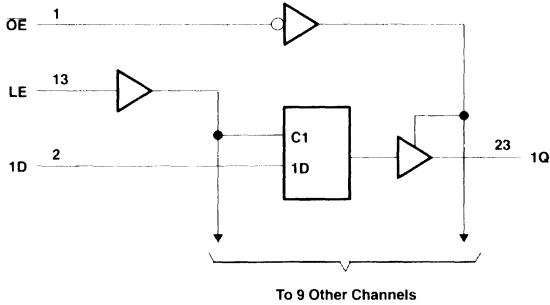
MARCH 1993

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

SN74LVC841
10-BIT BUS-INTERFACE D-TYPE LATCH
WITH 3-STATE OUTPUTS

MARCH 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air):	
DB package	0.5 W
DW package	0.85 W
PW package	0.5 W
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7$ V		-12
		$V_{CC} = 3$ V		-24†
I_{OL}	Low-level output current	$V_{CC} = 2.7$ V		12
		$V_{CC} = 3$ V		24†
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	-40	85	°C

NOTE 3: Unused or floating inputs must be held high or low.

† Current duty cycle ≤ 50%, $f \geq 1$ kHz

PRODUCT PREVIEW

SN74LVC841
10-BIT BUS-INTERFACE D-TYPE LATCH
WITH 3-STATE OUTPUTS

MARCH 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} [†]	MIN	TYP	MAX	UNIT
V _{IK}	I _I = -18 mA	2.7 V			-1.2	V
V _{OH}	I _{OH} = -100 μA	MIN to MAX	V _{CC} - 0.2			V
	I _{OH} = -12 mA	2.7 V	2.2			
	I _{OH} = -24 mA	3 V	2.4			
V _{OL}	I _{OL} = -24 mA	3 V	2			V
	I _{OL} = 100 μA	MIN to MAX	0.2			
	I _{OL} = 12 mA	2.7 V	0.4			
	I _{OL} = 24 mA	3 V	0.55			
I _I	V _I = V _{CC} or GND	3.6 V			±5	μA
I _{OZ}	V _O = V _{CC} or GND	3.6 V			±10	μA
I _{CC}	V _I = V _{CC} or GND. I _O = 0	3.6 V			20	μA
ΔI _{CC}	V _{CC} = 3 V to 3.6 V. One input at V _{CC} - 0.6 V. Other inputs at V _{CC} or GND				500	μA
C _i	V _I = V _{CC} or GND	3.3 V		TBD		pF
C _o	V _O = V _{CC} or GND	3.3 V		TBD		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW



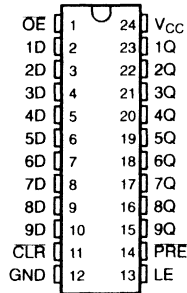
SN74LVC843

9-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS

MARCH 1993

- **Space-Saving Package Option: Shrink Small-Outline Package (DB) Features EIAJ 0.65-mm Lead Pitch**
- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Designed to Facilitate Incident Wave Switching for Line Impedances of 50 Ω or Greater**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline and Thin Shrink Small-Outline Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This 9-bit bus-interface D-type latch is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC843 is designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The nine latches are transparent D-type latches. The device has noninverting data (D) inputs and provides true data at its outputs.

A buffered output-enable (\overline{OE}) input can be used to place the nine outputs in either a normal logic state (high or low levels) or a high-impedance state. The outputs are also in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered-down. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (\overline{OE}) input does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74LVC843 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LVC843 is characterized for operation from -40°C to 85°C .

PRODUCT PREVIEW

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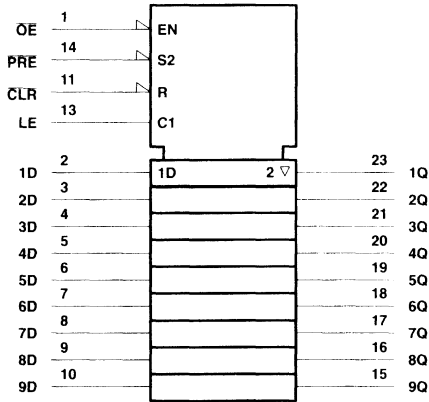
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SN74LVC843
9-BIT BUS-INTERFACE D-TYPE LATCH
WITH 3-STATE OUTPUTS
 MARCH 1993

FUNCTION TABLE

INPUTS					OUTPUT
PRE	CLR	C.E	LE	D	Q
L	X	L	X	X	H
H	L	L	X	X	L
H	H	L	H	L	L
H	H	L	H	H	H
H	H	L	L	X	Q ₀
X	X	H	X	X	Z

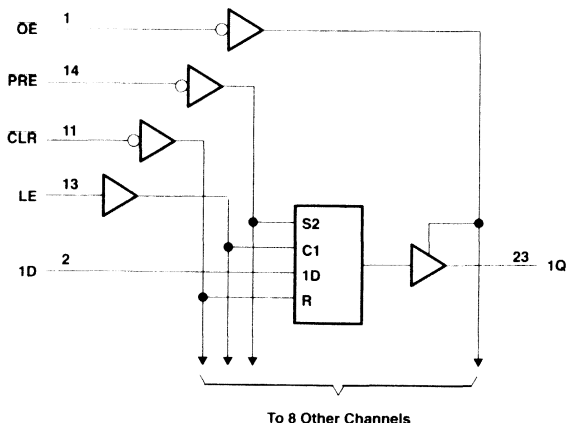
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air):	
DB package	0.5 W
DW package	0.85 W
PW package	0.5 W
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.

PRODUCT PREVIEW

SN74LVC843
9-BIT BUS-INTERFACE D-TYPE LATCH
WITH 3-STATE OUTPUTS

MARCH 1993

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$		V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7\text{ V}$		mA
		$V_{CC} = 3\text{ V}$		
I_{OL}	Low-level output current	$V_{CC} = 2.7\text{ V}$		mA
		$V_{CC} = 3\text{ V}$		
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	-40	85	°C

NOTE 3: Unused or floating inputs must be held high or low.

† Current duty cycle $\leq 50\%$, $f \geq 1\text{ kHz}$

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}^\dagger	MIN	TYP	MAX	UNIT
V_{IK}	$I_I = -18\text{ mA}$	2.7 V			-1.2	V
V_{OH}	$I_{OH} = -100\text{ }\mu\text{A}$	MIN to MAX	$V_{CC} - 0.2$		V	
	$I_{OH} = -12\text{ mA}$	2.7 V	2.2			
	$I_{OH} = -24\text{ mA}$	3 V	2.4			
V_{OL}	$I_{OL} = 100\text{ }\mu\text{A}$	MIN to MAX			0.2	V
	$I_{OL} = 12\text{ mA}$	2.7 V			0.4	
	$I_{OL} = 24\text{ mA}$	3 V			0.55	
I_I	$V_I = V_{CC}$ or GND	3.6 V			± 5	μA
I_{OZ}	$V_O = V_{CC}$ or GND	3.6 V			± 10	μA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			20	μA
ΔI_{CC}	$V_{CC} = 3\text{ V to }3.6\text{ V}$, Other inputs at V_{CC} or GND	One input at $V_{CC} - 0.6\text{ V}$,			500	μA
C_i	$V_I = V_{CC}$ or GND	3.3 V		TBD		pF
C_o	$V_O = V_{CC}$ or GND	3.5 V		TBD		pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW



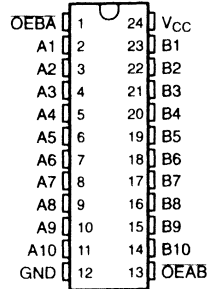
SN74LVC861

10-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

MARCH 1993

- **Space-Saving Package Option: Shrink Small-Outline Package (DB)**
Features EIAJ 0.65-mm Lead Pitch
- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Designed to Facilitate Incident Wave Switching for Line Impedances of 50 Ω or Greater**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline and Thin Shrink Small-Outline Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This 10-bit bus transceiver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC861 is designed for asynchronous communication between data buses. The control function implementation allows for maximum flexibility in timing.

This device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the output-enable (\overline{OEAB} and \overline{OEBA}) inputs.

The SN74LVC861 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LVC861 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

INPUTS		OPERATION
\overline{OEAB}	\overline{OEBA}	
L	H	A data to B bus
H	L	B data to A bus
H	H	Isolation
L	L	Latch A and B (A = B)

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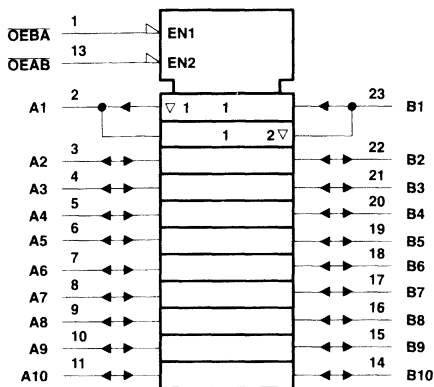
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PRODUCT PREVIEW

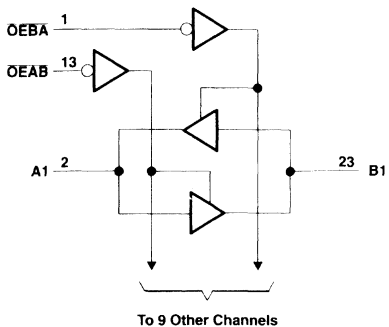
SN74LVC861
10-BIT BUS TRANSCEIVER
WITH 3-STATE OUTPUTS

MARCH 1993

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1)	-0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND pins	± 100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DB package	0.5 W
DW package	0.85 W
PW package	0.5 W
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.
 2. This value is limited to 4.6 V maximum.

PRODUCT PREVIEW

SN74LVC861
10-BIT BUS TRANSCEIVER
WITH 3-STATE OUTPUTS
MARCH 1993

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V _{CC}	Supply voltage	2.7	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V		V
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		V
V _I	Input voltage	0	V _{CC}	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2.7 V		mA
		V _{CC} = 3 V		
I _{OL}	Low-level output current	V _{CC} = 2.7 V		mA
		V _{CC} = 3 V		
Δt/Δv	Input transition rise or fall rate	0	10	ns/V
T _A	Operating free-air temperature	-40	85	°C

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.

† Current duty cycle ≤ 50%, f ≥ 1 kHz

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} †	MIN	TYP	MAX	UNIT
V _{IK}	I _I = -18 mA	2.7 V			-1.2	V
V _{OH}	I _{OH} = -100 μA	MIN to MAX	V _{CC} - 0.2			V
	I _{OH} = -12 mA	2.7 V	2.2			
		3 V	2.4			
	I _{OH} = -24 mA	3 V	2			
V _{OL}	I _{OL} = 100 μA	MIN to MAX			0.2	V
	I _{OL} = 12 mA		2.7 V		0.4	
	I _{OL} = 24 mA		3 V		0.55	
I _I	V _I = V _{CC} or GND	3.6 V			±5	μA
I _{OZ} §	V _O = V _{CC} or GND	3.6 V			±10	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V			20	μA
ΔI _{CC}	V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND				500	μA
C _I	Control inputs	V _I = V _{CC} or GND	3.3 V		TBD	pF
C _{I/O}	A or B ports	V _O = V _{CC} or GND	3.3 V		TBD	pF

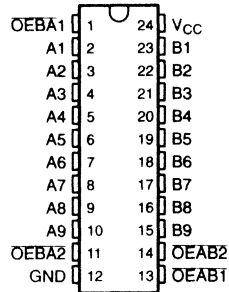
† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

§ For I/O ports, the parameter I_{OZ} includes the input leakage current.

PRODUCT PREVIEW

- **Space-Saving Package Option:**
Shrink Small-Outline Package (DB)
Features EIAJ 0.65-mm Lead Pitch
- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Designed to Facilitate Incident Wave Switching for Line Impedances of 50 Ω or Greater**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline and Thin Shrink Small-Outline Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This 9-bit bus transceiver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC863 is designed for asynchronous communication between data buses. The control function implementation allows for maximum flexibility in timing.

This device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the output-enable (OEAB and OEBA) inputs.

The outputs are in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered down.

The SN74LVC863 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LVC863 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

INPUTS				OPERATION
OEAB1	OEAB2	OEBA1	OEBA2	
L	L	L	L	Latch A and B
L	L	H	X	A to B
L	L	X	H	A to B
H	X	L	L	B to A
X	H	L	L	B to A
H	X	H	X	Isolation
H	X	X	H	
X	H	X	H	
X	H	H	X	

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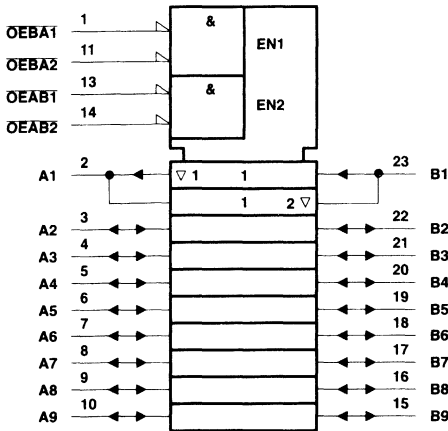
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PRODUCT PREVIEW

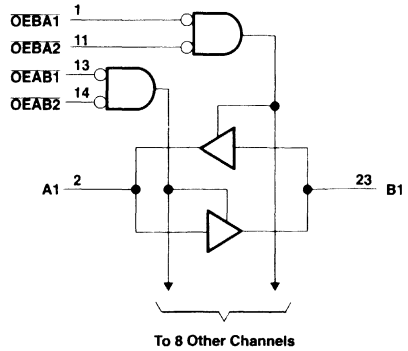
SN74LVC863
9-BIT BUS TRANSCEIVER
WITH 3-STATE OUTPUTS

MARCH 1993

logic symbol†



logic diagram (positive logic)



PRODUCT PREVIEW

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1)	-0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DB package	0.5 W
..... DW package	0.85 W
..... PW package	0.5 W
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V _{CC}	Supply voltage	2.7	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V		V
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		V
V _I	Input voltage	0	V _{CC}	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2.7 V		mA
		V _{CC} = 3 V		
I _{OL}	Low-level output current	V _{CC} = 2.7 V		mA
		V _{CC} = 3 V		
ΔV/Δv	Input transition rise or fall rate	0	10	ns/V
T _A	Operating free-air temperature	-40	85	°C

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.
† Current duty cycle ≤ 50%, f > 1 kHz

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} †	MIN	TYP	MAX	UNIT
V _{IK}	I _I = -18 mA	2.7 V			-1.2	V
V _{OH}	I _{OH} = -100 μA	MIN to MAX	V _{CC} - 0.2			V
	I _{OH} = -12 mA	2.7 V	2.2			
		3 V	2.4			
	I _{OH} = -24 mA	3 V	2			
V _{OL}	I _{OL} = 100 μA	MIN to MAX			0.2	V
	I _{OL} = 12 mA	2.7 V			0.4	
	I _{OL} = 24 mA	3 V			0.55	
I _I	V _I = V _{CC} or GND	3.6 V			±5	μA
I _{OZ} ‡	V _O = V _{CC} or GND	3.6 V			±10	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V			20	μA
ΔI _{CC}	V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND				500	μA
C _I	Control inputs	3.3 V			TBD	pF
C _{IO}	A or B ports	3.3 V			TBD	pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

PRODUCT PREVIEW

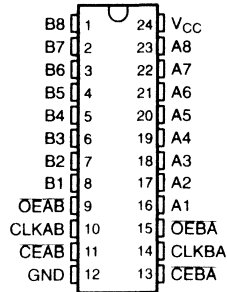
SN74LVC2952

OCTAL BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

JANUARY 1993

- **Space-Saving Package Option:**
Shrink Small-Outline Package (DB)
Features EIAJ 0.65-mm Lead Pitch
- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Designed to Facilitate Incident Wave Switching for Line Impedances of 50 Ω or Greater**
- **Typical V_{OLP} (Output Ground Bounce)**
< 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- **Typical V_{OHV} (Output V_{OH} Undershoot)**
> 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline and Thin Shrink Small-Outline Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal bus transceiver and register is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC2952 consists of two 8-bit back-to-back registers that store data flowing in both directions between two bidirectional buses. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock (CLKAB or CLKBA) input provided that the clock-enable (CEAB or CEBA) input is low. Taking the output-enable (OEAB or OEBA) input low accesses the data on either port.

The SN74LVC2952 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LVC2952 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE†

INPUTS				OUTPUT
CEAB	CLKAB	OEAB	A	B
H	X	L	X	B_0^\ddagger
X	L	L	X	B_0^\ddagger
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	Z

† A-to-B data flow is shown; B-to-A data flow is similar but uses CEBA, CLKBA, and OEBA.

‡ Level of B before the indicated steady-state input conditions were established.

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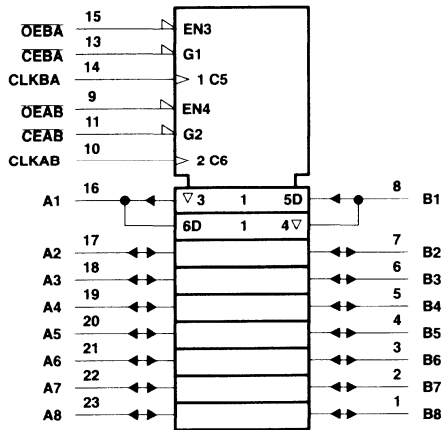
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PRODUCT PREVIEW

SN74LVC2952
OCTAL BUS TRANSCEIVER AND REGISTER
WITH 3-STATE OUTPUTS

JANUARY 1993

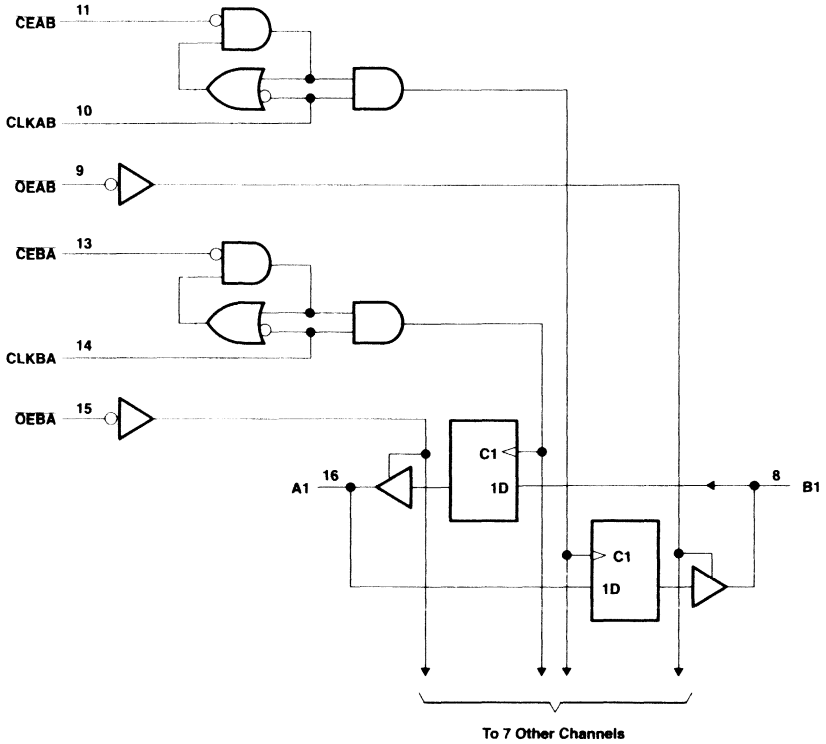
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

logic diagram (positive logic)



PRODUCT PREVIEW

SN74LVC2952
OCTAL BUS TRANSCEIVER AND REGISTER
WITH 3-STATE OUTPUTS

JANUARY 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1)	-0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DB package	0.5 W
..... DW package	0.85 W
..... PW package	0.5 W
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7$ V		mA
		$V_{CC} = 3$ V		
I_{OL}	Low-level output current	$V_{CC} = 2.7$ V		mA
		$V_{CC} = 3$ V		
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	-40	85	°C

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.

† Current duty cycle ≤ 50%, $f \geq 1$ kHz

PRODUCT PREVIEW



SN74LVC2952
OCTAL BUS TRANSCEIVER AND REGISTER
WITH 3-STATE OUTPUTS

JANUARY 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC} [†]	MIN	TYP	MAX	UNIT
V _{IK}		I _I = -18 mA	2.7 V			-1.2	V
V _{OH}		I _{OH} = -100 μA	MIN to MAX	V _{CC} - 0.2			V
		I _{OH} = -12 mA	2.7 V	2.2			
		I _{OH} = -24 mA	3 V	2.4			
V _{OL}		I _{OL} = 100 μA	MIN to MAX			0.2	V
		I _{OL} = 12 mA	2.7 V			0.4	
		I _{OL} = 24 mA	3 V			0.55	
I _I		V _I = V _{CC} or GND	3.6 V			±5	μA
I _{OZ} [‡]		V _O = V _{CC} or GND	3.6 V			±10	μA
I _{CC}		V _I = V _{CC} or GND, I _O = 0	3.6 V			20	μA
ΔI _{CC}		V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND				500	μA
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V		TBD		pF
C _{io}	A or B ports	V _O = V _{CC} or GND	3.3 V		TBD		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

PRODUCT PREVIEW

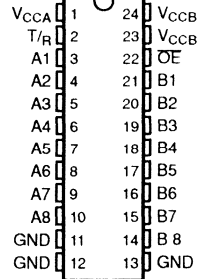
SN74LVC4245

OCTAL BUS TRANSCEIVER, 3.3V TO 5V LEVEL SHIFTER WITH 3-STATE OUTPUTS

AUGUST 1993

- **EPIC™** (Enhanced-Performance Implanted CMOS) Sub-Micron Process
- **Designed to Facilitate Incident Wave Switching for Line Impedances of 50Ω or Greater**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (DW) and Thin Shrink Small-Outline (PW) Packages**

SN74XXX4245 . . . JT PACKAGE
SN74XXX4245 . . . DB, DW, OR NT PACKAGE
(TOP VIEW)



description

The '4245 is an 8-bit transceiver that contains two separate supply rails, B port has V_{CCA} which is set at 5V and the A port has V_{CCB} which is set to operate at 3.3 V. This allows for translation from a 3.3V to a 5 V environment, and visa-versa.

The 'XXX4245 is a noninverting 3-state transceiver designed for synchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

The 74XXX4245 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable (OE) input can be used to disable the device so the buses are effectively isolated.

The 74XXX4245 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

INPUTS		OPERATION
OE	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

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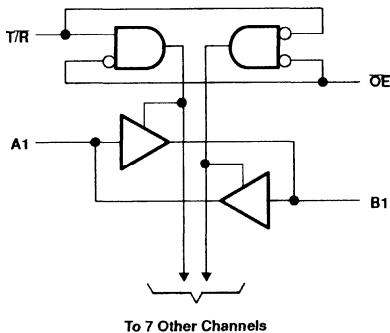
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PRODUCT PREVIEW

SN74LVC4245
OCTAL BUS TRANSCEIVER, 3.3V TO 5V LEVEL SHIFTER
WITH 3-STATE OUTPUTS

AUGUST 1993

logic symbol | logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range for V_{CCA} at 5V (unless otherwise noted)[†]

Supply voltage range, V_{CC1}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to $V_{CC1} + 0.5$ V
Output voltage range, V_O (see Note 1)	-0.5 V to $V_{CC1} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC1}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC1}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC1})	± 50 mA
Continuous current through V_{CC1} or GND pins	± 400 mA

absolute maximum ratings over operating free-air temperature range for V_{CCB} at 3.3V (unless otherwise noted)

Supply voltage range, V_{CC2}	-0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1)	-0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Note 1), (see Note 2)	-0.5 V to $V_{CC2} + 0.5$ V
Output voltage range, V_O (see Note 1), (see Note 2)	-0.5 V to $V_{CC2} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC2}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC2} or GND pins	± 100 mA

absolute maximum ratings over operating free-air temperature range for V_{CCA} at 5V or for V_{CCB} at 3.3V (unless otherwise noted)[†]

Maximum power package dissipation at $T_A = 55^\circ\text{C}$ (in still air): DGG	0.6 W
..... DL	0.85 W
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

NOTE 2: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

NOTE 3: This value is limited to 4.6 V maximum.

PRODUCT PREVIEW



SN74LVC4245
OCTAL BUS TRANSCEIVER, 3.3V TO 5V LEVEL SHIFTER
Header line 3

AUGUST 1993

recommended operating conditions for V_{CCA} at 5V (see Note 2)

		74XCXX4245			UNIT
		MIN	NOM	MAX	
V_{CCA}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage	0.8			V
V_I	Input voltage	0	V_{CCA}		V
V_O	Output voltage	0	V_{CCA}		V
I_{OH}	High-level output current				mA
I_{OL}	Low-level output current				mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10		ns/V
T_A	Operating free-air temperature	-40	85		°C

NOTE 4: Unused or floating pins (input or I/O) must be held high or low.

recommended operating conditions for V_{CCB} at 3.3V (see Note 3)

		MIN	NOM	MAX	UNIT
V_{CCB}	Supply voltage	2.7		3.6	V
V_{IH}	High-level input voltage	$V_{CCB} = 2.7 \text{ V to } 3.6 \text{ V}$			V
V_{IL}	Low-level input voltage	$V_{CCB} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	V
V_I	Input voltage	0	V_{CCB}		V
V_O	Output voltage	0	V_{CCB}		V
I_{OH}	High-level output current	$V_{CCB} = 2.7 \text{ V}$			mA
		$V_{CCB} = 3 \text{ V}$			
I_{OL}	Low-level output current	$V_{CCB} = 2.7 \text{ V}$			mA
		$V_{CCB} = 3 \text{ V}$			
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10		ns/V
T_A	Operating free-air temperature	-40	85		°C

NOTE 5: Unused or floating pins (input or I/O) must be held high or low.

§ Current duty cycle $\leq 50\%$, $f \geq 1 \text{ kHz}$

PRODUCT PREVIEW

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SN74LVC4245
OCTAL BUS TRANSCEIVER, 3.3V TO 5V LEVEL SHIFTER
WITH 3-STATE OUTPUTS

AUGUST 1993

electrical characteristics over recommended operating free-air temperature range for V_{CCA} at 5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			74LVC4245		UNIT
				MIN	TYP	MAX	MIN	MAX	
V_{OH}		$I_{OH} = -50 \mu\text{A}$	4.5 V	4.4		4.4		V	
			5.5 V	5.4		5.4			
	$I_{OH} = -24 \text{ mA}$	4.5 V	3.94		3.8				
		5.5 V	4.94		4.8				
	$I_{OH} = -50 \text{ mA}^\dagger$	5.5 V							
$I_{OH} = -75 \text{ mA}^\dagger$	5.5 V			3.85					
V_{OL}		$I_{OL} = 50 \mu\text{A}$	4.5 V		0.1	0.1	V		
			5.5 V		0.1	0.1			
	$I_{OL} = -24 \text{ mA}$	4.5 V		0.36	0.44				
		5.5 V		0.36	0.44				
	$I_{OL} = 50 \text{ mA}^\dagger$	5.5 V							
$I_{OL} = 75 \text{ mA}^\dagger$	5.5 V								
I_I	Control inputs	$V_I = V_{CC}$ or GND	5.5 V				μA		
I_{OZ}^\ddagger	A or B ports	$V_O = V_{CC}$ or GND	5.5 V				μA		
I_{CC}		$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V				μA		
ΔI_{CC}^\S		One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V				mA		
C_i	Control inputs	$V_I = V_{CC}$ or GND	5 V				pF		
C_{iO}	A or B ports	$V_O = V_{CC}$ or GND	5 V				pF		

Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

[†] For I/O ports, the parameter I_{OZ} includes the input leakage current.

[§] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC} .

For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

PRODUCT PREVIEW

SN74LVC4245
OCTAL BUS TRANSCEIVER, 3.3V TO 5V LEVEL SHIFTER
WITH 3-STATE OUTPUTS

AUGUST 1993

electrical characteristics over recommended operating free-air temperature range for V_{CCB} at 3.3V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = -40 \text{ TO } 85^\circ\text{C}$			UNIT
			MIN	TYP	MAX	
V_{IK}	$I_I = -18 \text{ mA}$	2.7 V			-1.2	V
V_{OH}	$I_{OH} = -100 \mu\text{A}$	V_{CC}^\dagger	$V_{CC} - 0.2$			V
	$I_{OH} = -12 \text{ mA}$	2.7 V	2.2			
	$I_{OH} = -12 \text{ mA}$	3 V	2.4			
	$I_{OH} = -24 \text{ mA}$	3 V	2			
V_{OL}	$I_{OL} = 100 \mu\text{A}$	V_{CC}^\dagger	0.2			V
	$I_{OL} = 12 \text{ mA}$	2.7 V	0.4			
	$I_{OL} = 24 \text{ mA}$	3 V	0.55			
I_I	$V_I = V_{CC}$ or GND	3.6 V				μA
I_{OZ}	$V_O = V_{CC}$ or GND	3.6 V				μA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V				μA
ΔI_{CC}	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$, one input at $V_{CC} - 0.6 \text{ V}$, other inputs at V_{CC} or GND					μA
C_i	Control inputs $V_I = V_{CC}$ or GND	3.3 V	TBD			pF
C_{io}	A or B ports $V_O = V_{CC}$ or GND	3.3 V	TBD			pF

$V_{CC} = \text{Min to Max}$

† For I/O ports, the parameter I_{OZ} includes the input leakage current.

switching characteristics over recommended operating free-air temperature range, $V_{CCA} = 5 \text{ V} \pm 0.5 \text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			74LVC4245		UNIT
			MIN	TYP	MAX	MIN	MAX	
f_{max}								MHz
t_{pd}	A or B	B or A						ns
t_{en}	OEBA or OEAB	A or B						ns
t_{dis}								

operating characteristics, $V_{CC2} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	$C_L = 50 \text{ pF}$, $f = 1 \text{ MHz}$		pF
		Outputs disabled			

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SN74LVC4245
OCTAL BUS TRANSCEIVER, 3.3V TO 5V LEVEL SHIFTER
WITH 3-STATE OUTPUTS

AUGUST 1993

switching characteristics over recommended operating free-air temperature range, for V_{CCB} at 3.3V, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3 V \pm 0.3 V$			$V_{CC} = 2.7 V$	UNIT
			MIN	TYP	MAX	MAX	
t_{pd}	A or B	B or A					ns
t_{en}	OE	A or B					ns
t_{dis}							

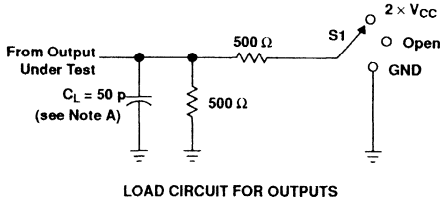
operating characteristics, $V_{CCB} = 3.3 V$, $T_A = 25^\circ C$

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	$C_L = 50$ pF, $f = 10$ MHz		pF
		Outputs disabled			

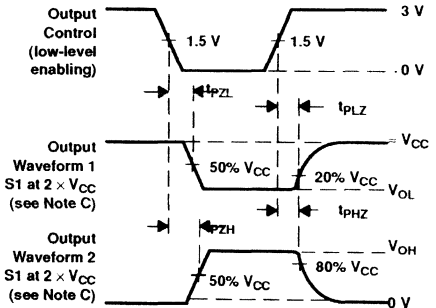
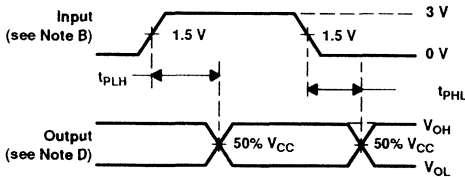
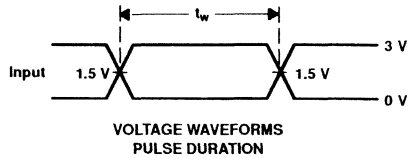
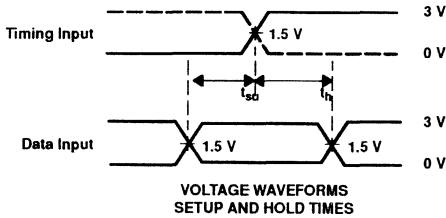
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

$V_{CCA} = 5\text{ V}$



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND



NOTES: A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10\text{ MHz}$, $Z_o = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. The outputs are measured one at a time with one transition per measurement.

PRODUCT PREVIEW

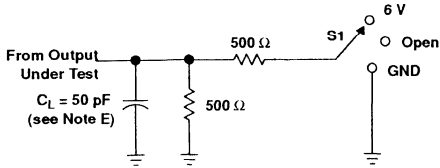
SN74LVC4245
OCTAL BUS TRANSCEIVER, 3.3V TO 5V LEVEL SHIFTER
WITH 3-STATE OUTPUTS

AUGUST 1993

PARAMETER MEASUREMENT INFORMATION

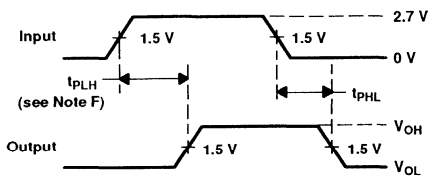
PARAMETER MEASUREMENT INFORMATION, CONTINUED

$V_{CCB} = 3.3V$

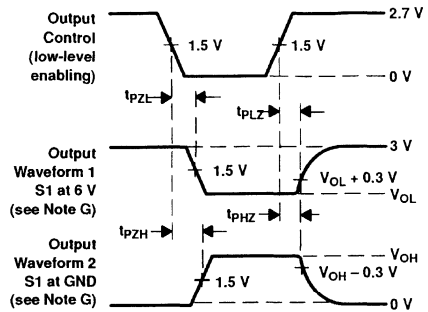


LOAD CIRCUIT FOR OUTPUTS

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: E. C_L includes probe and jig capacitance.

F. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$, $t_r \leq 3$ ns, $t_f \leq 3$ ns. For testing pulse duration: $t_w = t_r = 1$ to 3 ns. Pulse polarity can be either high-to-low-to-high or low-to-high-to-low.

G. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

H. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

SN74LVC16240
16-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS
NOVEMBER 1993

- Member of the Texas Instruments *Widebus™* Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Designed to Facilitate Incident Wave Switching for Line Impedances of 50 Ω or Greater
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages

description

This 16-bit buffer/driver is designed for 2.7-V to 3.6-V V_{CC} operation.

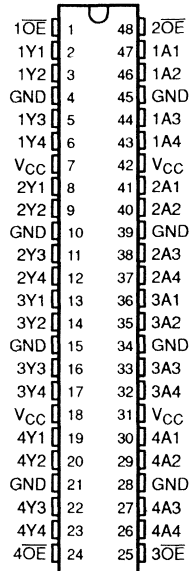
The SN74LVC16240 is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. It provides inverting outputs and symmetrical \overline{OE} (active-low output-enable) inputs.

The SN74LVC16240 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74LVC16240 is characterized for operation from -40°C to 85°C .

DGG OR DL PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each 4-bit buffer)

INPUTS		OUTPUT
\overline{OE}	A	Y
L	H	L
L	L	H
H	X	Z

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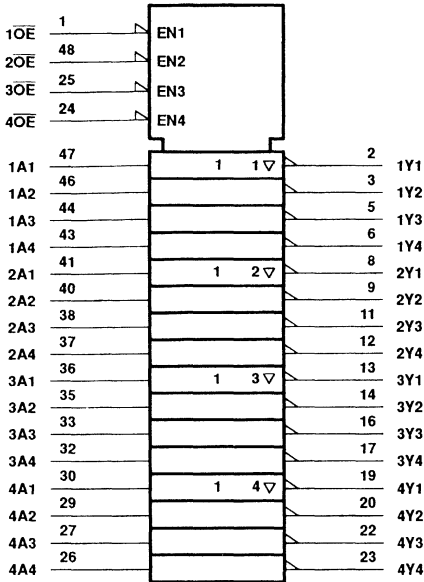


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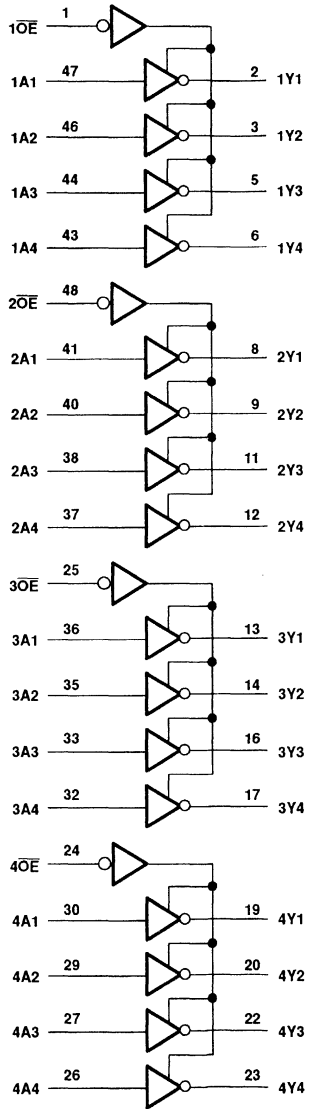
PRODUCT PREVIEW

SN74LVC16240
16-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS
 NOVEMBER 1993

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

SN74LVC16240
16-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS
 NOVEMBER 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DGG package	0.8 W
DL package	0.85 W
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7$ V	-12	mA
		$V_{CC} = 3$ V	-24‡	
I_{OL}	Low-level output current	$V_{CC} = 2.7$ V	12	mA
		$V_{CC} = 3$ V	24‡	
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	-40	85	°C

NOTE 3: Unused or floating inputs must be held high or low.

‡ Current duty cycle ≤ 50%, $f \geq 1$ kHz

PRODUCT PREVIEW

SN74LVC16240
16-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS
 NOVEMBER 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} †	MIN	TYP	MAX	UNIT
V _{IK}	I _I = -18 mA	2.7 V			-1.2	V
V _{OH}	I _{OH} = -100 µA	MIN to MAX	V _{CC} -0.2			V
	I _{OH} = -12 mA	2.7 V	2.2			
		3 V	2.4			
	I _{OH} = -24 mA	3 V	2			
V _{OL}	I _{OL} = 100 µA	MIN to MAX			0.2	V
	I _{OL} = 12 mA	2.7 V			0.4	
	I _{OL} = 24 mA	3 V			0.55	
I _I	V _I = V _{CC} or GND	3.6 V			±5	µA
I _{OZ}	V _O = V _{CC} or GND	3.6 V			±10	µA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V			20	µA
ΔI _{CC}	V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND				500	µA
C _i	V _I = V _{CC} or GND	3.3 V				pF
C _o	V _O = V _{CC} or GND	3.3 V				pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

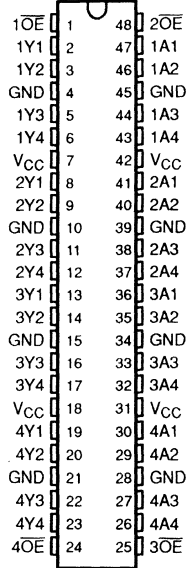
PRODUCT PREVIEW

SN74LVC16244
16-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS

NOVEMBER 1993

- Member of the Texas Instruments *Widebus™* Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Designed to Facilitate Incident Wave Switching for Line Impedances of 50 Ω or Greater
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages

DGG OR DL PACKAGE
(TOP VIEW)



description

This 16-bit buffer/driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC16244 is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. It provides true outputs and symmetrical \overline{OE} (active-low output-enable) inputs.

The SN74LVC16244 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74LVC16244 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each 4-bit buffer)

INPUTS		OUTPUT
\overline{OE}	A	Y
L	H	H
L	L	L
H	X	Z

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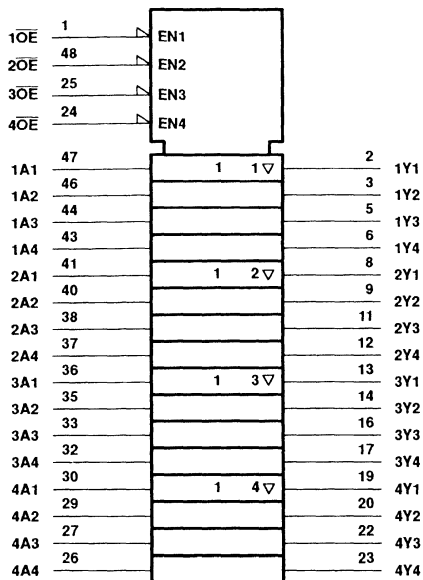


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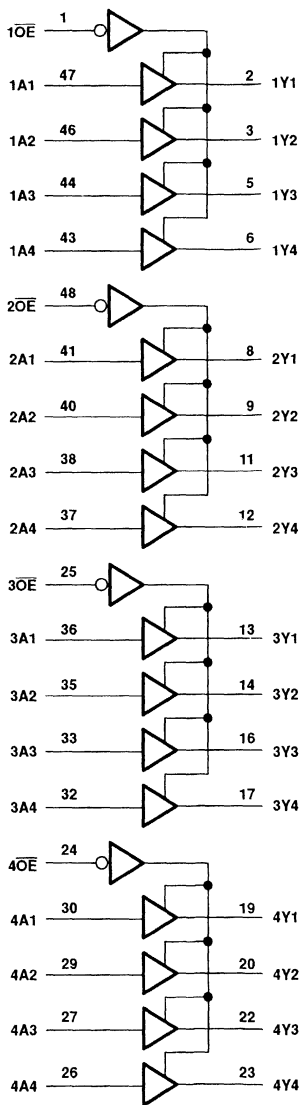
PRODUCT PREVIEW

SN74LVC16244
16-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS
 NOVEMBER 1993

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

SN74LVC16244
16-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS
 NOVEMBER 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DGG package	0.8 W
DL package	0.85 W
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7$ V	-12	mA
		$V_{CC} = 3$ V	-24‡	
I_{OL}	Low-level output current	$V_{CC} = 2.7$ V	12	mA
		$V_{CC} = 3$ V	24‡	
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	-40	85	°C

NOTE 3: Unused or floating inputs must be held high or low.

‡ Current duty cycle ≤ 50%, $f \geq 1$ kHz

PRODUCT PREVIEW

SN74LVC16244
16-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS
 NOVEMBER 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}^\dagger	MIN	TYP	MAX	UNIT
V_{IK}	$I_I = -18 \text{ mA}$	2.7 V			-1.2	V
V_{OH}	$I_{OH} = -100 \mu\text{A}$	MIN to MAX	$V_{CC} - 0.2$			V
	$I_{OH} = -12 \text{ mA}$	2.7 V	2.2			
		3 V	2.4			
	$I_{OH} = -24 \text{ mA}$	3 V	2			
V_{OL}	$I_{OL} = 100 \mu\text{A}$	MIN to MAX			0.2	V
	$I_{OL} = 12 \text{ mA}$		2.7 V		0.4	
	$I_{OL} = 24 \text{ mA}$		3 V		0.55	
I_I	$V_I = V_{CC} \text{ or GND}$	3.6 V			± 5	μA
I_{OZ}	$V_O = V_{CC} \text{ or GND}$	3.6 V			± 10	μA
I_{CC}	$V_I = V_{CC} \text{ or GND}, I_O = 0$	3.6 V			20	μA
ΔI_{CC}	$V_{CC} = 3 \text{ V to } 3.6 \text{ V},$ Other inputs at V_{CC} or GND One input at $V_{CC} - 0.6 \text{ V},$				500	μA
C_i	$V_I = V_{CC} \text{ or GND}$	3.3 V				pF
C_o	$V_O = V_{CC} \text{ or GND}$	3.3 V				pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

SN74LVC16245 16-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

NOVEMBER 1993

- Member of the Texas Instruments *Widebus™* Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Designed to Facilitate Incident Wave Switching for Line Impedances of 50 Ω or Greater
- Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages

description

This 16-bit (dual-octal) noninverting bus transceiver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC16245 is designed for asynchronous communication between data buses. The control function implementation minimizes external timing requirements.

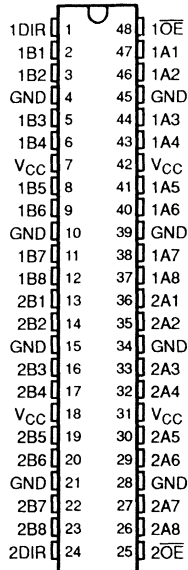
This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so that the buses are effectively isolated.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVC16245 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74LVC16245 is characterized for operation from -40°C to 85°C .

DGG OR DL PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
\overline{OE}	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

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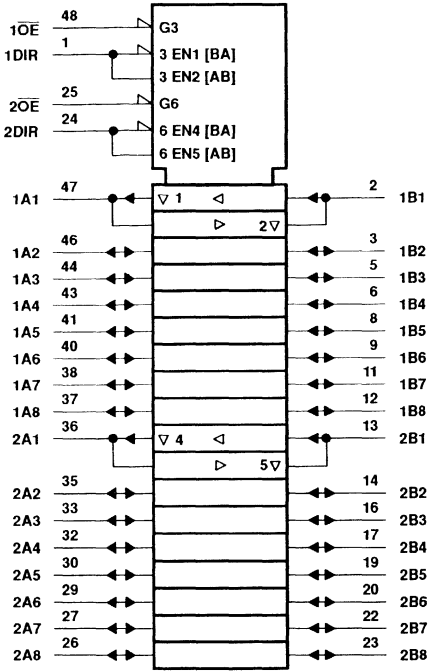
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PRODUCT PREVIEW

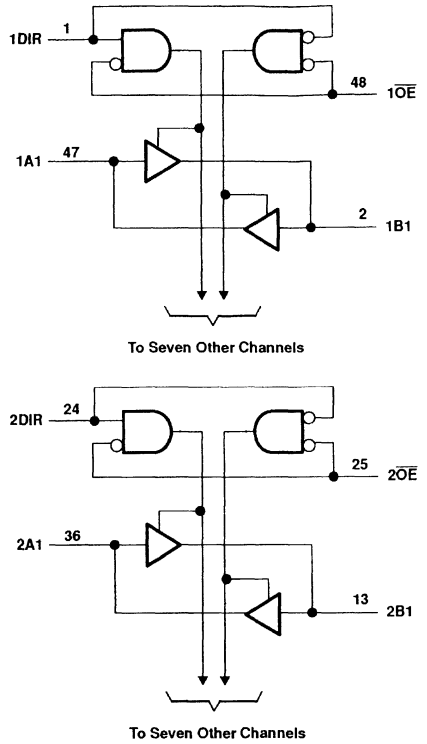
SN74LVC16245
16-BIT BUS TRANSCEIVER
WITH 3-STATE OUTPUTS
 NOVEMBER 1993

PRODUCT PREVIEW

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN74LVC16245
16-BIT BUS TRANSCEIVER
WITH 3-STATE OUTPUTS

NOVEMBER 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1)	-0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DGG package	0.8 W
DL package	0.85 W
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7$ V		mA
		$V_{CC} = 3$ V		
I_{OL}	Low-level output current	$V_{CC} = 2.7$ V		mA
		$V_{CC} = 3$ V		
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_A	Operating free-air temperature	-40	85	°C

NOTE 3: Unused or floating control pins must be held high or low.

PRODUCT PREVIEW

SN74LVC16245
16-BIT BUS TRANSCEIVER
WITH 3-STATE OUTPUTS

NOVEMBER 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC} †	MIN	TYP	MAX	UNIT
V _{IK}		I _I = -18 mA	2.7 V			-1.2	V
V _{OH}		I _{OH} = -100 µA	MIN to MAX	V _{CC} - 0.2			V
		I _{OH} = -12 mA	2.7 V	2.2			
			3 V	2.4			
		I _{OH} = -24 mA	3 V	2			
V _{OL}		I _{OL} = 100 µA	MIN to MAX			0.2	V
		I _{OL} = 12 mA	2.7 V			0.4	
		I _{OL} = 24 mA	3 V			0.55	
I _I	Control pins	V _I = V _{CC} or GND	3.6 V			±5	µA
I _I (hold)	Data I/Os	V _I = 0.8 V	3 V	75			µA
		V _I = 2 V		-75			
I _{OZ} ‡		V _O = V _{CC} or GND	3.6 V			±10	µA
I _{CC}		V _I = V _{CC} or GND, I _O = 0	3.6 V			40	µA
ΔI _{CC}		V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND				500	µA
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V		3.5		pF
C _{io}	A or B ports	V _O = V _{CC} or GND	3.3 V		5		pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

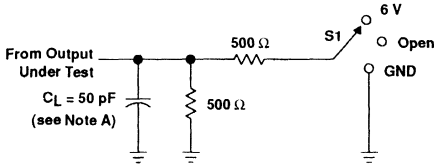
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V	UNIT
			MIN	TYP†	MAX	MAX	
t _{PLH}	A or B	B or A	1	1.8	3.5	3.8	ns
t _{PHL}			1	2.2	3.5	3.8	
t _{PZH}	OE	B or A	1	2.6	5	6	ns
t _{PZL}			1	2.7	4.6	5.2	
t _{PHZ}	OE	B or A	1	2.8	4.5	4.8	ns
t _{PLZ}			1	2.9	4.5	4.7	

operating characteristics, V_{CC} = 3.3 V, T_A = 25° C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance per bit	Outputs enabled	28	pF
		Outputs disabled	4	

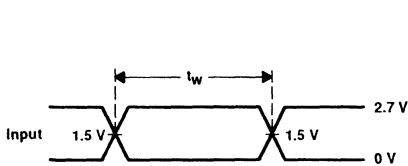


PARAMETER MEASUREMENT INFORMATION

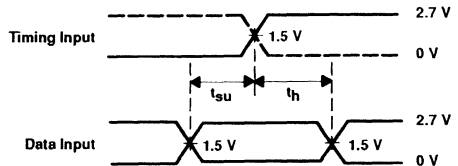


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

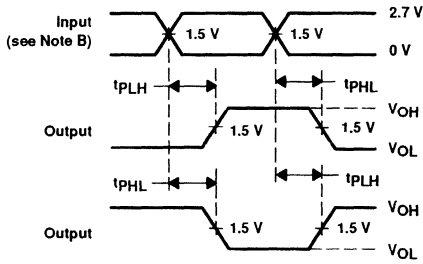
LOAD CIRCUIT FOR OUTPUTS



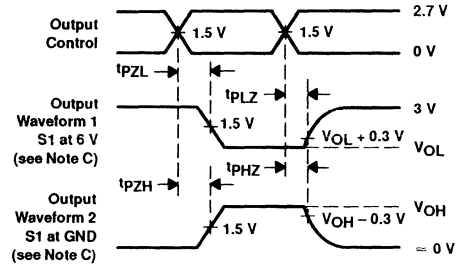
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

SN74LVC16373

16-BIT TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

NOVEMBER 1993

- Member of the Texas Instruments *Widebus™* Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Designed to Facilitate Incident Wave Switching for Line Impedances of 50 Ω or Greater
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages

description

This 16-bit transparent D-type latch is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC16373 is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. It can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

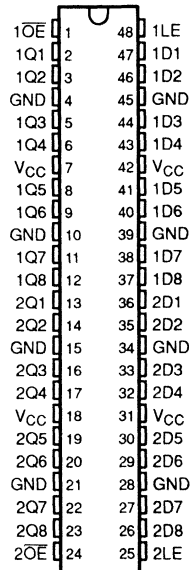
A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (\overline{OE}) input does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74LVC16373 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74LVC16373 is characterized for operation from -40°C to 85°C .

DGG OR DL PACKAGE
(TOP VIEW)



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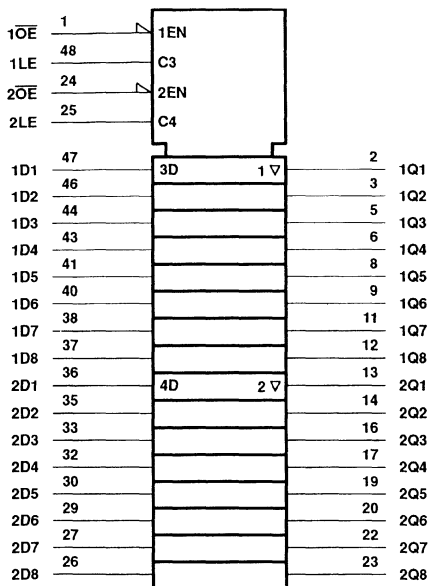
SN74LVC16373
16-BIT TRANSPARENT D-TYPE LATCH
WITH 3-STATE OUTPUTS

NOVEMBER 1993

FUNCTION TABLE
 (each 8-bit section)

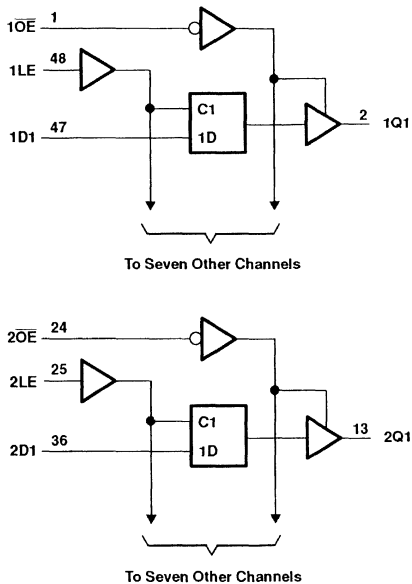
INPUTS			OUTPUT
OE	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q ₀
H	X	X	Z

logic symbol†



PRODUCT PREVIEW

logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN74LVC16373
16-BIT TRANSPARENT D-TYPE LATCH
WITH 3-STATE OUTPUTS
 NOVEMBER 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DGG package	0.8 W
..... DL package	0.85 W
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7$ V	-12	mA
		$V_{CC} = 3$ V	-24‡	
I_{OL}	Low-level output current	$V_{CC} = 2.7$ V	12	mA
		$V_{CC} = 3$ V	24‡	
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	-40	85	°C

NOTE 3: Unused or floating inputs must be held high or low.

‡ Current duty cycle ≤ 50%, $f \geq 1$ kHz

PRODUCT PREVIEW

SN74LVC16373
16-BIT TRANSPARENT D-TYPE LATCH
WITH 3-STATE OUTPUTS
 NOVEMBER 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} [†]	MIN	TYP	MAX	UNIT
V _{IK}	I _I = -18 mA	2.7 V			-1.2	V
V _{OH}	I _{OH} = -100 μA	MIN to MAX	V _{CC} - 0.2			V
	I _{OH} = -12 mA	2.7 V	2.2			
		3 V	2.4			
	I _{OH} = -24 mA	3 V	2			
V _{OL}	I _{OL} = 100 μA	MIN to MAX			0.2	V
	I _{OL} = 12 mA	2.7 V			0.4	
	I _{OL} = 24 mA	3 V			0.55	
I _I	V _I = V _{CC} or GND	3.6 V			±5	μA
I _{OZ}	V _O = V _{CC} or GND	3.6 V			±10	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V			20	μA
ΔI _{CC}	V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND				500	μA
C _i	V _I = V _{CC} or GND	3.3 V			TBD	pF
C _o	V _O = V _{CC} or GND	3.3 V			TBD	pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

SN74LVC16374
16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP
WITH 3-STATE OUTPUTS

NOVEMBER 1993

- Member of the Texas Instruments *Widebus™* Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Designed to Facilitate Incident Wave Switching for Line Impedances of 50 Ω or Greater
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages

description

This 16-bit edge-triggered D-type flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC16374 is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. It can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK) input, the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs.

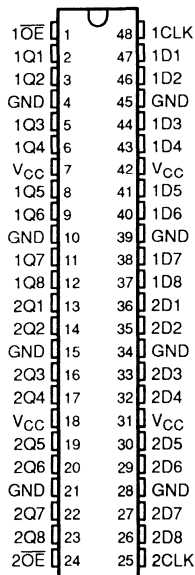
A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (\overline{OE}) input does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74LVC16374 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74LVC16374 is characterized for operation from -40°C to 85°C .

DGG OR DL PACKAGE
(TOP VIEW)



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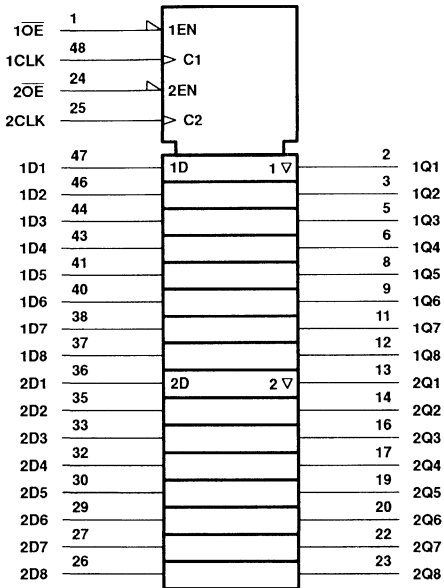
SN74LVC16374
16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP
WITH 3-STATE OUTPUTS

NOVEMBER 1993

FUNCTION TABLE
 (each flip-flop)

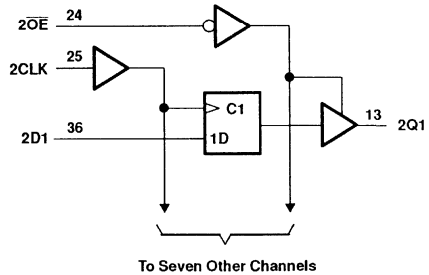
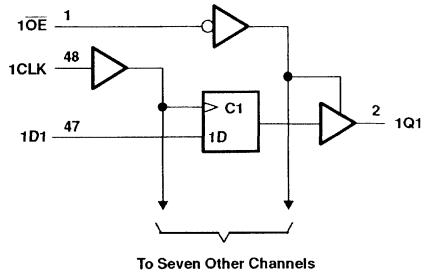
INPUTS			OUTPUT
\overline{OE}	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



PRODUCT PREVIEW

logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN74LVC16374
16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP
WITH 3-STATE OUTPUTS
 NOVEMBER 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DGG package	0.8 W
DL package	0.85 W
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7$ V		-12
		$V_{CC} = 3$ V		-24‡
I_{OL}	Low-level output current	$V_{CC} = 2.7$ V		12
		$V_{CC} = 3$ V		24‡
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	-40	85	°C

NOTE 3: Unused or floating inputs must be held high or low.

‡ Current duty cycle ≤ 50%, $f \geq 1$ kHz

PRODUCT PREVIEW

SN74LVC16374
16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP
WITH 3-STATE OUTPUTS

NOVEMBER 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} †	MIN	TYP	MAX	UNIT
V _{IK}	I _I = -18 mA	2.7 V			-1.2	V
V _{OH}	I _{OH} = -100 μA	MIN to MAX	V _{CC} - 0.2			V
	I _{OH} = -12 mA	2.7 V	2.2			
		3 V	2.4			
	I _{OH} = -24 mA	3 V	2			
V _{OL}	I _{OL} = 100 μA	MIN to MAX			0.2	V
	I _{OL} = 12 mA		2.7 V		0.4	
	I _{OL} = 24 mA		3 V		0.55	
I _I	V _I = V _{CC} or GND	3.6 V			±5	μA
I _{OZ}	V _O = V _{CC} or GND	3.6 V			±10	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V			20	μA
ΔI _{CC}	V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND				500	μA
C _I	V _I = V _{CC} or GND	3.3 V	TBD			pF
C _o	V _O = V _{CC} or GND	3.3 V	TBD			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW



SN74LVC16543
16-BIT REGISTERED TRANSCEIVER
WITH 3-STATE OUTPUTS

NOVEMBER 1993

- Member of the Texas Instruments *Widebus™* Family
- *EPIC™* (Enhanced-Performance Implanted CMOS) Submicron Process
- Designed to Facilitate Incident Wave Switching for Line Impedances of 50 Ω or Greater
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages

description

This 16-bit registered transceiver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC16543 can be used as two 8-bit transceivers or one 16-bit transceiver. Separate latch-enable (\overline{LEAB} or $LEBA$) and output-enable (\overline{OEAB} or $OEBA$) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable (\overline{CEAB}) input must be low in order to enter data from A or to output data from B. If \overline{CEAB} is low and \overline{LEAB} is low, the A-to-B latches are transparent; a subsequent low-to-high transition of \overline{LEAB} puts the A latches in the storage mode. With \overline{CEAB} and \overline{OEAB} both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the \overline{CEBA} , \overline{LEBA} , and \overline{OEBA} inputs.

The SN74LVC16543 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74LVC16543 is characterized for operation from -40°C to 85°C .

DGG OR DL PACKAGE
(TOP VIEW)

$\overline{1OEAB}$	1	56	$\overline{1OEBA}$
$\overline{1LEAB}$	2	55	$\overline{1LEBA}$
$\overline{1CEAB}$	3	54	$\overline{1CEBA}$
GND	4	53	GND
1A1	5	52	1B1
1A2	6	51	1B2
V_{CC}	7	50	V_{CC}
1A3	8	49	1B3
1A4	9	48	1B4
1A5	10	47	1B5
GND	11	46	GND
1A6	12	45	1B6
1A7	13	44	1B7
1A8	14	43	1B8
2A1	15	42	2B1
2A2	16	41	2B2
2A3	17	40	2B3
GND	18	39	GND
2A4	19	38	2B4
2A5	20	37	2B5
2A6	21	36	2B6
V_{CC}	22	35	V_{CC}
2A7	23	34	2B7
2A8	24	33	2B8
GND	25	32	GND
$\overline{2CEAB}$	26	31	$\overline{2CEBA}$
$\overline{2LEAB}$	27	30	$\overline{2LEBA}$
$\overline{2OEAB}$	28	29	$\overline{2OEBA}$

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SN74LVC16543
16-BIT REGISTERED TRANSCEIVER
WITH 3-STATE OUTPUTS

NOVEMBER 1993

FUNCTION TABLE†
 (each 8-bit section)

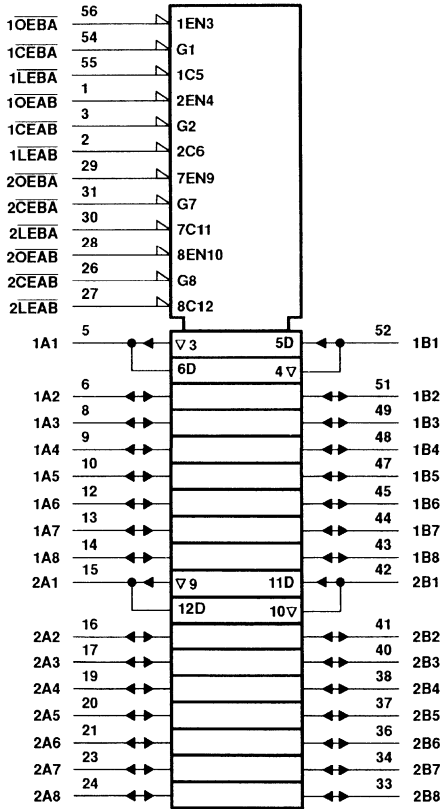
INPUTS				OUTPUT B
CEAB	LEAB	OEAB	A	
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B ₀ ‡
L	L	L	L	L
L	L	L	H	H

† A-to-B data flow is shown; B-to-A flow control is the same except that it uses CEBA, LEBA, and OEBA.

‡ Output level before the indicated steady-state input conditions were established.

logic symbols§

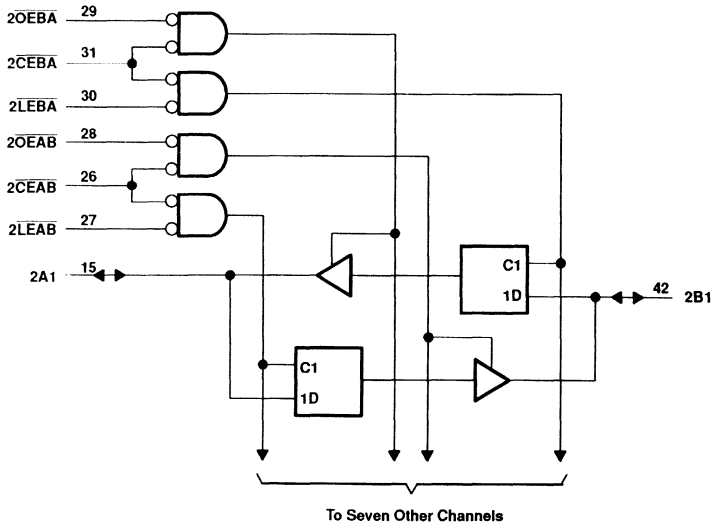
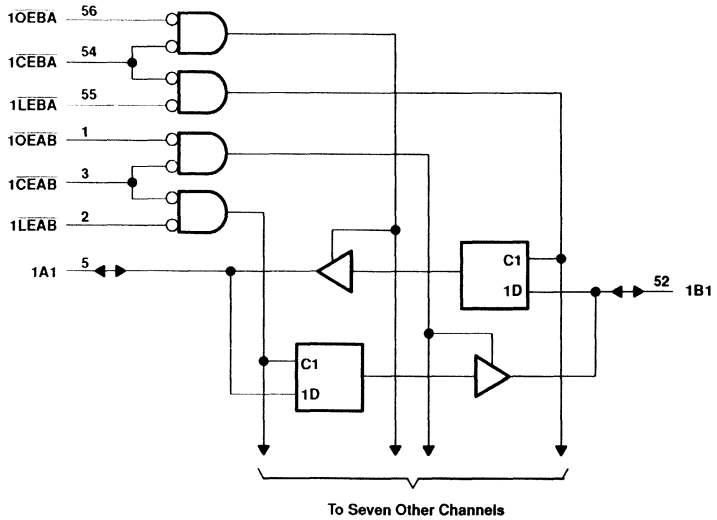
PRODUCT PREVIEW



§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



logic diagram (positive logic)



PRODUCT PREVIEW

SN74LVC16543
16-BIT REGISTERED TRANSCEIVER
WITH 3-STATE OUTPUTS
 NOVEMBER 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1)	-0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DGG package	1 W
..... DL package	1 W
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7$ V		-12
		$V_{CC} = 3$ V		-24‡
I_{OL}	Low-level output current	$V_{CC} = 2.7$ V		12
		$V_{CC} = 3$ V		24‡
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	-40	85	°C

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.

‡ Current duty cycle ≤ 50%, $f \geq 1$ kHz

PRODUCT PREVIEW



SN74LVC16543
16-BIT REGISTERED TRANSCEIVER
WITH 3-STATE OUTPUTS
 NOVEMBER 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC} †	MIN	TYP	MAX	UNIT
V _{IK}		I _I = -18 mA	2.7 V			-1.2	V
V _{OH}		I _{OH} = -100 µA	MIN to MAX	V _{CC} - 0.2			V
		I _{OH} = -12 mA	2.7 V	2.2			
		I _{OH} = -24 mA	3 V	2.4			
V _{OL}		I _{OL} = 100 µA	MIN to MAX			0.2	V
		I _{OL} = 12 mA	2.7 V			0.4	
		I _{OL} = 24 mA	3 V			0.55	
I _I		V _I = V _{CC} or GND	3.6 V			±5	µA
I _{OZ} ‡		V _O = V _{CC} or GND	3.6 V			±10	µA
I _{CC}		V _I = V _{CC} or GND, I _O = 0	3.6 V			20	µA
ΔI _{CC}		V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND				500	µA
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V				pF
C _{io}	A or B ports	V _O = V _{CC} or GND	3.3 V				pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

PRODUCT PREVIEW



SN74LVC16646

16-BIT BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

NOVEMBER 1993

- Member of the Texas Instruments *Widebus™* Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Designed to Facilitate Incident Wave Switching for Line Impedances of 50 Ω or Greater
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages

description

This 16-bit bus transceiver and register is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC16646 can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the SN74LVC16646.

Output-enable (\overline{OE}) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. The direction control (DIR) determines which bus receives data when \overline{OE} is low. In the isolation mode (\overline{OE} high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

The SN74LVC16646 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74LVC16646 is characterized for operation from -40°C to 85°C .

DGG OR DL PACKAGE
(TOP VIEW)

1DIR	1	56	$\overline{1OE}$
1CLKAB	2	55	1CLKBA
1SAB	3	54	1SBA
GND	4	53	GND
1A1	5	52	1B1
1A2	6	51	1B2
V_{CC}	7	50	V_{CC}
1A3	8	49	1B3
1A4	9	48	1B4
1A5	10	47	1B5
GND	11	46	GND
1A6	12	45	1B6
1A7	13	44	1B7
1A8	14	43	1B8
2A1	15	42	2B1
2A2	16	41	2B2
2A3	17	40	2B3
GND	18	39	GND
2A4	19	38	2B4
2A5	20	37	2B5
2A6	21	36	2B6
V_{CC}	22	35	V_{CC}
2A7	23	34	2B7
2A8	24	33	2B8
GND	25	32	GND
2SAB	26	31	2SBA
2CLKAB	27	30	2CLKBA
2DIR	28	29	$2\overline{OE}$

PRODUCT PREVIEW

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SN74LVC16646
16-BIT BUS TRANSCEIVER AND REGISTER
WITH 3-STATE OUTPUTS
 NOVEMBER 1993

PRODUCT PREVIEW

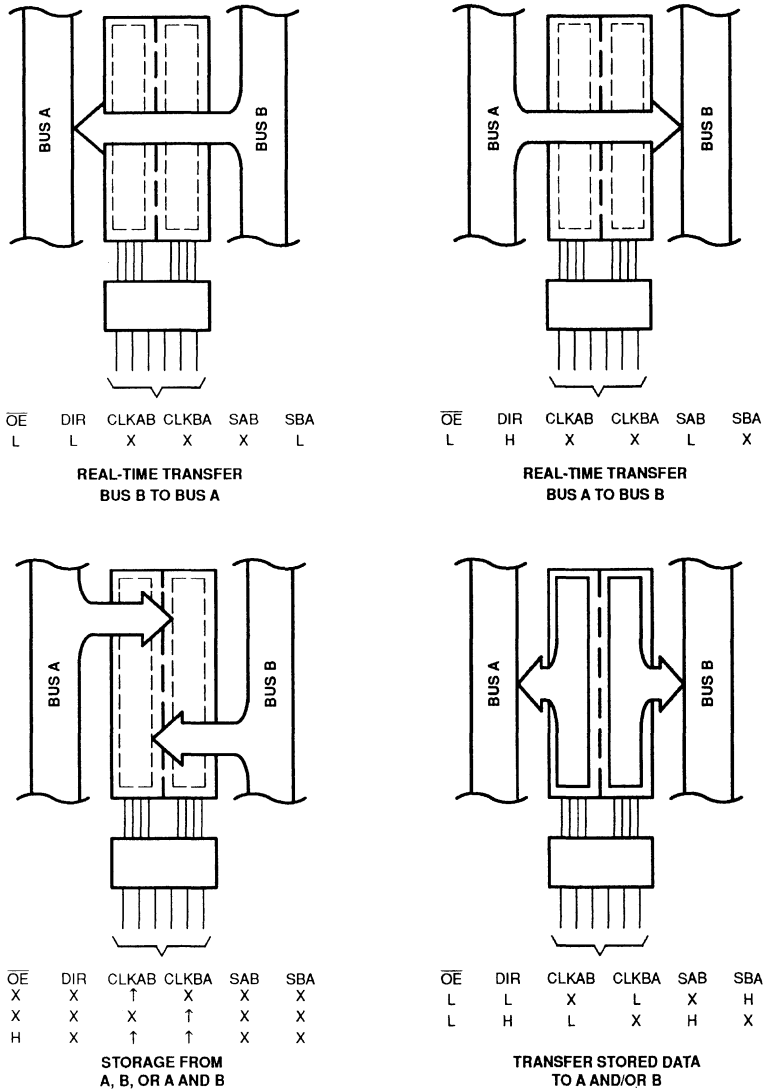
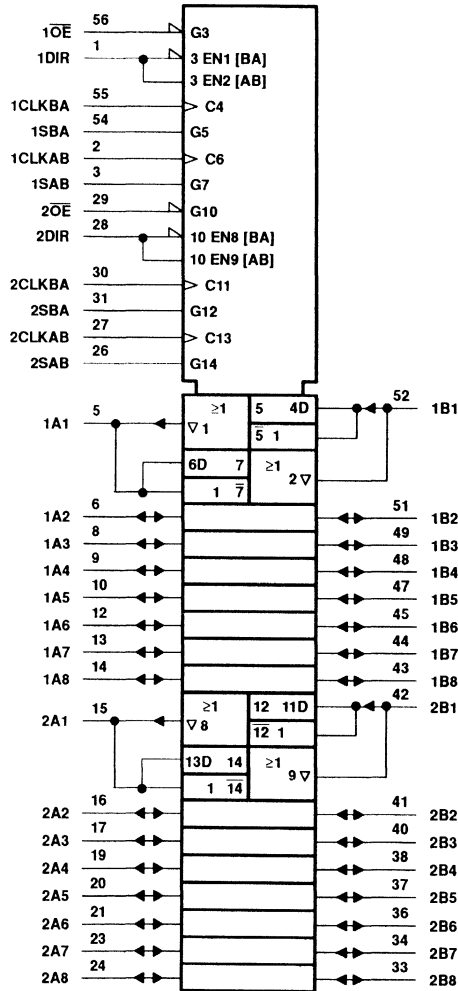


Figure 1. Bus-Management Functions

logic symbol†



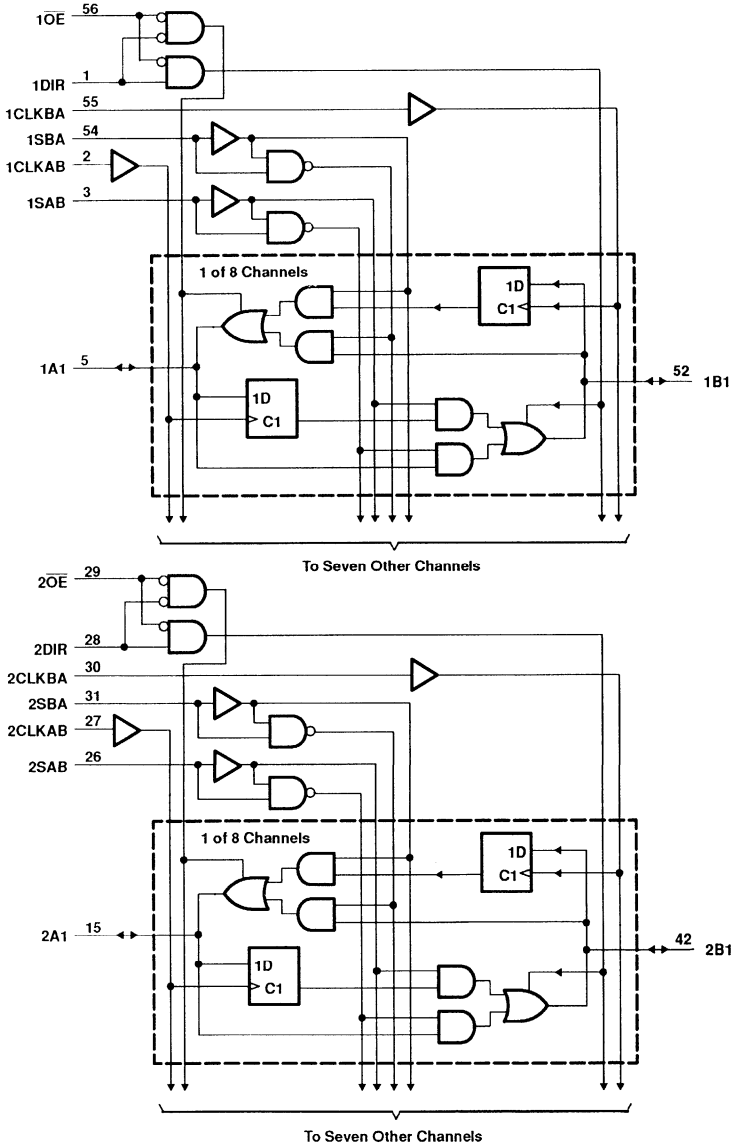
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

SN74LVC16646
16-BIT BUS TRANSCEIVER AND REGISTER
WITH 3-STATE OUTPUTS

NOVEMBER 1993

logic diagram (positive logic)



PRODUCT PREVIEW

SN74LVC16646
16-BIT BUS TRANSCEIVER AND REGISTER
WITH 3-STATE OUTPUTS
 NOVEMBER 1993

FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION
OE	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	L	L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	L	X	H	X	Input	Output	Stored A data to B bus

† The data output functions may be enabled or disabled by various signals at the OE and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1)	-0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DGG package	1 W
DL package	1 W
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.
 2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7$ V		-12
		$V_{CC} = 3$ V		-24§
I_{OL}	Low-level output current	$V_{CC} = 2.7$ V		12
		$V_{CC} = 3$ V		24§
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	-40	85	°C

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.

§ Current duty cycle ≤ 50%, $f \geq 1$ kHz

PRODUCT PREVIEW

SN74LVC16646
16-BIT BUS TRANSCEIVER AND REGISTER
WITH 3-STATE OUTPUTS

NOVEMBER 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} †	MIN	TYP	MAX	UNIT
V _{IK}	I _I = -18 mA	2.7 V			-1.2	V
V _{OH}	I _{OH} = -100 µA	MIN to MAX	V _{CC} -0.2			V
	I _{OH} = -12 mA	2.7 V	2.2			
		3 V	2.4			
	I _{OH} = -24 mA	3 V	2			
V _{OL}	I _{OL} = 100 µA	MIN to MAX			0.2	V
	I _{OL} = 12 mA	2.7 V			0.4	
	I _{OL} = 24 mA	3 V			0.55	
I _I	V _I = V _{CC} or GND	3.6 V			±5	µA
I _{OZ} ‡	V _O = V _{CC} or GND	3.6 V			±10	µA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V			20	µA
ΔI _{CC}	V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND				500	µA
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V			pF
C _{io}	A or B ports	V _O = V _{CC} or GND	3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

PRODUCT PREVIEW

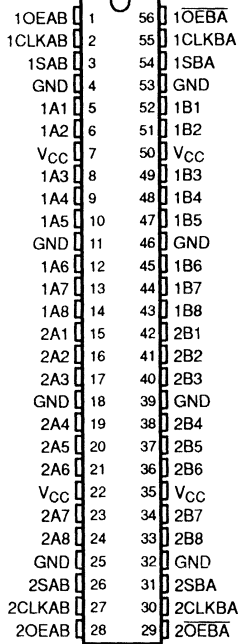
SN74LVC16652

16-BIT BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

NOVEMBER 1993

- Member of the Texas Instruments *Widebus™* Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Designed to Facilitate Incident Wave Switching for Line Impedances of 50 Ω or Greater
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages

DGG OR DL PACKAGE
(TOP VIEW)



description

This 16-bit bus transceiver and register is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC16652 consists of D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. The device can be used as two 8-bit transceivers or one 16-bit transceiver.

Complementary output-enable (OEAB and \overline{OEBA}) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high input level selects stored data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the SN74LVC16652.

Data on the A or B bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the levels on the select-control or output-enable inputs. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and \overline{OEBA} . In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus line are at high impedance, each set of bus lines remains at its last level configuration.

The SN74LVC16652 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74LVC16652 is characterized for operation from -40°C to 85°C .

PRODUCT PREVIEW

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SN74LVC16652
16-BIT BUS TRANSCEIVER AND REGISTER
WITH 3-STATE OUTPUTS
 NOVEMBER 1993

PRODUCT PREVIEW

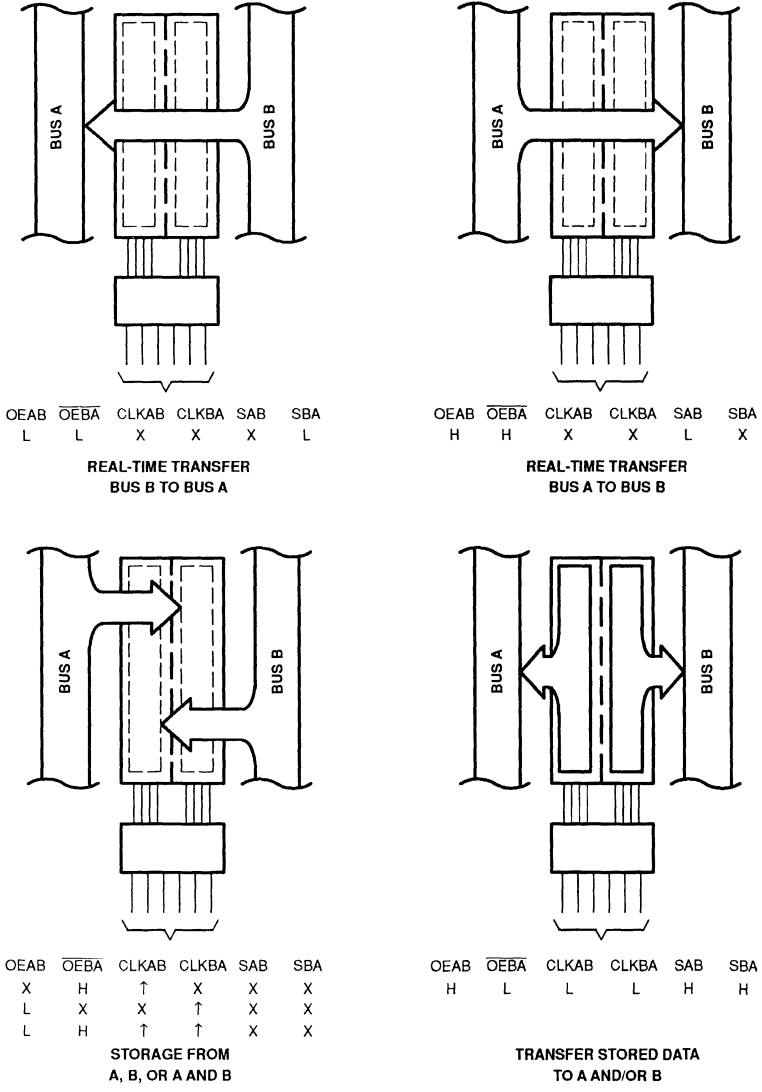
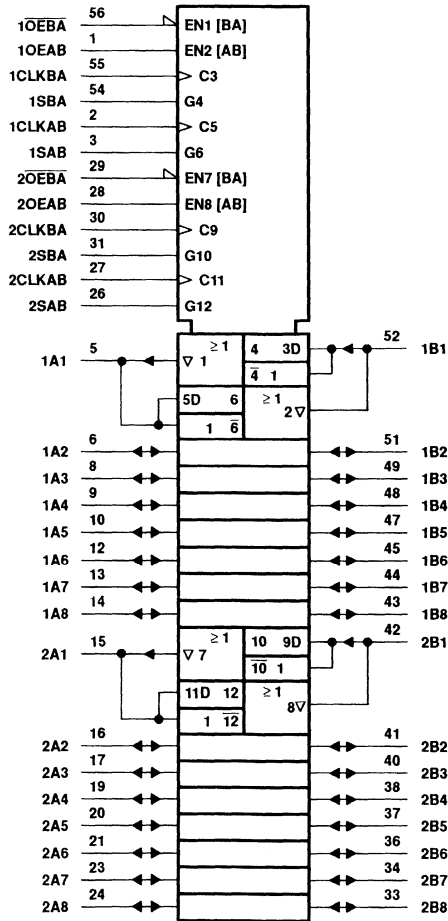


Figure 1. Bus-Management Functions

SN74LVC16652
16-BIT BUS TRANSCEIVER AND REGISTER
WITH 3-STATE OUTPUTS
NOVEMBER 1993

logic symbol†

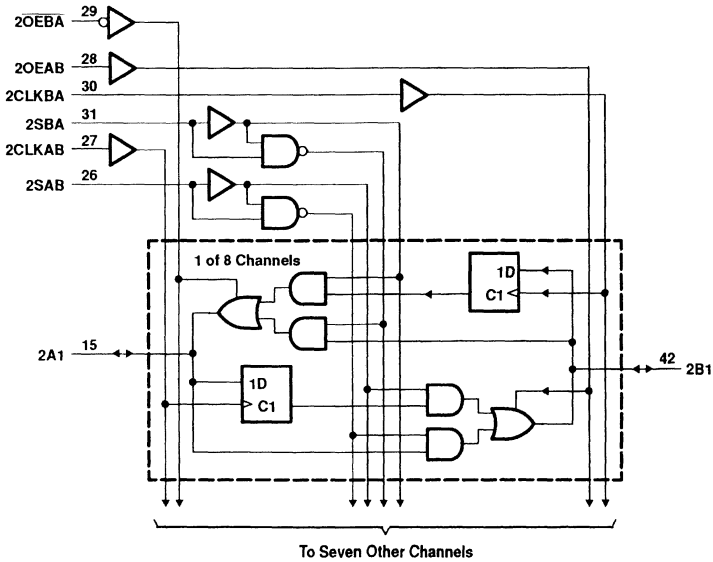
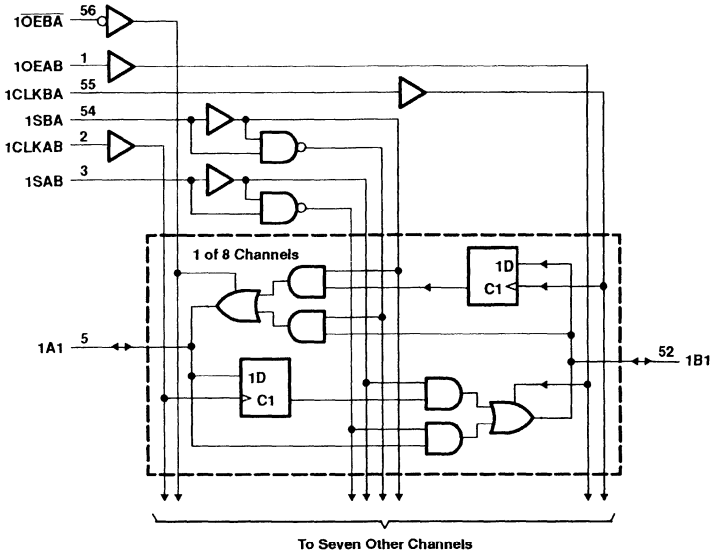


PRODUCT PREVIEW

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN74LVC16652
16-BIT BUS TRANSCEIVER AND REGISTER
WITH 3-STATE OUTPUTS
 NOVEMBER 1993

logic diagram (positive logic)



PRODUCT PREVIEW

SN74LVC16652

16-BIT BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

NOVEMBER 1993

FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
L	H	L	L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	L	X	X	Input	Unspecified‡	Store A, hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers
L	X	L	↑	X	X	Unspecified‡	Input	Hold A, store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	L	X	H	X	Input	Output	Stored A data to B bus
H	L	L	L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

† The data output functions may be enabled or disabled by a variety of level combinations at the OEAB or OEBA inputs. Data input functions are always enabled, i.e., data at the bus pins is stored on every low-to-high transition on the clock inputs.

‡ Select control = L; clocks can occur simultaneously.

§ Select control = H; clocks must be staggered in order to load both registers.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1)	-0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DGG package	1 W
DL package	1 W
Storage temperature range	-65°C to 150°C

§ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This value is limited to 4.6 V maximum.

PRODUCT PREVIEW

SN74LVC16652
16-BIT BUS TRANSCEIVER AND REGISTER
WITH 3-STATE OUTPUTS
 NOVEMBER 1993

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V _{CC}	Supply voltage	2.7	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V		V
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		V
V _I	Input voltage	0	V _{CC}	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2.7 V		-12
		V _{CC} = 3 V		-24†
I _{OL}	Low-level output current	V _{CC} = 2.7 V		12
		V _{CC} = 3 V		24†
Δt/Δv	Input transition rise or fall rate	0	10	ns/V
T _A	Operating free-air temperature	-40	85	°C

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.

† Current duty cycle ≤ 50%, f ≤ 1 kHz

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} ‡	MIN	TYP	MAX	UNIT
V _{IK}	I _I = -18 mA	2.7 V			-1.2	V
V _{OH}	I _{OH} = -100 μA	MIN to MAX	V _{CC} - 0.2			V
	I _{OH} = -12 mA	2.7 V	2.2			
	I _{OH} = -24 mA	3 V	2.4			
V _{OL}	I _{OL} = 100 μA	MIN to MAX			0.2	V
	I _{OL} = 12 mA	2.7 V			0.4	
	I _{OL} = 24 mA	3 V			0.55	
I _I	V _I = V _{CC} or GND	3.6 V			±5	μA
I _{OZ} §	V _O = V _{CC} or GND	3.6 V			±10	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V			20	μA
ΔI _{CC}	V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND				500	μA
C _I	Control inputs	V _I = V _{CC} or GND	3.3 V			pF
C _{IO}	A or B ports	V _O = V _{CC} or GND	3.3 V			pF

‡ For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

§ For I/O ports, the parameter I_{OZ} includes the input leakage current.

PRODUCT PREVIEW



SN74LVC16952 16-BIT REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

NOVEMBER 1993

- Member of the Texas Instruments *Widebus™* Family
- *EPIC™* (Enhanced-Performance Implanted CMOS) Submicron Process
- Designed to Facilitate Incident Wave Switching for Line Impedances of 50 Ω or Greater
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages

description

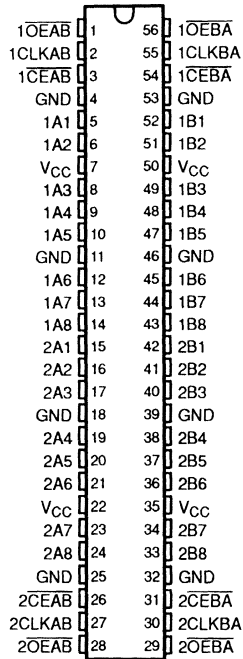
This 16-bit registered transceiver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC16952 contains two sets of D-type flip-flops for temporary storage of data flowing in either direction. It can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock (CLKAB or CLKBA) input provided that the clock-enable ($\overline{\text{CEAB}}$ or $\overline{\text{CEBA}}$) input is low. Taking the output-enable ($\overline{\text{OEAB}}$ or $\overline{\text{OEBA}}$) input low accesses the data on either port.

The SN74LVC16952 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74LVC16952 is characterized for operation from -40°C to 85°C .

DGG OR DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

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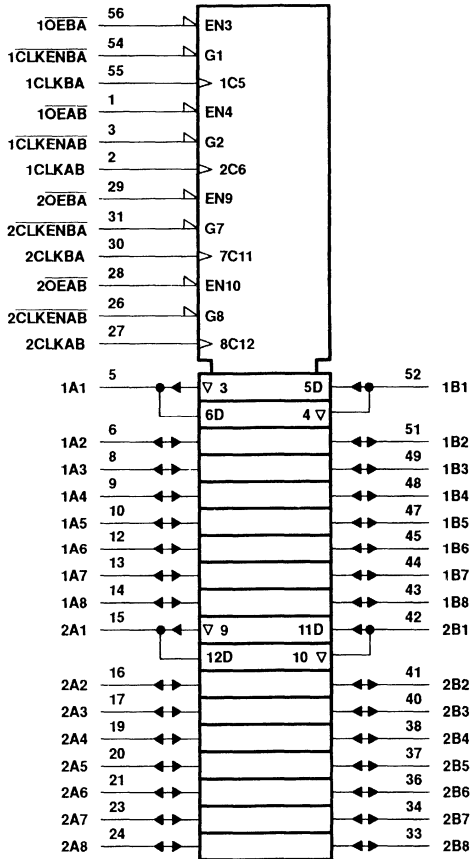
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SN74LVC16952
16-BIT REGISTERED TRANSCEIVER
WITH 3-STATE OUTPUTS
 NOVEMBER 1993

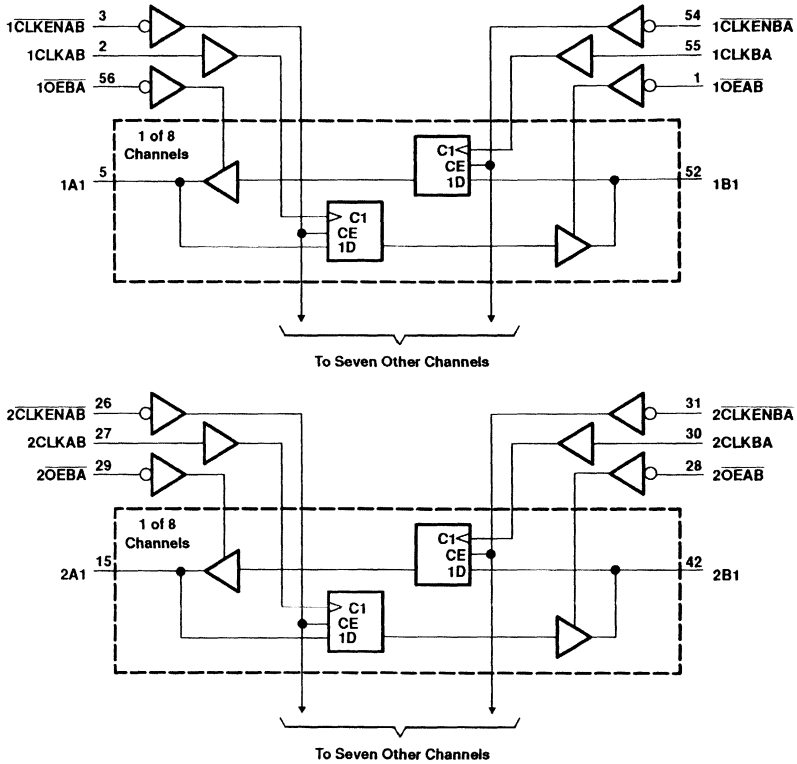
logic symbol†



PRODUCT PREVIEW

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



FUNCTION TABLE†

INPUTS				OUTPUT B
CLKENAB	CLKAB	OEAB	A	
H	X	L	X	B ₀ ‡
X	L	L	X	B ₀ ‡
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	Z

† A-to-B data flow is shown; B-to-A data flow is similar but uses CLKENBA, CLKBA, and OEBA.

‡ Level of B before the indicated steady-state input conditions were established.

PRODUCT PREVIEW

SN74LVC16952
16-BIT REGISTERED TRANSCEIVER
WITH 3-STATE OUTPUTS

NOVEMBER 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1)	-0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DGG package	1 W
DL package	1 W
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7$ V	-12	mA
		$V_{CC} = 3$ V	-24‡	
I_{OL}	Low-level output current	$V_{CC} = 2.7$ V	12	mA
		$V_{CC} = 3$ V	24‡	
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	-40	85	°C

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.

‡ Current duty cycle ≤ 50%, $f \geq 1$ kHz

PRODUCT PREVIEW



SN74LVC16952
16-BIT REGISTERED TRANSCEIVER
WITH 3-STATE OUTPUTS
NOVEMBER 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC} †	MIN	TYP	MAX	UNIT
V _{IK}		I _I = -18 mA	2.7 V			-1.2	V
V _{OH}		I _{OH} = -100 μA	MIN to MAX	V _{CC} - 0.2			V
		I _{OH} = -12 mA	2.7 V	2.2			
		I _{OH} = -24 mA	3 V	2.4			
V _{OL}		I _{OL} = 100 μA	MIN to MAX			0.2	V
		I _{OL} = 12 mA	2.7 V			0.4	
		I _{OL} = 24 mA	3 V			0.55	
I _I		V _I = V _{CC} or GND	3.6 V			±5	μA
I _{OZ} ‡		V _O = V _{CC} or GND	3.6 V			±10	μA
I _{CC}		V _I = V _{CC} or GND, I _O = 0	3.6 V			20	μA
ΔI _{CC}		V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND				500	μA
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V				pF
C _{io}	A or B ports	V _O = V _{CC} or GND	3.3 V				pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

PRODUCT PREVIEW



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SN74ALVC16240
16-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS

JANUARY 1993

- Member of the Texas Instruments *Widebus™* Family
- *EPIC™* (Enhanced-Performance Implanted CMOS) Submicron Process
- Designed to Facilitate Incident Wave Switching for Line Impedances of 50 Ω or Greater
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ$ C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ$ C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages

description

This 16-bit buffer/driver is designed for 2.7-V to 3.6-V V_{CC} operation.

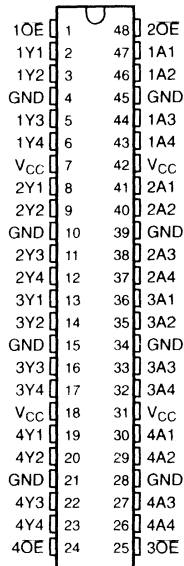
The SN74ALVC16240 is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. It provides inverting outputs and symmetrical OE (active-low output-enable) inputs.

The SN74ALVC16240 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16240 is characterized for operation from -40° C to 85° C.

DGG OR DL PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each 4-bit buffer)

INPUTS		OUTPUT
OE	A	Y
L	H	L
L	L	H
H	X	Z

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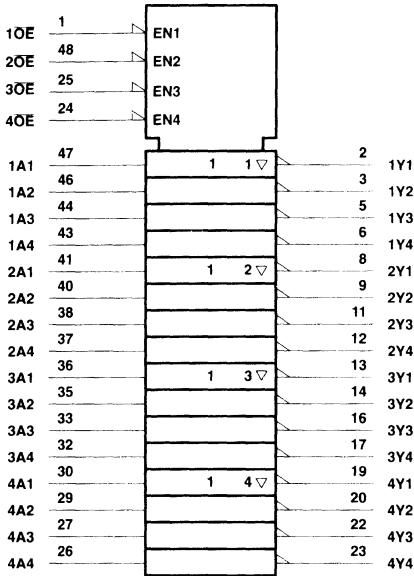


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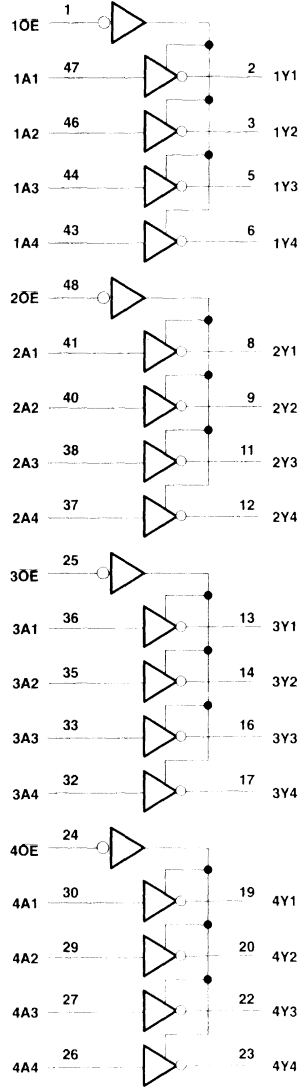
PRODUCT PREVIEW

SN74ALVC16240
16-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS
 JANUARY 1993

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DGG package	0.6 W
..... DL package	0.85 W
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT	
V_{CC}	Supply voltage	2.7	3.6	V	
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		2	V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		0.8	V
V_I	Input voltage	0	V_{CC}	V	
V_O	Output voltage	0	V_{CC}	V	
I_{OH}	High-level output current	$V_{CC} = 2.7$ V		-12	mA
		$V_{CC} = 3$ V		-24 [‡]	
I_{OL}	Low-level output current	$V_{CC} = 2.7$ V		12	mA
		$V_{CC} = 3$ V		24 [‡]	
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V	
T_A	Operating free-air temperature	-40	85	C	

NOTE 3. Unused or floating inputs must be held high or low.

[‡] Current duty cycle ≤ 50%, $f > 1$ kHz

PRODUCT PREVIEW

SN74ALVC16240
16-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS

JANUARY 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}^{\dagger}	MIN	TYP	MAX	UNIT
V_{IK}	$I_I = -18 \text{ mA}$	2.7 V			-1.2	V
V_{OH}	$I_{OH} = -100 \mu\text{A}$	MIN to MAX	$V_{CC} - 0.2$			V
	$I_{OH} = -12 \text{ mA}$	2.7 V	2.2			
		3 V	2.4			
V_{OL}	$I_{OH} = -24 \text{ mA}$	3 V	2			V
	$I_{OL} = 100 \mu\text{A}$	MIN to MAX	0.2			
	$I_{OL} = 12 \text{ mA}$	2.7 V	0.4			
	$I_{OL} = 24 \text{ mA}$	3 V	0.55			
I_I	$V_I = V_{CC}$ or GND	3.6 V			+5	μA
I_{OZ}	$V_O = V_{CC}$ or GND	3.6 V			+10	μA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			20	μA
ΔI_{CC}	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$, Other inputs at V_{CC} or GND	One input at $V_{CC} - 0.6 \text{ V}$,			500	μA
C_I	$V_I = V_{CC}$ or GND	3.3 V		TBD		pF
C_O	$V_O = V_{CC}$ or GND	3.3 V		TBD		pF

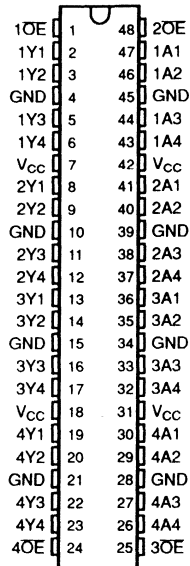
[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

SN74ALVC16244
16-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS
 SEPTEMBER 1993

- Member of the Texas Instruments *Widebus™* Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages

DGG OR DL PACKAGE
(TOP VIEW)



description

This 16-bit buffer/driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74ALVC16244 is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. It provides true outputs and symmetrical \overline{OE} (active-low output-enable) inputs.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVC16244 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16244 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each 4-bit buffer)

INPUTS		OUTPUT
\overline{OE}	A	Y
L	H	H
L	L	L
H	X	Z

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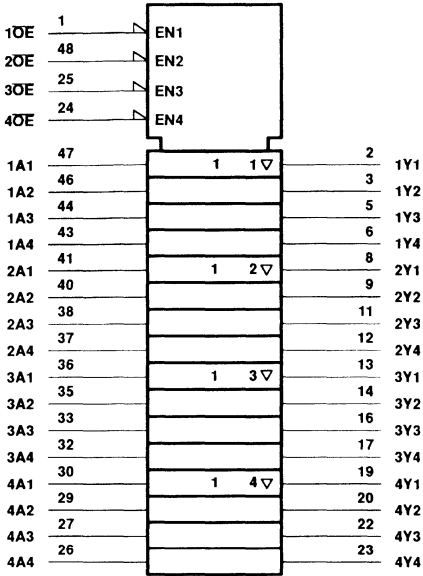


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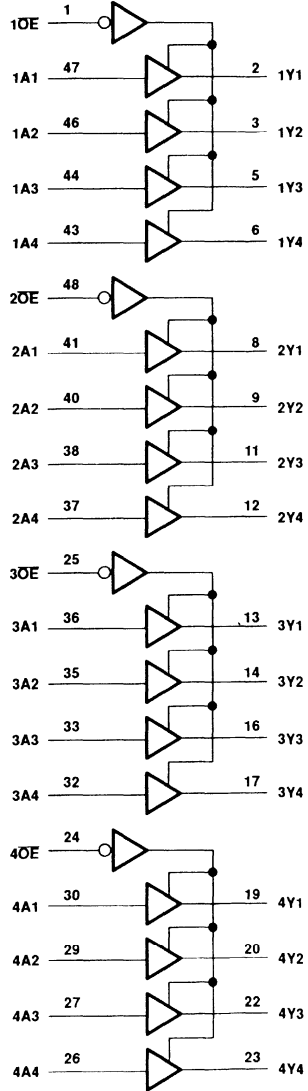
PRODUCT PREVIEW

SN74ALVC16244
16-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS
 SEPTEMBER 1993

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

SN74ALVC16244
16-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS
 SEPTEMBER 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 4.6 V
Output voltage range, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DGG package	0.8 W
DL package	0.85 W
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7$ V		-12
		$V_{CC} = 3$ V		-24
I_{OL}	Low-level output current	$V_{CC} = 2.7$ V		12
		$V_{CC} = 3$ V		24
$\Delta t/\Delta v$	input transition rise or fall rate	0	5	ns/V
T_A	Operating free-air temperature	-40	85	°C

NOTE 2: Unused or floating control pins must be held high or low.

PRODUCT PREVIEW

SN74ALVC16244
16-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS
 SEPTEMBER 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC} †	MIN	TYP	MAX	UNIT
V _{IK}		I _I = -18 mA	2.7 V			-1.2	V
V _{OH}		I _{OH} = -100 µA	MIN to MAX	V _{CC} - 0.2			V
		I _{OH} = -12 mA	2.7 V	2.2			
			3 V	2.4			
		I _{OH} = -24 mA	3 V	2			
V _{OL}		I _{OL} = 100 µA	MIN to MAX			0.2	V
		I _{OL} = 12 mA	2.7 V			0.4	
		I _{OL} = 24 mA	3 V			0.55	
I _I	Inputs	V _I = V _{CC} or GND	3.6 V			±5	µA
I _{hold}	Data pins	V _I = 0.8 V	3 V	75			µA
		V _I = 2 V		-75			
I _{OZ}		V _O = V _{CC} or GND	3.6 V			±10	µA
I _{CC}		V _I = V _{CC} or GND, I _O = 0	3.6 V			40	µA
ΔI _{CC}		V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND				500	µA
C _I		V _I = V _{CC} or GND	3.3 V		3.5		pF
C _O		V _O = V _{CC} or GND	3.3 V		3		pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

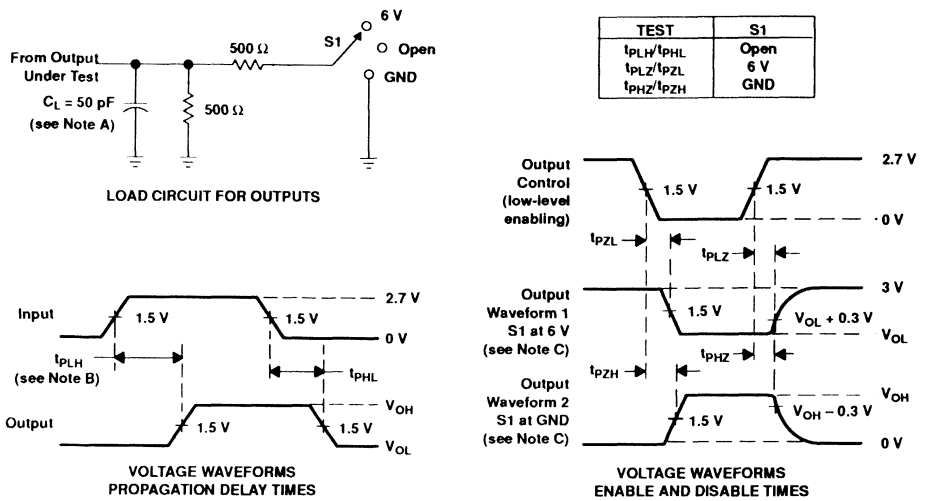
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V	UNIT
			MIN	TYP†	MAX	MAX	
t _{PLH}	A	Y	1	2	3.6	3.9	ns
t _{PHL}			1	2.1	3.6	3.9	
t _{PZH}	OE	Y	1	2.8	5	5.8	ns
t _{PZL}			1	2.8	5	5.8	
t _{PHZ}	OE	Y	1	3.2	4.9	5.4	ns
t _{PLZ}			1	3.2	4.9	5.4	

operating characteristics, V_{CC} = 3.3 V, T_A = 25° C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance per bit	Outputs enabled	16	pF
		Outputs disabled	5	pF

PRODUCT PREVIEW





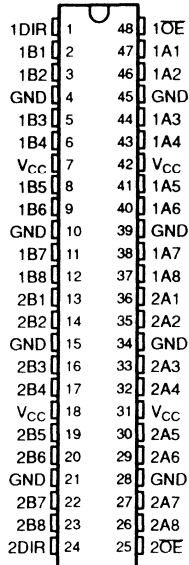
- NOTES
- A C_L includes probe and jig capacitance.
 - B All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_o = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 - C Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - D The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SN74ALVC16245
16-BIT BUS TRANSCEIVER
WITH 3-STATE OUTPUTS
 SEPTEMBER 1993

- Member of the Texas Instruments **Widebus™** Family
- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages

DGG OR DL PACKAGE
(TOP VIEW)



description

This 16-bit (dual-octal) noninverting bus transceiver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74ALVC16245 is designed for asynchronous communication between data buses. The control function implementation minimizes external timing requirements.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so that the buses are effectively isolated.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVC16245 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16245 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
\overline{OE}	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

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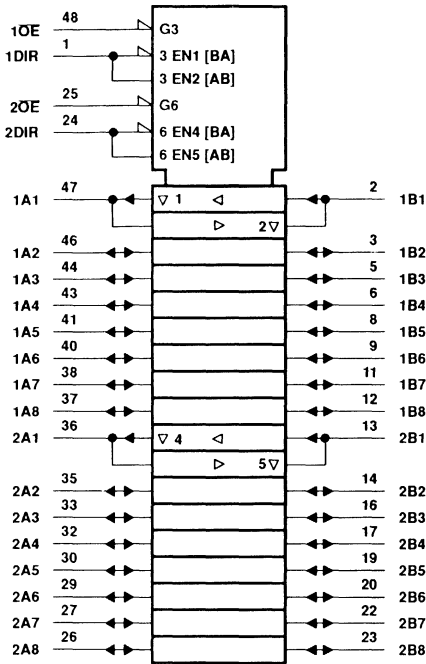


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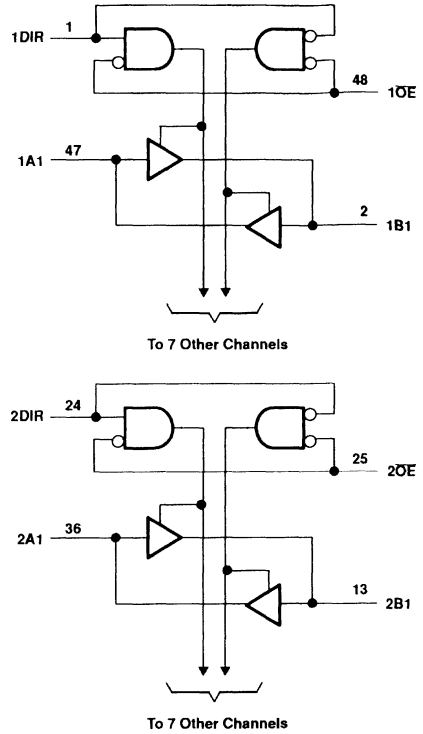
PRODUCT PREVIEW

SN74ALVC16245
16-BIT BUS TRANSCEIVER
WITH 3-STATE OUTPUTS
 SEPTEMBER 1993

logic symbol†



logic diagram (positive logic)



PRODUCT PREVIEW

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN74ALVC16245
16-BIT BUS TRANSCEIVER
WITH 3-STATE OUTPUTS
 SEPTEMBER 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1)	-0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DGG package	0.8 W
DL package	0.85 W
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

1. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7$ V	-12	mA
		$V_{CC} = 3$ V	-24	
I_{OL}	Low-level output current	$V_{CC} = 2.7$ V	12	mA
		$V_{CC} = 3$ V	24	
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_A	Operating free-air temperature	-40	85	°C

NOTE 2: Unused or floating control pins must be held high or low.

PRODUCT PREVIEW

SN74ALVC16245
16-BIT BUS TRANSCEIVER
WITH 3-STATE OUTPUTS
 SEPTEMBER 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}^{\dagger}	MIN	TYP	MAX	UNIT
V_{IK}		$I_I = -18 \text{ mA}$	2.7 V			-1.2	V
V_{OH}		$I_{OH} = -100 \mu\text{A}$	MIN to MAX	$V_{CC} - 0.2$			V
		$I_{OH} = -12 \text{ mA}$	2.7 V	2.2			
			3 V	2.4			
		$I_{OH} = -24 \text{ mA}$	3 V	2			
V_{OL}		$I_{OL} = 100 \mu\text{A}$	MIN to MAX			0.2	V
		$I_{OL} = 12 \text{ mA}$	2.7 V			0.4	
		$I_{OL} = 24 \text{ mA}$	3 V			0.55	
I_I	Control pins	$V_I = V_{CC}$ or GND	3.6 V			± 5	μA
I_{hold}	Data I/Os	$V_I = 0.8 \text{ V}$	3 V	75			μA
		$V_I = 2 \text{ V}$		-75			
I_{OZ}^{\ddagger}		$V_O = V_{CC}$ or GND	3.6 V			± 10	μA
I_{CC}		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			40	μA
ΔI_{CC}		$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$, Other inputs at V_{CC} or GND				500	μA
C_i	Control inputs	$V_I = V_{CC}$ or GND	3.3 V		3.5		pF
C_{io}	A or B ports	$V_O = V_{CC}$ or GND	3.3 V		5		pF

\dagger For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

\ddagger For I/O ports, the parameter I_{OZ} includes the input leakage current.

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$			$V_{CC} = 2.7 \text{ V}$	UNIT
			MIN	TYP \ddagger	MAX	MAX	
t_{PLH}	A or B	B or A	1	2	3.6	3.9	ns
t_{PHL}			1	2.1	3.6	3.9	
t_{PZH}	OE	B or A	1	2.8	5	5.8	ns
t_{PZL}			1	2.8	5	5.8	
t_{PHZ}	OE	B or A	1	3.2	4.9	5.4	ns
t_{PLZ}			1	3.2	4.9	5.4	

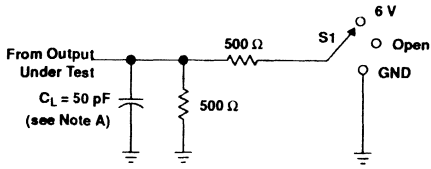
operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per bit	Outputs enabled	28	pF
		Outputs disabled	4	pF

PRODUCT PREVIEW

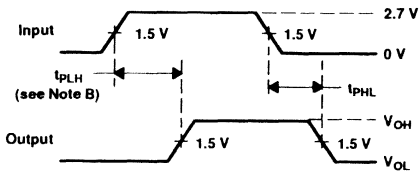


PARAMETER MEASUREMENT INFORMATION

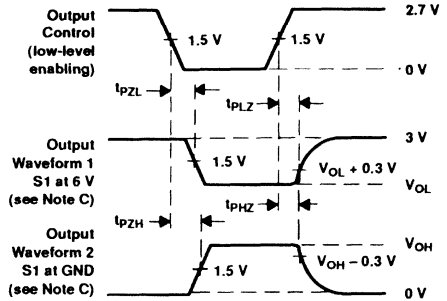


LOAD CIRCUIT FOR OUTPUTS

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
 PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
 ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

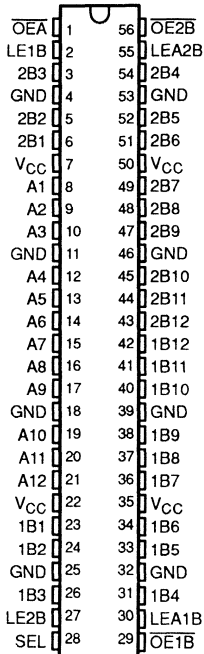
SN74ALVC16260

12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCHES WITH 3-STATE OUTPUTS

JUNE 1993

- **EPIC™ (Enhanced-Performance Implanted CMOS) Sub-Micron Process**
- **Member of the Texas Instruments Widebus™ Family**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3 V, T_A = 25^\circ C$**
- **Typical V_{OHV} (Output V_{CC} Overshoot) > 2 V at $V_{CC} = 3.3 V, T_A = 25^\circ C$**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Packaged in Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

SN74ALVC16260 . . . DGG or DL PACKAGE
(TOP VIEW)



description

The ALVC16260 is a 12-bit to 24-bit multiplexed D-type latch used in applications where two separate data paths must be multiplexed onto, or demultiplexed from, a single data path. Typical applications include multiplexing and/or demultiplexing of address and data information in microprocessor- or bus-interface applications. This device is also useful in memory-interleaving applications.

Three 12-bit I/O ports (A1–A12, 1B1–1B12, and 2B1–2B12) are available for address and/or data transfer. The output-enable ($\overline{OE1B}$, $\overline{OE2B}$, and \overline{OEA}) inputs control the bus transceiver functions. The $\overline{OE1B}$ and $\overline{OE2B}$ control signals also allow bank control in the A to B direction.

Address and/or data information can be stored using the internal storage latches. The latch-enable (LE1B, LE2B, LEA1B, and LEA2B) inputs are used to control data storage. When the latch-enable input is high, the latch is transparent. When the latch-enable input goes low, the data present at the inputs is latched and remains latched until the latch-enable input is returned high.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

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PRODUCT PREVIEW

SN74ALVC16260
12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCHES
WITH 3-STATE OUTPUTS

JUNE 1993

description (continued)

The SN74ALVC16260 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16260 is characterized for operation from -40°C to 85°C .

FUNCTION TABLES

B TO A ($\overline{\text{OE}}\text{B} = \text{H}$)

INPUTS						OUTPUT A
1B	2B	SEL	LE1B	LE2B	$\overline{\text{OE}}\text{A}$	
H	X	H	H	X	L	H
L	X	H	H	X	L	L
X	X	H	L	X	L	A ₀
X	H	L	X	H	L	H
X	L	L	X	H	L	L
X	X	L	X	L	L	A ₀
X	X	X	X	X	H	Z

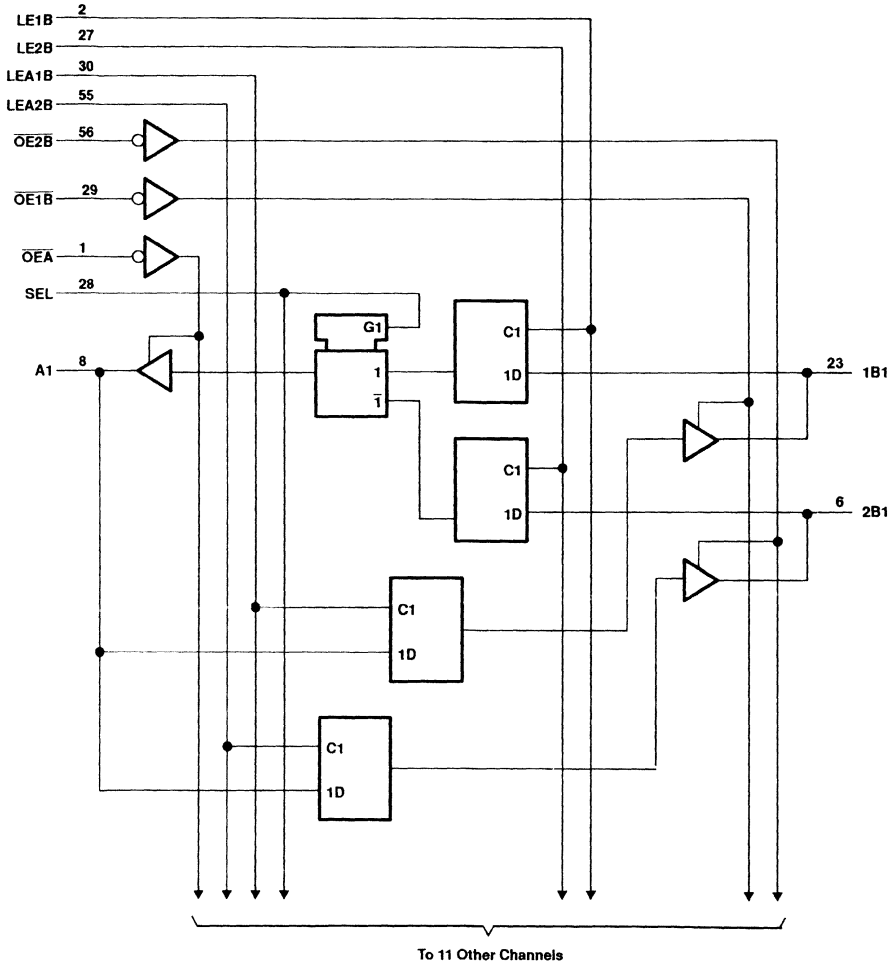
A TO B ($\overline{\text{OE}}\text{A} = \text{H}$)

INPUTS					OUTPUTS	
A	LEA1B	LEA2B	$\overline{\text{OE}}\text{1B}$	$\overline{\text{OE}}\text{2B}$	1B	2B
H	H	H	L	L	H	H
L	H	H	L	L	L	L
H	H	L	L	L	H	2B ₀
L	H	L	L	L	L	2B ₀
H	L	H	L	L	1B ₀	H
L	L	H	L	L	1B ₀	L
X	L	L	L	L	1B ₀	2B ₀
X	X	X	H	H	Z	Z
X	X	X	L	H	Active	Z
X	X	X	H	L	Z	Active
X	X	X	L	L	Active	Active

PRODUCT PREVIEW

SN74ALVC16260
12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCHES
WITH 3-STATE OUTPUTS
 JUNE 1993

logic diagram (positive logic)



PRODUCT PREVIEW

SN74ALVC16260

12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCHES WITH 3-STATE OUTPUTS

JUNE 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1)	-0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power package dissipation at $T_A = 55^\circ\text{C}$ (in still air):DGG	0.7W
..... DL	1W
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

NOTE 2: The input and output positive voltage ratings may be exceeded up to 4.6V if the input and output clamp-current ratings are observed.

recommended operating conditions(see Note 3)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2.7		3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		2	V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7$ V		-12	mA
		$V_{CC} = 3$ V		-24§	
I_{OL}	Low-level output current	$V_{CC} = 2.7$ V		12	mA
		$V_{CC} = 3$ V		24§	
$\Delta t/\Delta v$	Input transition rise or fall rate		Ø	10	ns/V
T_A	Operating free-air temperature	-40		85	°C

NOTE 3: Unused or floating control pins must be held high or low.

§ Current duty cycle ≤ 50%, $f \geq 1$ kHz

PRODUCT PREVIEW

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SN74ALVC16260

12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCHES WITH 3-STATE OUTPUTS

JUNE 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = -40 TO 85°C			UNIT
			MIN	TYP	MAX	
V _{OH}	I _{OH} = -100 μA	V _{CC} †	V _{CC} -0.2			V
	I _{OH} = -12 mA	2.7 V	2.2			
	I _{OH} = -12 mA	3 V	2.4			
	I _{OH} = -24 mA	3 V	2			
V _{OL}	I _{OL} = 100 μA	V _{CC} †	0.2			V
	I _{OL} = 12 mA	2.7 V	0.4			
	I _{OL} = 24 mA	3 V	0.55			
I _I	V _I = V _{CC} or GND	3.6 V	±5			μA
I _{hold}	V _I = 0.8 V	3.0 V	75			μA
	V _I = 2 V		-75			
I _{OZ}	V _O = V _{CC} or GND	3.6 V	±10			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V	20			μA
ΔI _{CC}	V _{CC} = 3 V to 3.6 V, one input at V _{CC} - 0.6 V, other inputs at V _{CC} or GND		500			μA
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V			pF
C _{ip}	A or B ports	V _O = V _{CC} or GND	3.3 V			pF

† V_{CC} = Min to Max

‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

PRODUCT PREVIEW

SN74ALVC16269

12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS

MARCH 1993

- EPIC™ (Enhanced-Performance Implanted CMOS) Sub-Micron Process

- Member of the Texas Instruments Widebus™ Family

- Supports Unregulated Battery Operation Down to 2.7 V

- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$

- Typical V_{OHV} (Output V_{CC} Overshoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$

- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)

- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17

- Packaged in Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

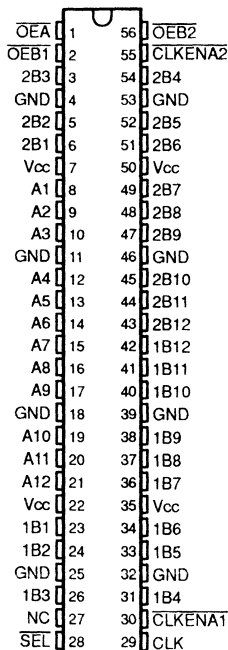
The 'ALVC16269 is a 12-bit to 24-bit registered bus exchanger, which is intended for applications where two separate ports must be multiplexed onto, or de-multiplexed from, a single port. It is particularly suitable as an interface between sync DRAMs and high speed microprocessors. The SN74ALVC16269 is designed specifically for low-voltage (3.3V) V_{CC} operation.

Data is stored in the internal B-port registers on the low-to-high transition of the CLK input, provided that the appropriate $\overline{\text{CLKEN}}_A$ inputs are low. Proper control of these inputs allows two sequential 12-bit words to be presented as a 24-bit word on the B-port. For data transfer in the B to A direction, a single storage register is provided. The $\overline{\text{SEL}}$ line selects 1B or 2B data for the A outputs. The register on the A output permits the fastest possible data transfer, thus extending the period that the data will be valid on the bus. The control pins are registered so that all transactions are synchronous with the clock. Data flow is controlled by the active-low output enables ($\overline{\text{OEA}}$, $\overline{\text{OEB1}}$, $\overline{\text{OEB2}}$).

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

The SN74ALVC16269 is characterized for operation from -40°C to 85°C .

SN74ALVC16269 . . . DGG or DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

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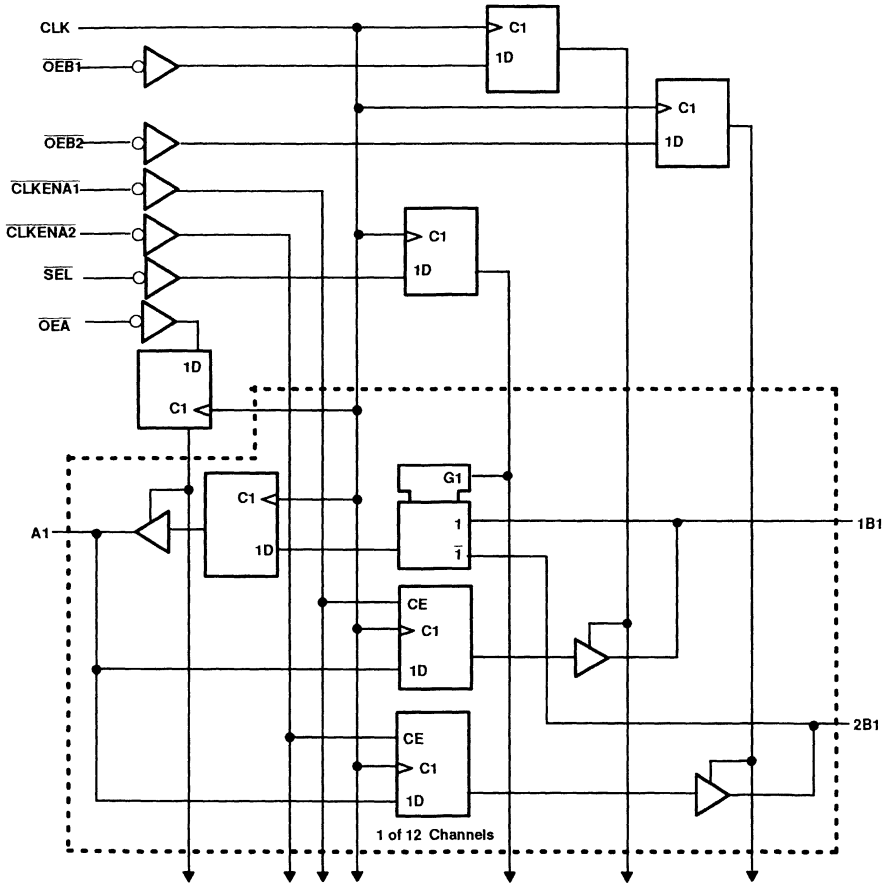
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SN74ALVC16269
12-BIT TO 24-BIT REGISTERED BUS EXCHANGER
WITH 3-STATE OUTPUTS

MARCH 1993

logic diagram (positive logic)

PRODUCT PREVIEW



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Function Tables

OUTPUT-ENABLE TABLE

INPUTS			OUTPUTS	
CLK	OEA	OEB	A	1B, 2B
↑	H	H	Z	Z
↑	H	L	Z	Active
↑	L	H	Active	Z
↑	L	L	Active	Active

A-TO-B STORAGE TABLE ($\overline{OEB} = L$)

INPUTS			OUTPUTS		
CLKENA1	CLKENA2	CLK	A	1B	2B
H	H	X	X	1B ₀ ‡	2B ₀ ‡
L	X	↑	L	L ¹	X
L	X	↑	H	H ¹	X
X	L	↑	L	X	L
X	L	↑	H	X	H

1 TWO CLK edges are needed to propagate data

B-TO-A STORAGE TABLE ($\overline{OEA} = L$)

INPUTS				OUTPUT
CLK	SEL	1B	2B	A
X	H	X	X	A ₀ ‡
X	L	X	X	A ₀ ‡
↑	H	L	X	L
↑	H	H	X	H
↑	L	X	L	L
↑	L	X	H	H

‡ Output level before the indicated steady-state input conditions were established

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power package dissipation at $T_A = 55^\circ\text{C}$ (in still air): DL	1W
..... DGG	0.7 W
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed

NOTE 2: The input and output positive voltage ratings may be exceeded up to 4.6V if the input and output clamp-current ratings are observed.

SN74ALVC16269
12-BIT TO 24-BIT REGISTERED BUS EXCHANGER
WITH 3-STATE OUTPUTS

MARCH 1993

recommended operating conditions(see Note 3)

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	2.7		3.6	V
V _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V		2	V
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	V
V _I	Input voltage	0		V _{CC}	V
V _O	Output voltage	0		V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2.7 V		-12	mA
		V _{CC} = 3 V		-24 [§]	
I _{OL}	Low-level output current	V _{CC} = 2.7 V		12	mA
		V _{CC} = 3 V		24 [§]	
Δt/Δv	Input transition rise or fall rate	6		10	ns/V
T _A	Operating free-air temperature	-40		85	°C

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.

§ Current duty cycle ≤ 50%, f ≥ 1 kHz

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = -40 TO 85°C			UNIT
			MIN	TYP	MAX	
V _{OH}	I _{OH} = -100 μA	V _{CC} [†]	V _{CC} - 0.2			V
	I _{OH} = -12 mA	2.7 V	2.2			
	I _{OH} = -12 mA	3 V	2.4			
	I _{OH} = -24 mA	3 V	2			
V _{OL}	I _{OL} = 100 μA	V _{CC} [†]	0.2			V
	I _{OL} = 12 mA	2.7 V	0.4			
	I _{OL} = 24 mA	3 V	0.55			
I _I	V _I = V _{CC} or GND	3.6 V	±5			μA
I _{OZ}	V _O = V _{CC} or GND	3.6 V	±10			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V	20			μA
ΔI _{CC}	V _{CC} = 3 V to 3.6 V, one input at V _{CC} - 0.6 V, other inputs at V _{CC} or GND		500			μA
C _I	Control inputs	V _I = V _{CC} or GND	3.3 V			pF
C _{I0}	A or B ports	V _O = V _{CC} or GND	3.3 V			pF

[†] V_{CC} = Min to Max

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

PRODUCT PREVIEW

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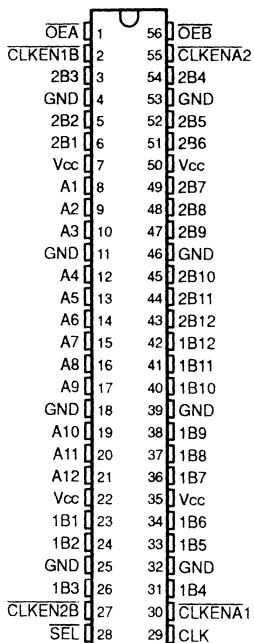


SN74ALVC16270 12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS

MARCH 1993

- **EPIC™** (Enhanced-Performance Implanted CMOS) Sub-Micron Process
- Member of the Texas Instruments **Widebus™** Family
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{CC} Overshoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Packaged in Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

SN74ALVC16270 . . . DGG or DL PACKAGE
(TOP VIEW)



description

The 'ALVC16270 is a 12-bit to 24-bit registered bus exchanger, which is intended for use in applications where data must be transferred from a narrow high speed bus to a wide lower frequency bus. It is designed specifically for low-voltage (3.3V) V_{CC} operation.

The device provides for synchronous data exchange between the two ports. Data is stored in the internal registers on the low-to-high transition of the CLK input, provided that the appropriate $\overline{\text{CLKEN}}$ inputs are low. The SEL line selects 1B or 2B data for the A outputs. For data transfer in the A to B direction, a two stage pipeline is provided in the A to 1B path, with a single storage register in the A to 2B path. Proper control of the $\overline{\text{CLKEN}}$ inputs allow two sequential 12-bit words to be presented synchronously as a 24-bit word on the B port. Data flow is controlled by the active-low output enables ($\overline{\text{OEA}}$, $\overline{\text{OEB}}$). These control pins are registered so that data flow changes are synchronous with the clock.

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

The SN74ALVC16270 is characterized for operation from -40°C to 85°C .

PRODUCT PREVIEW

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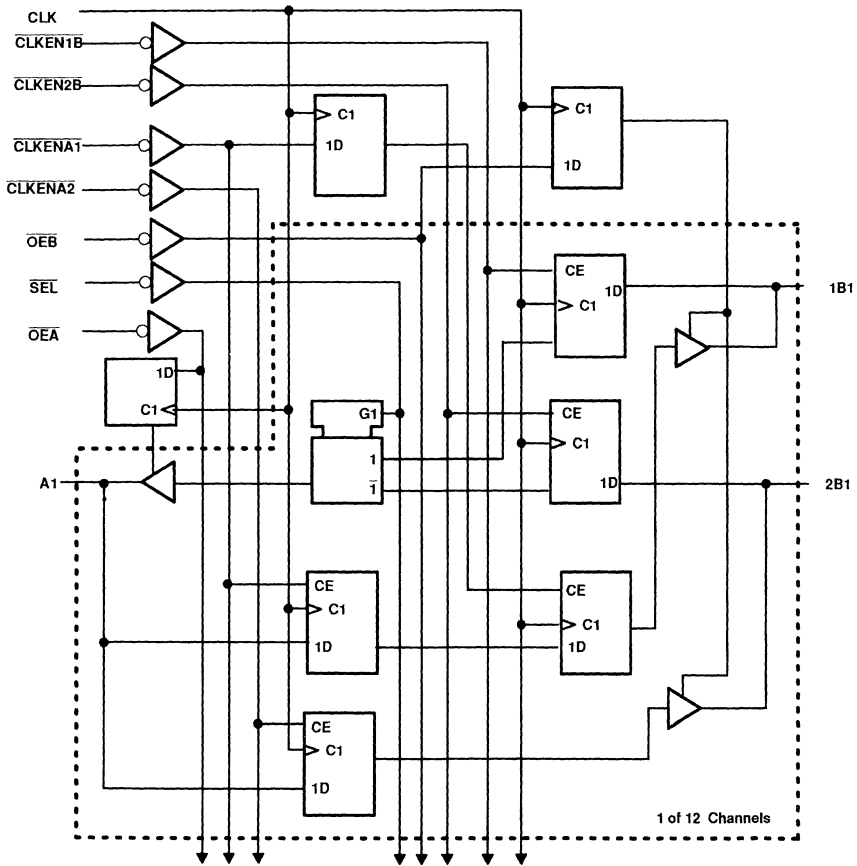


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SN74ALVC16270
12-BIT TO 24-BIT REGISTERED BUS EXCHANGER
WITH 3-STATE OUTPUTS
 MARCH 1993

logic diagram (positive logic)

PRODUCT PREVIEW



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SN74ALVC16270
12-BIT TO 24-BIT REGISTERED BUS EXCHANGER
WITH 3-STATE OUTPUTS
 MARCH 1993

Function Tables

OUTPUT-ENABLE TABLE

CLK	INPUTS		OUTPUTS	
	OEA	OEB	A	1B, 2B
↑	H	H	Z	Z
↑	H	L	Z	Active
↑	L	H	Active	Z
↑	L	L	Active	Active

A-TO-B STORAGE TABLE ($\overline{OEB} = L$)

INPUTS			OUTPUTS		
CLKENA1	CLKENA2	CLK	A	1B	2B
H	H	X	X	1B ₀ †	2B ₀ †
L	X	↑	L	L ¹	X
L	X	↑	H	H ¹	X
X	L	↑	L	X	L
X	L	↑	H	X	H

1 TWO CLK edges are needed to propagate data

B-TO-A STORAGE TABLE ($\overline{OEA} = L$)

INPUTS				OUTPUT		
CLKEN1B	CLKEN2B	CLK	SEL	1B	2B	A
H	X	X	H	X	X	A ₀ †
X	H	X	L	X	X	A ₀ †
L	X	↑	H	L	X	L
L	X	↑	H	H	X	H
X	L	↑	L	X	L	L
X	L	↑	L	X	H	H

† Output level before the indicated steady-state input conditions were established.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power package dissipation at $T_A = 55^\circ\text{C}$ (in still air): DL	1W
DGG	0.7 W
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

NOTE 2: The input and output positive voltage ratings may be exceeded up to 4.6V if the input and output clamp-current ratings are observed.

PRODUCT PREVIEW

SN74ALVC16270
12-BIT TO 24-BIT REGISTERED BUS EXCHANGER
WITH 3-STATE OUTPUTS

MARCH 1993

recommended operating conditions(see Note 3)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2.7		3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2			V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$			0.8	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7\text{ V}$			-12	mA
		$V_{CC} = 3\text{ V}$			-24§	
I_{OL}	Low-level output current	$V_{CC} = 2.7\text{ V}$			12	mA
		$V_{CC} = 3\text{ V}$			24§	
$\Delta t_{\Delta v}$	Input transition rise or fall rate		8		10	ns/V
T_A	Operating free-air temperature		-40		85	°C

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.

§ Current duty cycle $\leq 50\%$, $f \geq 1\text{ kHz}$

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = -40\text{ TO }85^\circ\text{C}$			UNIT	
			MIN	TYP	MAX		
V_{OH}	$I_{OH} = -100\ \mu\text{A}$	V_{CC}^\dagger	$V_{CC} - 0.2$			V	
	$I_{OH} = -12\ \text{mA}$	2.7 V	2.2				
	$I_{OH} = -12\ \text{mA}$	3 V	2.4				
	$I_{OH} = -24\ \text{mA}$	3 V	2				
V_{OL}	$I_{OL} = 100\ \mu\text{A}$	V_{CC}^\dagger	0.2			V	
	$I_{OL} = 12\ \text{mA}$	2.7 V	0.4				
	$I_{OL} = 24\ \text{mA}$	3 V	0.55				
I_I	$V_I = V_{CC}\text{ or GND}$	3.6 V	± 5			μA	
I_{OZ}	$V_O = V_{CC}\text{ or GND}$	3.6 V	± 10			μA	
I_{CC}	$V_I = V_{CC}\text{ or GND, } I_O = 0$	3.6 V	20			μA	
ΔI_{CC}	$V_{CC} = 3\text{ V to }3.6\text{ V, one input at } V_{CC} - 0.6\text{ V, other inputs at } V_{CC}\text{ or GND}$		500			μA	
C_I	Control inputs	$V_I = V_{CC}\text{ or GND}$	3.3 V				pF
C_{IO}	A or B ports	$V_O = V_{CC}\text{ or GND}$	3.3 V				pF

$^\dagger V_{CC} = \text{Min to Max}$

‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

PRODUCT PREVIEW

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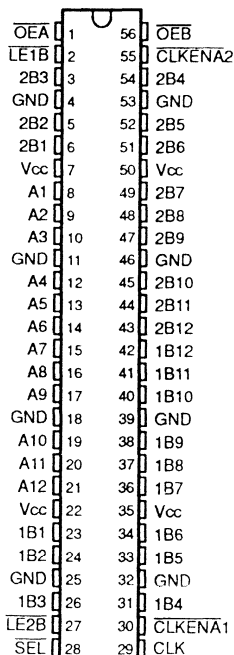


SN74ALVC16271 12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS

MARCH 1993

- EPIC™ (Enhanced-Performance Implanted CMOS) Sub-Micron Process
- Member of the Texas Instruments Widebus™ Family
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{CC} Overshoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Packaged in Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

SN74ALVC16271... DGG or DL PACKAGE
(TOP VIEW)



description

The 74ALVC16271 is a 12-bit to 24-bit registered bus exchanger, which can be used in applications where two separate data paths must be multiplexed onto, or demultiplexed from, a single data path. It is designed specifically for low-voltage (3.3-V) V_{CC} operation.

The part provides for synchronous data exchange between the two ports. Data is stored in the internal data registers on the low-to-high transition of the CLK input, provided that the $\overline{\text{CLKEN}}$ inputs are low. The $\overline{\text{SEL}}$ line selects 1B or 2B data for the A outputs. The data present on the A inputs is stored on every low-to-high transition of CLK provided $\overline{\text{LE}}$ is low. Data flow is controlled by the active-low output enables (OEA, OEB).

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

The SN74ALVC16271 is characterized for operation from -40°C to 85°C .

PRODUCT PREVIEW

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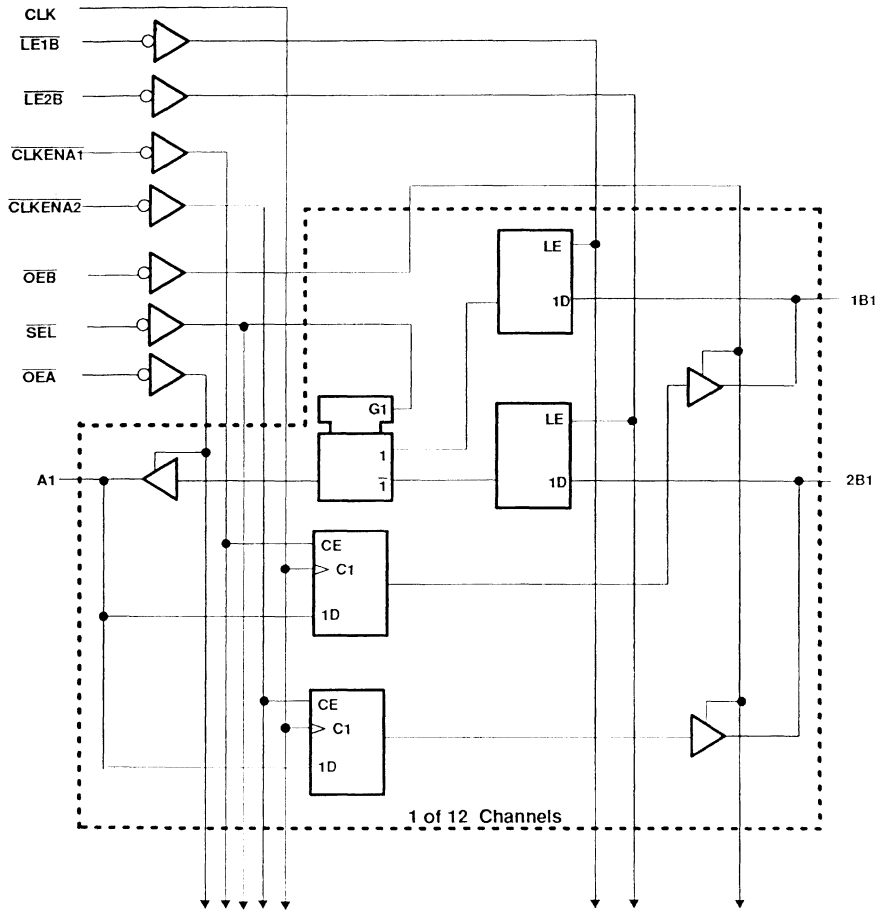
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SN74ALVC16271
12-BIT TO 24-BIT REGISTERED BUS EXCHANGER
WITH 3-STATE OUTPUTS
 MARCH 1993

logic diagram (positive logic)



PRODUCT PREVIEW

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SN74ALVC16271
12-BIT TO 24-BIT REGISTERED BUS EXCHANGER
WITH 3-STATE OUTPUTS

Function Tables

OUTPUT-ENABLE TABLE

CLK	INPUTS		OUTPUTS	
	OEA	OEB	A	1B, 2B
↑	H	H	Z	Z
↑	H	L	Z	Active
↑	L	H	Active	Z
↑	L	L	Active	Active

A-TO-B STORAGE TABLE ($\overline{OEB} = L$)

INPUTS			OUTPUTS	
CLKENA1	CLKENA2	CLK	A	1B 2B
H	H	X	X	1B0† 2B0†
L	X	↑	L	L1 X
L	X	↑	H	H1 X
X	L	↑	L	X L
X	L	↑	H	A0 H

1 TWO CLK edges are needed to propagate data

B-TO-A STORAGE TABLE ($\overline{OEA} = L$)

INPUTS				OUTPUT
LE	SEL	1B	2B	A
H	X	X	X	A0†
H	X	X	X	A0†
L	H	L	X	L
L	H	H	X	H
L	L	X	L	L
L	L	X	H	H

† Output level before the indicated steady-state input conditions were established.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V	
Input voltage range, V_I (except I/O ports) (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V	
Input voltage range, V_I (I/O ports) (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V	
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V	
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA	
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA	
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA	
Continuous current through V_{CC} or GND pins	±100 mA	
Maximum power package dissipation at $T_A = 55^\circ\text{C}$ (in still air): DL	1 W	
	DGG	0.7 W
Storage temperature range	-65°C to 150°C	

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

NOTE 1 The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

NOTE 2 The input and output positive voltage ratings may be exceeded up to 4.6 V if the input and output clamp current ratings are observed.

SN74ALVC16271
12-BIT TO 24-BIT REGISTERED BUS EXCHANGER
WITH 3-STATE OUTPUTS

MARCH 1993

recommended operating conditions(see Note 3)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2.7		3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2			V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$			0.8	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7\text{ V}$			-12	mA
		$V_{CC} = 3\text{ V}$			-24 [§]	
		$V_{CC} = 2.7\text{ V}$			12	
I_{OL}	Low-level output current	$V_{CC} = 2.7\text{ V}$			24 [§]	mA
		$V_{CC} = 3\text{ V}$				
$\Delta t_{\Delta V}$	Input transition rise or fall rate		0		10	ns/V
T_A	Operating free-air temperature		-40		85	°C

NOTE 3: Unused or floating pins (input or I/O) must be held high or low

§ Current duty cycle $\leq 50\%$, $f \geq 1\text{ kHz}$

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = -40\text{ TO }85^\circ\text{C}$			UNIT
			MIN	TYP	MAX	
V_{OH}	$I_{OH} = -100\ \mu\text{A}$	V_{CC}^\dagger	$V_{CC} - 0.2$			V
	$I_{OH} = -12\ \text{mA}$	2.7 V	2.2			
	$I_{OH} = -12\ \text{mA}$	3 V	2.4			
	$I_{OH} = -24\ \text{mA}$	3 V	2			
V_{OL}	$I_{OL} = 100\ \mu\text{A}$	V_{CC}^\dagger			0.2	V
	$I_{OL} = 12\ \text{mA}$	2.7 V			0.4	
	$I_{OL} = 24\ \text{mA}$	3 V			0.55	
I_I	$V_I = V_{CC}\text{ or GND}$	3.6 V			+5	μA
I_{OZ}	$V_O = V_{CC}\text{ or GND}$	3.6 V			+10	μA
I_{CC}	$V_I = V_{CC}\text{ or GND}, I_O = 0$	3.6 V			20	μA
ΔI_{CC}	$V_{CC} = 3\text{ V to }3.6\text{ V}$, one input at $V_{CC} - 0.6\text{ V}$, other inputs at $V_{CC}\text{ or GND}$				500	μA
C_i	Control inputs	$V_I = V_{CC}\text{ or GND}$	3.3 V			pF
C_{iO}	A or B ports	$V_O = V_{CC}\text{ or GND}$	3.3 V			pF

[†] $V_{CC} = \text{Min to Max}$

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current

PRODUCT PREVIEW

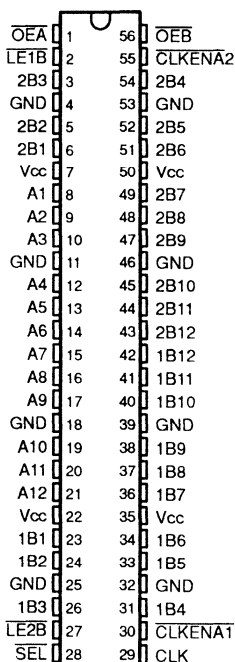
SN74ALVC16272

12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS

MARCH 1993

- EPIC™ (Enhanced-Performance Implanted CMOS) Sub-Micron Process
- Member of the Texas Instruments Widebus™ Family
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{CC} Overshoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Packaged in Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

SN74LVC16272 . . . DGG or DL PACKAGE
(TOP VIEW)



description

The LVC16272 is a 12-bit to 24-bit registered bus exchanger, which can be used in applications where two separate data paths must be multiplexed onto, or demultiplexed from, a single data path. It is designed specifically for low-voltage (3.3-V) Vcc operation.

The part provides for synchronous data exchange between the two ports. Data is stored in the internal data registers on the low-to-high transition of the CLK input, provided that the CLKEN inputs are low. The SEL line selects 1B or 2B data for the A outputs. The data present on the A1 input is stored on every low-to-high transition of CLK provided LEB is low. Data flow is controlled by the active-low output enables (OEA, OEB).

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

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The SN74LVC16272 is characterized for operation from -40°C to 85°C .

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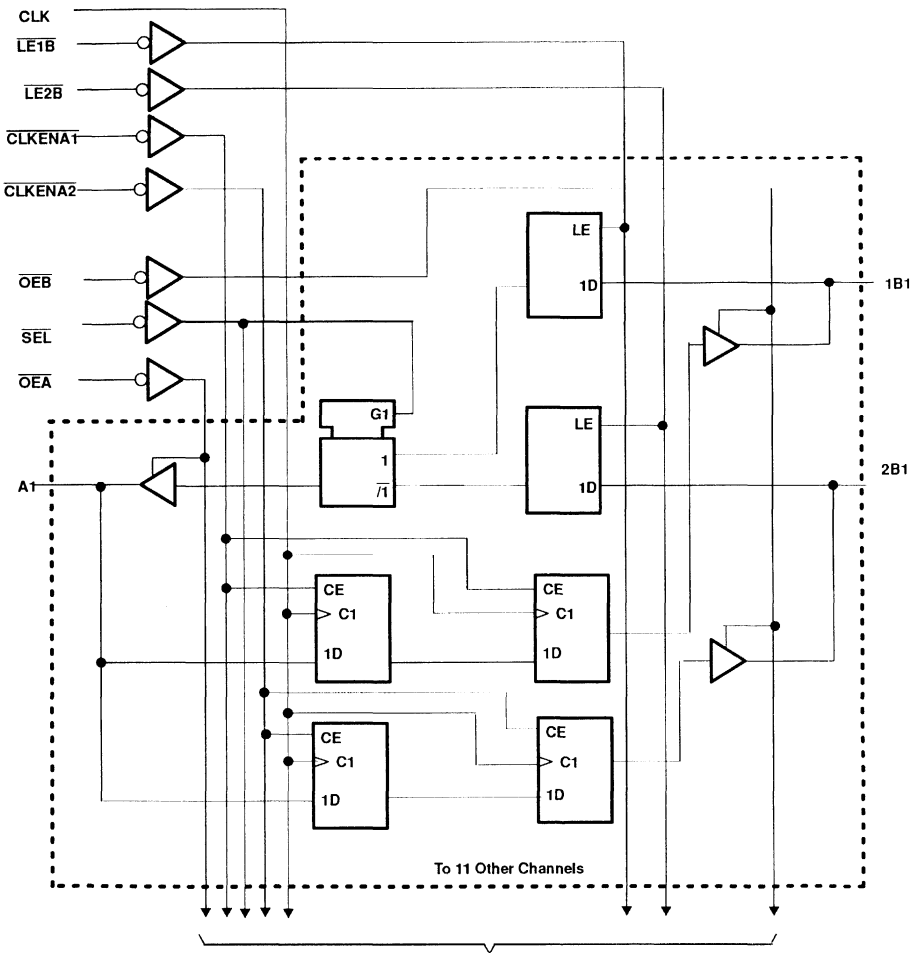


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PRODUCT PREVIEW

SN74ALVC16272
12-BIT TO 24-BIT REGISTERED BUS EXCHANGER
WITH 3-STATE OUTPUTS
 MARCH 1993

logic diagram (positive logic)



PRODUCT PREVIEW

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SN74ALVC16272

12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS

MARCH 1993

Function Tables

OUTPUT-ENABLE TABLE

INPUTS			OUTPUTS	
CLK	OEA	OEB	A	1B, 2B
↑	H	H	Z	Z
↑	H	L	Z	Active
↑	L	H	Active	Z
↑	L	L	Active	Active

A-TO-B STORAGE TABLE (OEB = L)

INPUTS			OUTPUTS	
CLKENA1	CLKENA2	CLK	A	1B 2B
H	H	X	X	1B ₀ † 2B ₀ †
L	X	↑	L	L ¹ X
L	X	↑	H	H ¹ X
X	L	↑	L	X L
X	L	↑	H	A ₀ H

B-TO-A STORAGE TABLE (OEA = L)

INPUTS				OUTPUT
LE	SEL	1B	2B	A
H	X	X	X	A ₀ †
H	X	X	X	A ₀ †
L	H	L	X	L
L	H	H	X	H
L	L	X	L	L
L	L	X	H	H

† Output level before the indicated steady-state input conditions were established.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power package dissipation at $T_A = 55^\circ\text{C}$ (in still air): DL	1W
..... DGG	0.7 W
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

NOTE 2: The input and output positive voltage ratings may be exceeded up to 4.6V if the input and output clamp-current ratings are observed.

SN74ALVC16272
12-BIT TO 24-BIT REGISTERED BUS EXCHANGER
WITH 3-STATE OUTPUTS

MARCH 1993

recommended operating conditions(see Note 3)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2.7		3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2			V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$			0.8	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7\text{ V}$			-12	mA
		$V_{CC} = 3\text{ V}$			-24§	
I_{OL}	Low-level output current	$V_{CC} = 2.7\text{ V}$			12	mA
		$V_{CC} = 3\text{ V}$			24§	
$\Delta t/\Delta v$	Input transition rise or fall rate		0.		10	ns/V
T_A	Operating free-air temperature		-40		85	°C

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.

§ Current duty cycle $\leq 50\%$, $f \geq 1\text{ kHz}$

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = -40\text{ TO }85^\circ\text{C}$			UNIT
			MIN	TYP	MAX	
V_{OH}	$I_{OH} = -100\ \mu\text{A}$	V_{CC}^\dagger	$V_{CC} - 0.2$			V
	$I_{OH} = -12\ \text{mA}$	2.7 V	2.2			
	$I_{OH} = -12\ \text{mA}$	3 V	2.4			
	$I_{OH} = -24\ \text{mA}$	3 V	2			
V_{OL}	$I_{OL} = 100\ \mu\text{A}$	V_{CC}^\dagger			0.2	V
	$I_{OL} = 12\ \text{mA}$	2.7 V			0.4	
	$I_{OL} = 24\ \text{mA}$	3 V			0.55	
I_I	$V_I = V_{CC}$ or GND	3.6 V			± 5	μA
I_{OZ}	$V_O = V_{CC}$ or GND	3.6 V			± 10	μA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			20	μA
ΔI_{CC}	$V_{CC} = 3\text{ V to }3.6\text{ V}$, one input at $V_{CC} - 0.6\text{ V}$, other inputs at V_{CC} or GND				500	μA
C_i	Control inputs	$V_I = V_{CC}$ or GND	3.3 V			pF
C_{iO}	A or B ports	$V_O = V_{CC}$ or GND	3.3 V			pF

¹ $V_{CC} = \text{Min to Max}$

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

PRODUCT PREVIEW

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SN74ALVC16373
16-BIT TRANSPARENT D-TYPE LATCH
WITH 3-STATE OUTPUTS

JANUARY 1993

- Member of the Texas Instruments *Widebus™* Family
- *EPIC™* (Enhanced-Performance Implanted CMOS) Submicron Process
- Designed to Facilitate Incident Wave Switching for Line Impedances of 50 Ω or Greater
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages

description

This 16-bit transparent D-type latch is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74ALVC16373 is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. It can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

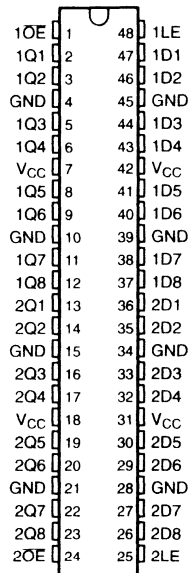
A buffered output-enable (OE) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (OE) input does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74ALVC16373 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16373 is characterized for operation from -40°C to 85°C .

DGG OR DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

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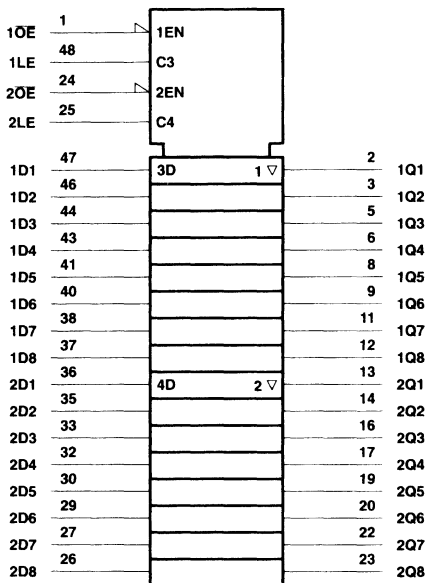
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SN74ALVC16373
16-BIT TRANSPARENT D-TYPE LATCH
WITH 3-STATE OUTPUTS
 JANUARY 1993

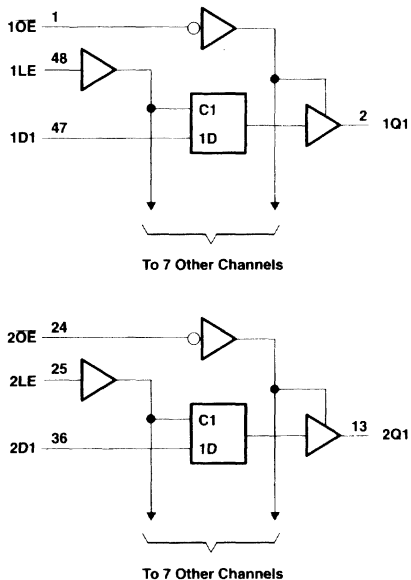
FUNCTION TABLE
 (each 8-bit section)

INPUTS			OUTPUT
OE	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q ₀
H	X	X	Z

logic symbol†



logic diagram (positive logic)



PRODUCT PREVIEW

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN74ALVC16373
16-BIT TRANSPARENT D-TYPE LATCH
WITH 3-STATE OUTPUTS
JANUARY 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DGG package	0.6 W
DL package	0.85 W
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7$ V	-12	mA
		$V_{CC} = 3$ V	-24†	
I_{OL}	Low-level output current	$V_{CC} = 2.7$ V	12	mA
		$V_{CC} = 3$ V	24†	
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	-40	85	°C

NOTE 3: Unused or floating inputs must be held high or low.
 † Current duty cycle < 50%, $f > 1$ kHz

PRODUCT PREVIEW

SN74ALVC16373
16-BIT TRANSPARENT D-TYPE LATCH
WITH 3-STATE OUTPUTS

JANUARY 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} [†]	MIN	TYP	MAX	UNIT
V _{IK}	I _I = -18 mA	2.7 V			-1.2	V
V _{OH}	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2			V
	I _{OH} = -12 mA	2.7 V	2.2			
		3 V	2.4			
	I _{OH} = -24 mA	3 V	2			
V _{OL}	I _{OL} = 100 μA	MIN to MAX			0.2	V
	I _{OL} = 12 mA	2.7 V			0.4	
	I _{OL} = 24 mA	3 V			0.55	
I _I	V _I = V _{CC} or GND	3.6 V			±5	μA
I _{OZ}	V _O = V _{CC} or GND	3.6 V			±10	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V			20	μA
ΔI _{CC}	V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC} or GND, One input at V _{CC} - 0.6 V.				500	μA
C _I	V _I = V _{CC} or GND	3.3 V		TBD		pF
C _O	V _O = V _{CC} or GND	3.3 V		TBD		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

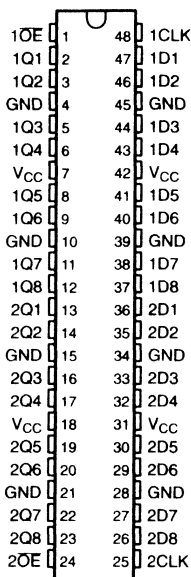
SN74ALVC16374

16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

JANUARY 1993

- Member of the Texas Instruments **Widebus™** Family
- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- Designed to Facilitate Incident Wave Switching for Line Impedances of 50 Ω or Greater
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages

DGG OR DL PACKAGE
(TOP VIEW)



description

This 16-bit edge-triggered D-type flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74ALVC16374 is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. It can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK) input, the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (\overline{OE}) input does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74ALVC16374 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16374 is characterized for operation from -40°C to 85°C .

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PRODUCT PREVIEW

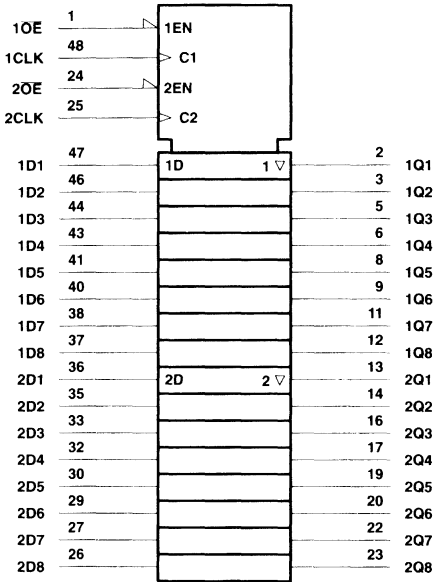
SN74ALVC16374
16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP
WITH 3-STATE OUTPUTS

JANUARY 1993

FUNCTION TABLE
 (each flip-flop)

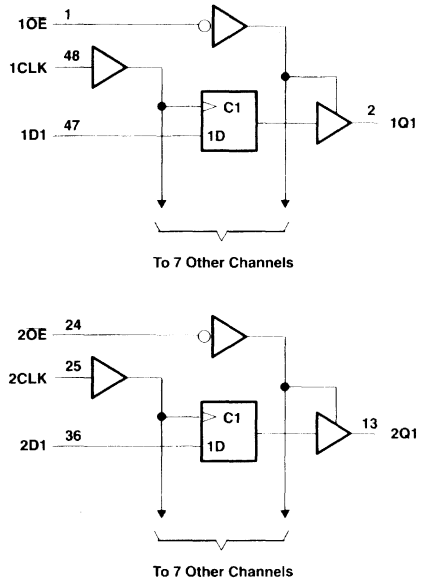
INPUTS			OUTPUT
OE	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q ₀
H	X	X	Z

logic symbol†



PRODUCT PREVIEW

logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN74ALVC16374

16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

JANUARY 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND pins	± 100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DGG package	0.6 W
DL package	0.85 W
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7$ V		-12
		$V_{CC} = 3$ V		-24 [‡]
I_{OL}	Low-level output current	$V_{CC} = 2.7$ V		12
		$V_{CC} = 3$ V		24 [‡]
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	-40	85	°C

NOTE 3: Unused or floating inputs must be held high or low.

[‡] Current duty cycle $\leq 50\%$, $f \leq 1$ kHz

PRODUCT PREVIEW

SN74ALVC16374
16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP
WITH 3-STATE OUTPUTS

JANUARY 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} [†]	MIN	TYP	MAX	UNIT
V _{IK}	I _I = -18 mA	2.7 V			-1.2	V
V _{OH}	I _{OH} = -100 μA	MIN to MAX	V _{CC} - 0.2			V
	I _{OH} = -12 mA	2.7 V	2.2			
		3 V	2.4			
	I _{OH} = -24 mA	3 V	2			
V _{OL}	I _{OL} = 100 μA	MIN to MAX			0.2	V
	I _{OL} = 12 mA	2.7 V			0.4	
		3 V			0.55	
	I _{OL} = 24 mA					
I _I	V _I = V _{CC} or GND	3.6 V			±5	μA
I _{OZ}	V _O = V _{CC} or GND	3.6 V			±10	μA
I _{CC}	V _I = V _{CC} or GND. I _O = 0	3.6 V			20	μA
ΔI _{CC}	V _{CC} = 3 V to 3.6 V. Other inputs at V _{CC} or GND. One input at V _{CC} - 0.6 V.				500	μA
C _I	V _I = V _{CC} or GND	3.3 V		TBD		pF
C _O	V _O = V _{CC} or GND	3.3 V		TBD		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

SN74ALVC16500

18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

JANUARY 1993

- Member of the Texas Instruments *Widebus™* Family
- *UBT™* (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode
- *EPIC™* (Enhanced-Performance Implanted CMOS) Submicron Process
- Designed to Facilitate Incident Wave Switching for Line Impedances of 50 Ω or Greater
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages

description

This 18-bit universal bus transceiver is designed for 2.7-V to 3.6-V V_{CC} operation.

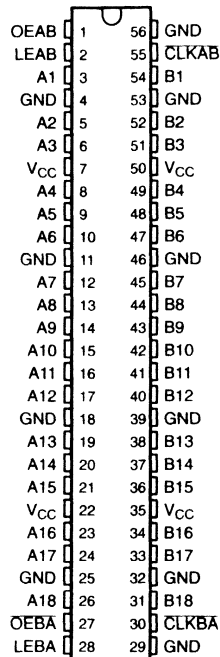
Data flow in each direction is controlled by output-enable (OEAB and $\overline{\text{OEBA}}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the high-to-low transition of CLKAB . Output-enable OEAB is active high. When OEAB is high, the B-port outputs are active. When OEAB is low, the B-port outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{\text{OEBA}}$, LEBA, and CLKBA . The output enables are complementary (OEAB is active high, and $\overline{\text{OEBA}}$ is active low).

The SN74ALVC16500 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16500 is characterized for operation from -40°C to 85°C .

DGG OR DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

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SN74ALVC16500
18-BIT UNIVERSAL BUS TRANSCEIVER
WITH 3-STATE OUTPUTS

JANUARY 1993

FUNCTION TABLE†

INPUTS				OUTPUT
OEAB	LEAB	CLKAB	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	B ₀ †
H	L	L	X	B ₀ §

† A-to-B data flow is shown; B-to-A flow is similar but uses OEBA, LEBA, and CLKBA.

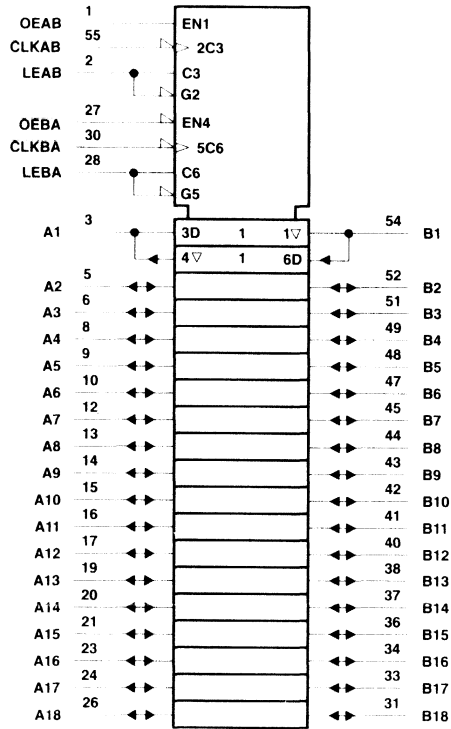
‡ Output level before the indicated steady-state input conditions were established.

§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low.

PRODUCT PREVIEW

SN74ALVC16500
18-BIT UNIVERSAL BUS TRANSCEIVER
WITH 3-STATE OUTPUTS
JANUARY 1993

logic symbol†



PRODUCT PREVIEW

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

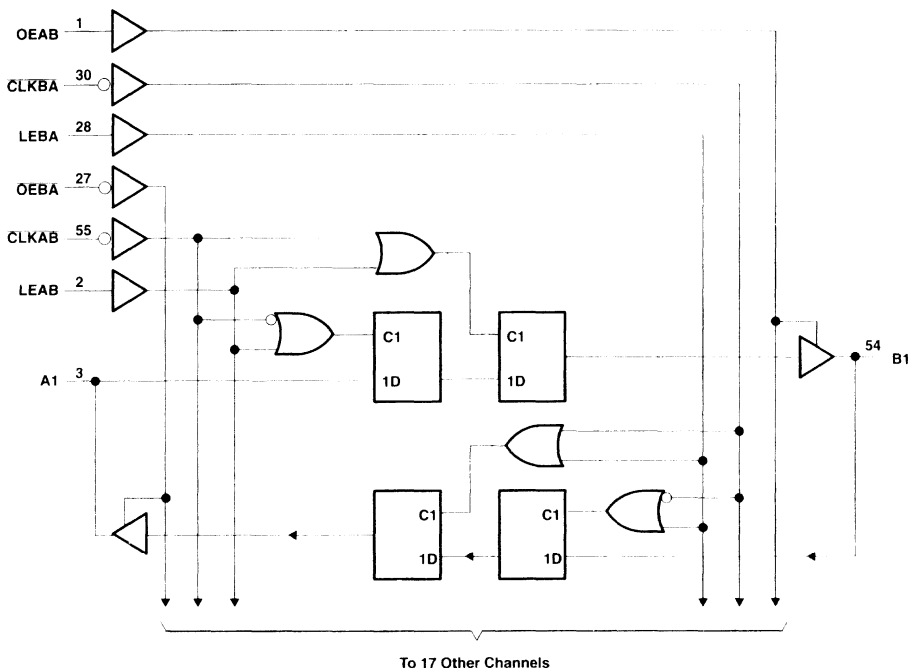
SN74ALVC16500

18-BIT UNIVERSAL BUS TRANSCEIVER

WITH 3-STATE OUTPUTS

JANUARY 1993

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†]

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1)	-0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air):	
DGG package	0.7 W
DL package	1 W
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This value is limited to 4.6 V maximum.

SN74ALVC16500
18-BIT UNIVERSAL BUS TRANSCEIVER
WITH 3-STATE OUTPUTS
 JANUARY 1993

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V _{CC}	Supply voltage	2.7	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V		V
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		V
V _I	Input voltage	0	V _{CC}	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2.7 V		mA
		V _{CC} = 3 V		
I _{OL}	Low-level output current	V _{CC} = 2.7 V		mA
		V _{CC} = 3 V		
Δt/Δv	Input transition rise or fall rate	0	10	ns/V
T _A	Operating free-air temperature	-40	85	°C

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.
 † Current duty cycle < 50%, f ≥ 1 kHz

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} [‡]	MIN	TYP	MAX	UNIT
V _{IK}	I _I = -18 mA	2.7 V			-1.2	V
V _{OH}	I _{OH} = -100 μA	MIN to MAX	V _{CC} - 0.2			V
	I _{OH} = -12 mA	2.7 V	2.2			
	I _{OH} = -24 mA	3 V	2.4			
V _{OL}	I _{OL} = 100 μA	MIN to MAX			0.2	V
	I _{OL} = 12 mA	2.7 V			0.4	
	I _{OL} = 24 mA	3 V			0.55	
I _I	V _I = V _{CC} or GND	3.6 V			±5	μA
I _{OZ} [§]	V _O = V _{CC} or GND	3.6 V			±10	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V			20	μA
ΔI _{CC}	V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND				500	μA
C _i	Control inputs V _I = V _{CC} or GND	3.3 V		TBD		pF
C _{io}	A or B ports V _O = V _{CC} or GND	3.3 V		TBD		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.
[§] For I/O ports, the parameter I_{OZ} includes the input leakage current.

PRODUCT PREVIEW



SN74ALVC16501

18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

JANUARY 1993

- Member of the Texas Instruments *Widebus™* Family
- **UBT™** (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode
- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- Designed to Facilitate Incent Wave Switching for Line Impedances of 50 Ω or Greater
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages

description

This 18-bit universal bus transceiver is designed for 2.7-V to 3.6-V V_{CC} operation.

Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses OEBA, LEBA, and CLKBA. The output enables are complementary (OEAB is active high, and OEBA is active low).

The SN74ALVC16501 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16501 is characterized for operation from -40°C to 85°C .

DGG OR DL PACKAGE
(TOP VIEW)

OEAB	1	56	GND
LEAB	2	55	CLKAB
A1	3	54	B1
GND	4	53	GND
A2	5	52	B2
A3	6	51	B3
V_{CC}	7	50	V_{CC}
A4	8	49	B4
A5	9	48	B5
A6	10	47	B6
GND	11	46	GND
A7	12	45	B7
A8	13	44	B8
A9	14	43	B9
A10	15	42	B10
A11	16	41	B11
A12	17	40	B12
GND	18	39	GND
A13	19	38	B13
A14	20	37	B14
A15	21	36	B15
V_{CC}	22	35	V_{CC}
A16	23	34	B16
A17	24	33	B17
GND	25	32	GND
A18	26	31	B18
OEBA	27	30	CLKBA
LEBA	28	29	GND

PRODUCT PREVIEW

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SN74ALVC16501
18-BIT UNIVERSAL BUS TRANSCEIVER
WITH 3-STATE OUTPUTS

JANUARY 1993

FUNCTION TABLE¹

INPUTS				OUTPUT	
OEAB	LEAB	CLKAB	A	B	B
L	X	X	X		Z
H	H	X	L		L
H	H	X	H		H
H	L	↑	L		L
H	L	↑	H		H
H	L	H	X		B ₀ [‡]
H	L	L	X		B ₀ [§]

¹ A-to-B data flow is shown; B-to-A flow is similar but uses OEBA, LEBA, and CLKBA.

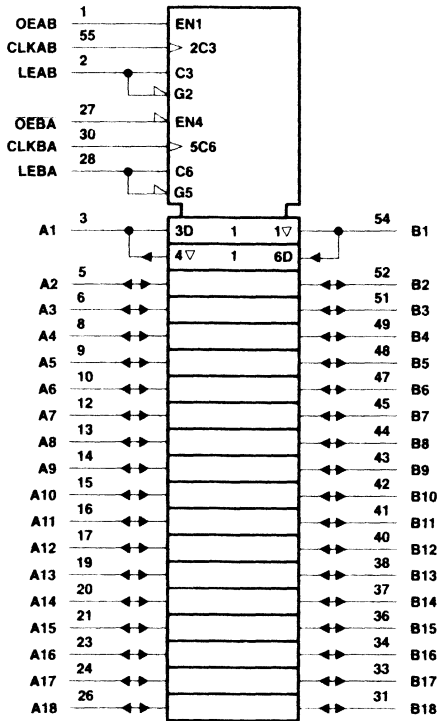
[‡] Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low.

[§] Output level before the indicated steady-state input conditions were established.

PRODUCT PREVIEW

SN74ALVC16501
18-BIT UNIVERSAL BUS TRANSCEIVER
WITH 3-STATE OUTPUTS
JANUARY 1993

logic symbol†



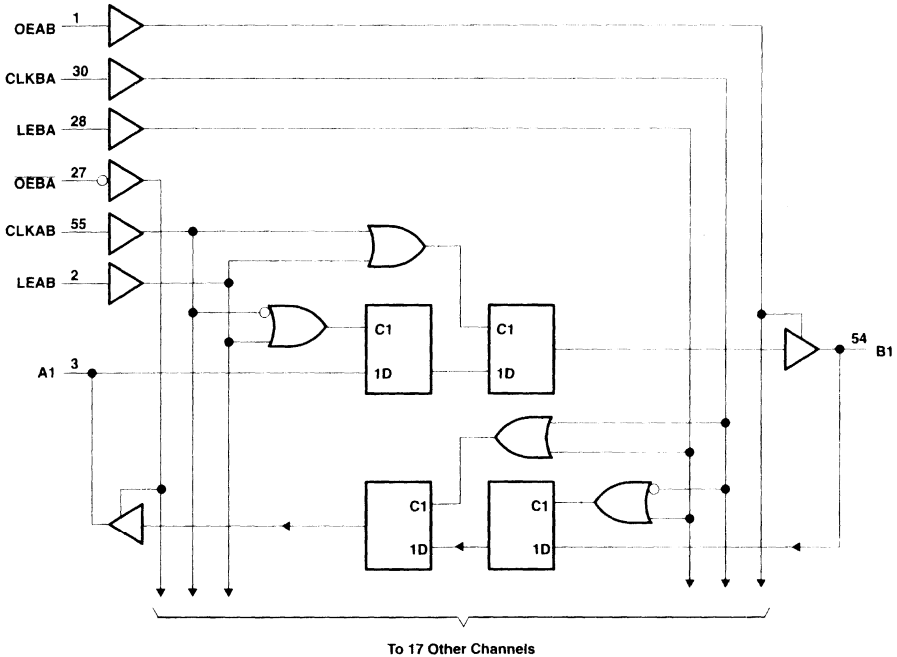
PRODUCT PREVIEW

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN74ALVC16501
18-BIT UNIVERSAL BUS TRANSCEIVER
WITH 3-STATE OUTPUTS

JANUARY 1993

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1)	-0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DGG package	0.7 W
DL package	1 W
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.



SN74ALVC16501
18-BIT UNIVERSAL BUS TRANSCEIVER
WITH 3-STATE OUTPUTS

JANUARY 1993

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V _{CC}	Supply voltage	2.7	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V		2
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8
V _I	Input voltage	0	V _{CC}	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2.7 V	-12	mA
		V _{CC} = 3 V	-24 [†]	
I _{OL}	Low-level output current	V _{CC} = 2.7 V	12	mA
		V _{CC} = 3 V	24 [†]	
ΔV/ΔV	Input transition rise or fall rate	0	10	ns/V
T _A	Operating free-air temperature	-40	85	°C

NOTE 3. Unused or floating pins (input or I/O) must be held high or low.

[†] Current duty cycle ≤ 50%, f ≥ 1 kHz

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} [‡]	MIN	TYP	MAX	UNIT
V _{IK}	I _I = -18 mA	2.7 V			-1.2	V
V _{OH}	I _{OH} = -100 μA	MIN to MAX	V _{CC} - 0.2			V
	I _{OH} = -12 mA	2.7 V	2.2			
	I _{OH} = -24 mA	3 V	2.4			
V _{OL}	I _{OH} = -24 mA	3 V	2			V
	I _{OL} = 100 μA	MIN to MAX			0.2	
	I _{OL} = 12 mA	2.7 V			0.4	
	I _{OL} = 24 mA	3 V			0.55	
I _I	V _I = V _{CC} or GND	3.6 V			±5	μA
I _{OZ} [§]	V _O = V _{CC} or GND	3.6 V			±10	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V			20	μA
ΔI _{CC}	V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND				500	μA
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V		TBD	pF
C _{io}	A or B ports	V _O = V _{CC} or GND	3.3 V		TBD	pF

[‡] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

[§] For I/O ports, the parameter I_{OZ} includes the input leakage current.

PRODUCT PREVIEW

SN74ALVC16543 16-BIT REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

JANUARY 1993

- Member of the Texas Instruments *Widebus™* Family
- *EPIC™* (Enhanced-Performance Implanted CMOS) Submicron Process
- Designed to Facilitate Incident Wave Switching for Line Impedances of 50 Ω or Greater
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages

description

This 16-bit registered transceiver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74ALVC16543 can be used as two 8-bit transceivers or one 16-bit transceiver. Separate latch-enable (LEAB or LEBA) and output-enable (OEAB or OEBA) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable (CEAB) input must be low in order to enter data from A or to output data from B. If CEAB is low and LEAB is low, the A-to-B latches are transparent; a subsequent low-to-high transition of LEAB puts the A latches in the storage mode. With CEAB and OEAB both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the CEBA, LEBA, and OEBA inputs.

The SN74ALVC16543 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16543 is characterized for operation from -40°C to 85°C .

DGG OR DL PACKAGE
(TOP VIEW)

1OEAB	1	56	1OEBA
1LEAB	2	55	1LEBA
1CEAB	3	54	1CEBA
GND	4	53	GND
1A1	5	52	1B1
1A2	6	51	1B2
V_{CC}	7	50	V_{CC}
1A3	8	49	1B3
1A4	9	48	1B4
1A5	10	47	1B5
GND	11	46	GND
1A6	12	45	1B6
1A7	13	44	1B7
1A8	14	43	1B8
2A1	15	42	2B1
2A2	16	41	2B2
2A3	17	40	2B3
GND	18	39	GND
2A4	19	38	2B4
2A5	20	37	2B5
2A6	21	36	2B6
V_{CC}	22	35	V_{CC}
2A7	23	34	2B7
2A8	24	33	2B8
GND	25	32	GND
2CEAB	26	31	2CEBA
2LEAB	27	30	2LEBA
2OEAB	28	29	2OEBA

PRODUCT PREVIEW

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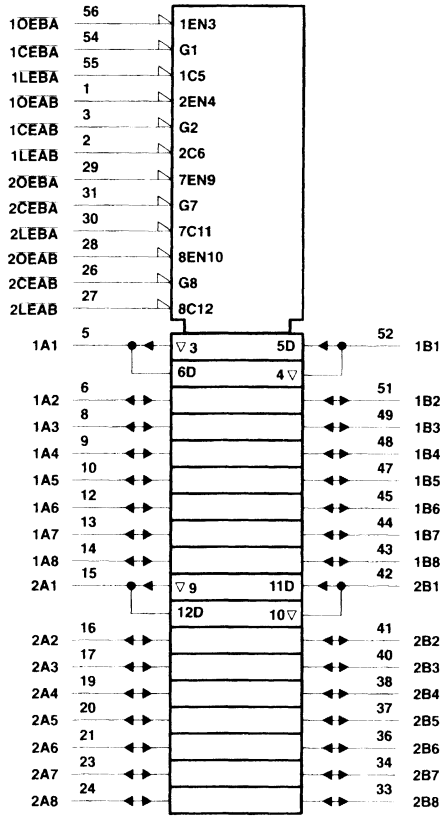
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SN74ALVC16543
16-BIT REGISTERED TRANSCEIVER
WITH 3-STATE OUTPUTS
 JANUARY 1993

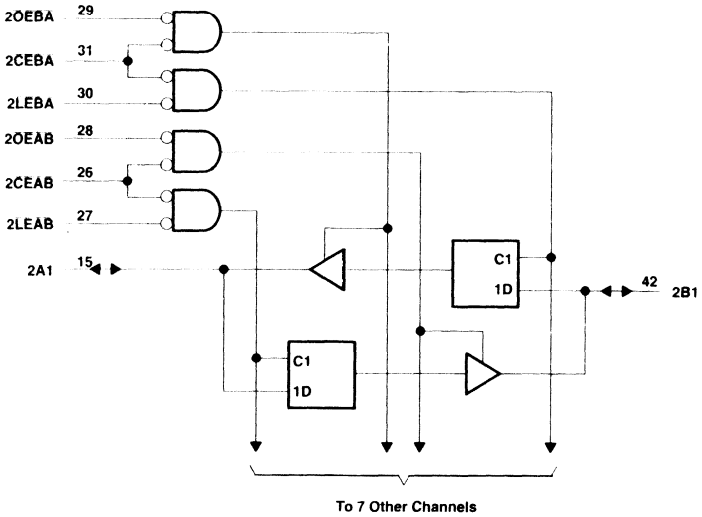
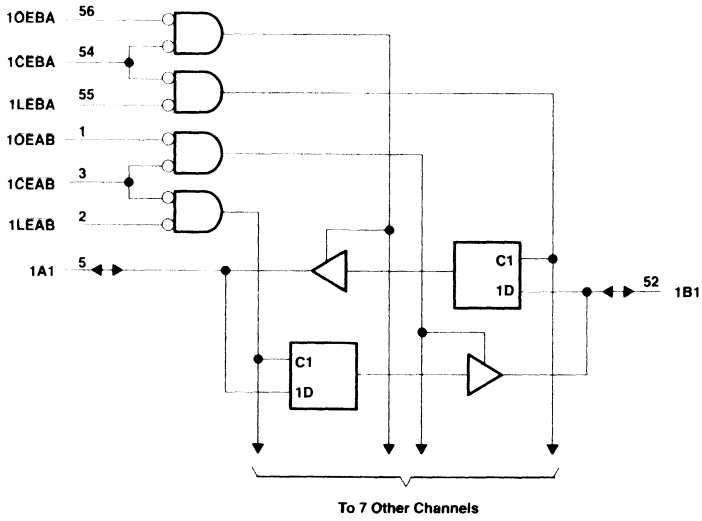
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

logic diagram (positive logic)



PRODUCT PREVIEW

SN74ALVC16543
16-BIT REGISTERED TRANSCEIVER
WITH 3-STATE OUTPUTS
 JANUARY 1993

FUNCTION TABLE†
 (each 8-bit section)

INPUTS				OUTPUT B
CEAB	LEAB	OEAB	A	
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B ₀ ‡
L	L	L	L	L
L	L	L	H	H

† A-to-B data flow is shown; B-to-A flow control is the same except that it uses CEBA, LEBA, and OEBA.

‡ Output level before the indicated steady-state input conditions were established.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1)	-0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DGG package	0.7 W
DL package	1 W
Storage temperature range	-65°C to 150°C

§ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7$ V	-12	mA
		$V_{CC} = 3$ V	-24‡	
I_{OL}	Low-level output current	$V_{CC} = 2.7$ V	12	mA
		$V_{CC} = 3$ V	24‡	
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	-40	85	°C

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.

‡ Current duty cycle ≤ 50%, $f \geq 1$ kHz



SN74ALVC16543
16-BIT REGISTERED TRANSCEIVER
WITH 3-STATE OUTPUTS

JANUARY 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}^\dagger	MIN	TYP	MAX	UNIT
V_{IK}		$I_I = -18 \text{ mA}$	2.7 V			-1.2	V
V_{OH}		$I_{OH} = -100 \mu\text{A}$	MIN to MAX	$V_{CC} - 0.2$			V
		$I_{OH} = -12 \text{ mA}$	2.7 V	2.2			
		$I_{OH} = -24 \text{ mA}$	3 V	2.4			
V_{OL}		$I_{OH} = -24 \text{ mA}$	3 V	2			V
		$I_{OL} = 100 \mu\text{A}$	MIN to MAX	0.2			
		$I_{OL} = 12 \text{ mA}$	2.7 V	0.4			
	$I_{OL} = 24 \text{ mA}$	3 V	0.55				
I_I		$V_I = V_{CC}$ or GND	3.6 V			± 5	μA
I_{OZ}^\ddagger		$V_O = V_{CC}$ or GND	3.6 V			± 10	μA
I_{CC}		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			20	μA
ΔI_{CC}		$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$, Other inputs at V_{CC} or GND				500	μA
C_i	Control inputs	$V_I = V_{CC}$ or GND	3.3 V		TBD		pF
C_o	A or B ports	$V_O = V_{CC}$ or GND	3.3 V		TBD		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

PRODUCT PREVIEW

SN74ALVC16600

18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

JANUARY 1993

- Member of the Texas Instruments *Widebus™* Family
- *UBT™* (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, or Clock-Enabled Mode
- *EPIC™* (Enhanced-Performance Implanted CMOS) Submicron Process
- Designed to Facilitate Incident Wave Switching for Line Impedances of 50 Ω or Greater
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages

description

This 18-bit universal bus transceiver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74ALVC16600 combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

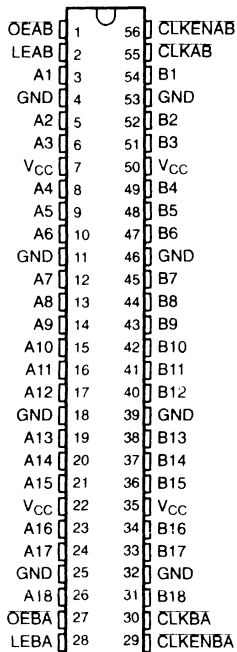
Data flow in each direction is controlled by output-enable (\overline{OEAB} and \overline{OEBA}), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock can be controlled by the clock-enable (CLKENAB and CLKENBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the high-to-low transition of CLKAB. Output enable \overline{OEAB} is active low. When \overline{OEAB} is low, the outputs are active. When \overline{OEAB} is high, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses \overline{OEBA} , LEBA, CLKBA, and CLKENBA.

The SN74ALVC16600 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16600 is characterized for operation from -40°C to 85°C .

DGG OR DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

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SN74ALVC16600
18-BIT UNIVERSAL BUS TRANSCEIVER
WITH 3-STATE OUTPUTS

JANUARY 1993

FUNCTION TABLE[†]

INPUTS					OUTPUT
CLKENAB	OEAB	LEAB	CLKAB	A	B
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B ₀ [‡]
H	L	L	X	X	B ₀ [‡]
L	L	L	↓	L	L
L	L	L	↓	H	H
L	L	L	H	X	B ₀ [‡]
L	L	L	L	X	B ₀ [§]

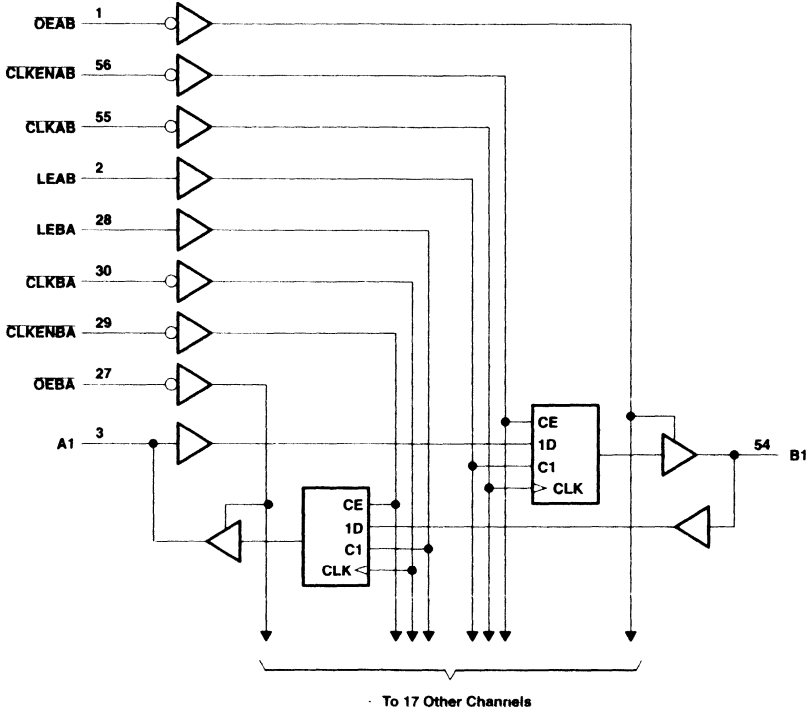
[†] A-to-B data flow is shown: B-to-A flow is similar but uses OEBA, LEBA, CLKBA, and CLKENBA.

[‡] Output level before the indicated steady-state input conditions were established.

[§] Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low.

PRODUCT PREVIEW

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1)	-0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND pins	± 100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DGG package	0.7 W
..... DL package	1 W
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.

SN74ALVC16600
18-BIT UNIVERSAL BUS TRANSCEIVER
WITH 3-STATE OUTPUTS

JANUARY 1993

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V _{CC}	Supply voltage	2.7	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V		V
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		V
V _I	Input voltage	0	V _{CC}	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2.7 V		-12
		V _{CC} = 3 V		-24†
I _{OL}	Low-level output current	V _{CC} = 2.7 V		12
		V _{CC} = 3 V		24†
Δt/Δv	Input transition rise or fall rate	0	10	ns/V
T _A	Operating free-air temperature	-40	85	°C

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.

† Current duty cycle ≤ 50%, f ≥ 1 kHz

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} ‡	MIN	TYP	MAX	UNIT
V _{IK}	I _i = -18 mA	2.7 V			-1.2	V
V _{OH}	I _{OH} = -100 μA	MIN to MAX	V _{CC} - 0.2			V
	I _{OH} = -12 mA	2.7 V	2.2			
	I _{OH} = -24 mA	3 V	2.4			
V _{OL}	I _{OL} = 100 μA	MIN to MAX			0.2	V
	I _{OL} = 12 mA	2.7 V			0.4	
	I _{OL} = 24 mA	3 V			0.55	
I _i	V _i = V _{CC} or GND	3.6 V			+5	μA
I _{OZ} §	V _O = V _{CC} or GND	3.6 V			+10	μA
I _{CC}	V _i = V _{CC} or GND, I _O = 0	3.6 V			20	μA
ΔI _{CC}	V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND				500	μA
C _i	Control inputs, V _i = V _{CC} or GND	3.3 V		TBD		pF
C _{io}	A or B ports, V _O = V _{CC} or GND	3.3 V		TBD		pF

‡ For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

§ For I/O ports, the parameter I_{OZ} includes the input leakage current.

PRODUCT PREVIEW

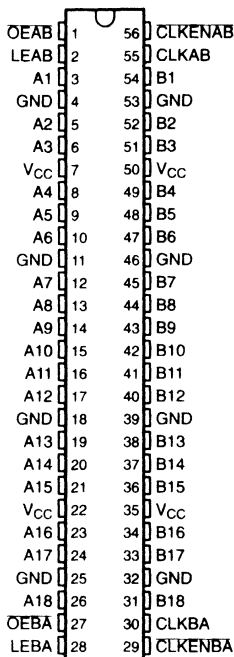


SN74ALVC16601 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

JANUARY 1993

- Member of the Texas Instruments *Widebus™* Family
- *UBT™* (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, or Clock-Enabled Mode
- *EPIC™* (Enhanced-Performance Implanted CMOS) Submicron Process
- Designed to Facilitate Incident Wave Switching for Line Impedances of 50 Ω or Greater
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages

DGG OR DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

This 18-bit universal bus transceiver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74ALVC16601 combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable (\overline{OEAB} and \overline{OEBA}), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock can be controlled by the clock-enable (CLKENAB and CLKENBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the high-to-low transition of CLKAB. Output enable \overline{OEAB} is active low. When \overline{OEAB} is low, the outputs are active. When \overline{OEAB} is high, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses \overline{OEBA} , LEBA, CLKBA, and CLKENBA.

The SN74ALVC16601 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16601 is characterized for operation from -40°C to 85°C .

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SN74ALVC16601
18-BIT UNIVERSAL BUS TRANSCEIVER
WITH 3-STATE OUTPUTS

JANUARY 1993

FUNCTION TABLE[†]

INPUTS					OUTPUT
CLKENAB	OEAB	LEAB	CLKAB	A	B
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B ₀ [‡]
H	L	L	X	X	B ₀ [‡]
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	L	L	X	B ₀ [‡]
L	L	L	H	X	B ₀ [§]

[†] A-to-B data flow is shown: B-to-A flow is similar but uses OEBA, LEBA, CLKBA, and CLKENBA.

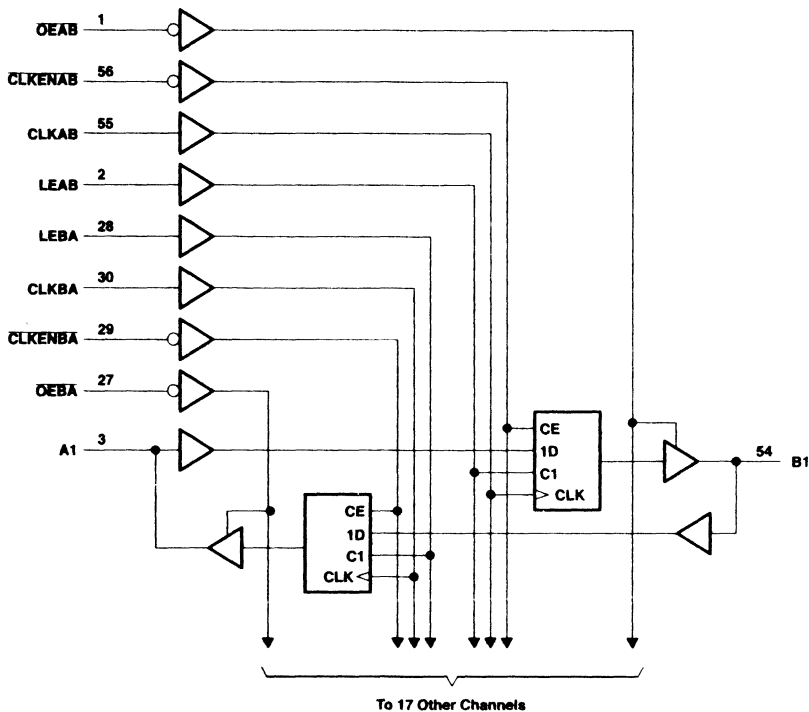
[‡] Output level before the indicated steady-state input conditions were established.

[§] Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low.

PRODUCT PREVIEW

SN74ALVC16601
18-BIT UNIVERSAL BUS TRANSCEIVER
WITH 3-STATE OUTPUTS
 JANUARY 1993

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1)	-0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND pins	± 100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DGG package	0.7 W
..... DL package	1 W
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.

SN74ALVC16601
18-BIT UNIVERSAL BUS TRANSCEIVER
WITH 3-STATE OUTPUTS
 JANUARY 1993

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V _{CC}	Supply voltage	2.7	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V		V
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		V
V _I	Input voltage	0	V _{CC}	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2.7 V		-12
		V _{CC} = 3 V		-24†
I _{OL}	Low-level output current	V _{CC} = 2.7 V		12
		V _{CC} = 3 V		24†
ΔV/Δv	Input transition rise or fall rate	0	10	ns/V
T _A	Operating free-air temperature	-40	85	C

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.
 † Current duty cycle ≤ 50%, f ≥ 1 kHz

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} ‡	MIN	TYP	MAX	UNIT
V _{IK}	I _I = -18 mA	2.7 V			-1.2	V
V _{OH}	I _{OH} = -100 μA	MIN to MAX	V _{CC} - 0.2			V
	I _{OH} = -12 mA	2.7 V	2.2			
		3 V	2.4			
	I _{OH} = -24 mA	3 V	2			
V _{OL}	I _{OL} = 100 μA	MIN to MAX			0.2	V
	I _{OL} = 12 mA	2.7 V			0.4	
	I _{OL} = 24 mA	3 V			0.55	
I _I	V _I = V _{CC} or GND	3.6 V			±5	μA
I _{OZ} §	V _O = V _{CC} or GND	3.6 V			±10	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V			20	μA
ΔI _{CC}	V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND				500	μA
C _I	Control inputs V _I = V _{CC} or GND	3.3 V		TBD		pF
C _{IO}	A or B ports V _O = V _{CC} or GND	3.3 V		TBD		pF

‡ For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

§ For I/O ports, the parameter I_{OZ} includes the input leakage current.

PRODUCT PREVIEW



SN74ALVC16646 16-BIT BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

JANUARY 1993

- Member of the Texas Instruments *Widebus™* Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Designed to Facilitate Incident Wave Switching for Line Impedances of 50 Ω or Greater
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages

description

This 16-bit bus transceiver and register is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74ALVC16646 can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the SN74ALVC16646.

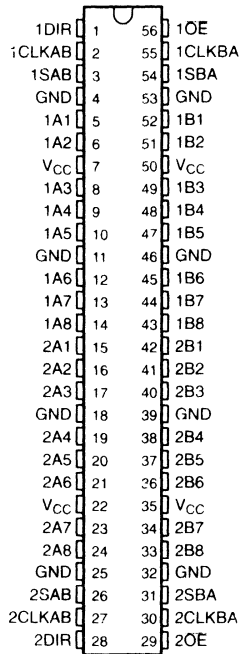
Output-enable (OE) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. The direction control (DIR) determines which bus receives data when OE is low. In the isolation mode (OE high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

The SN74ALVC16646 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16646 is characterized for operation from -40°C to 85°C .

DGG OR DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

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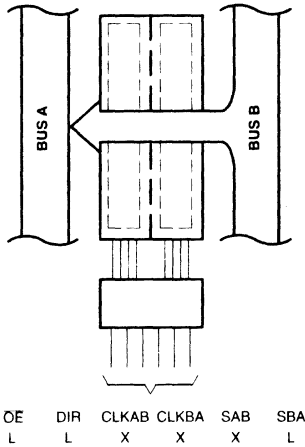


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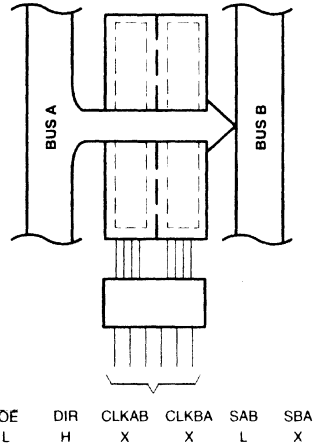
SN74ALVC16646
16-BIT BUS TRANSCEIVER AND REGISTER
WITH 3-STATE OUTPUTS

JANUARY 1993

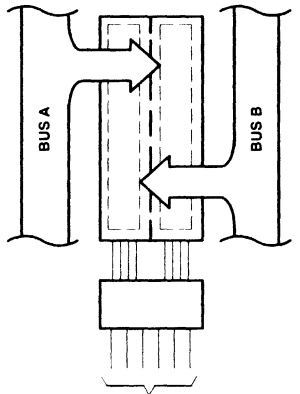
PRODUCT PREVIEW



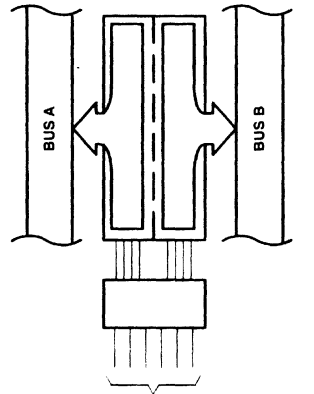
REAL-TIME TRANSFER
BUS B TO BUS A



REAL-TIME TRANSFER
BUS A TO BUS B



STORAGE FROM
A, B, OR A AND B



TRANSFER STORED DATA
TO A AND/OR B

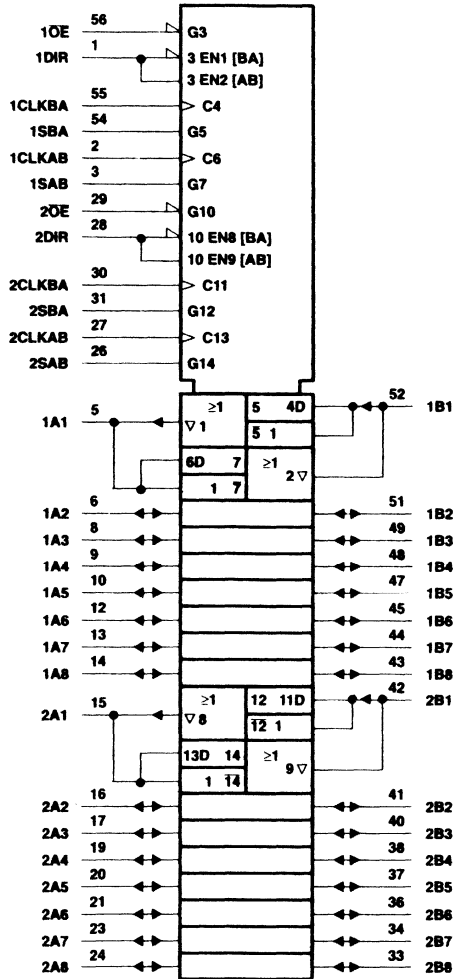
OE	DIR	CLKAB	CLKBA	SAB	SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

OE	DIR	CLKAB	CLKBA	SAB	SBA
L	L	X	L	X	H
L	H	L	X	H	X

Figure 1. Bus-Management Functions

SN74ALVC16646
16-BIT BUS TRANSCEIVER AND REGISTER
WITH 3-STATE OUTPUTS
JANUARY 1993

logic symbol

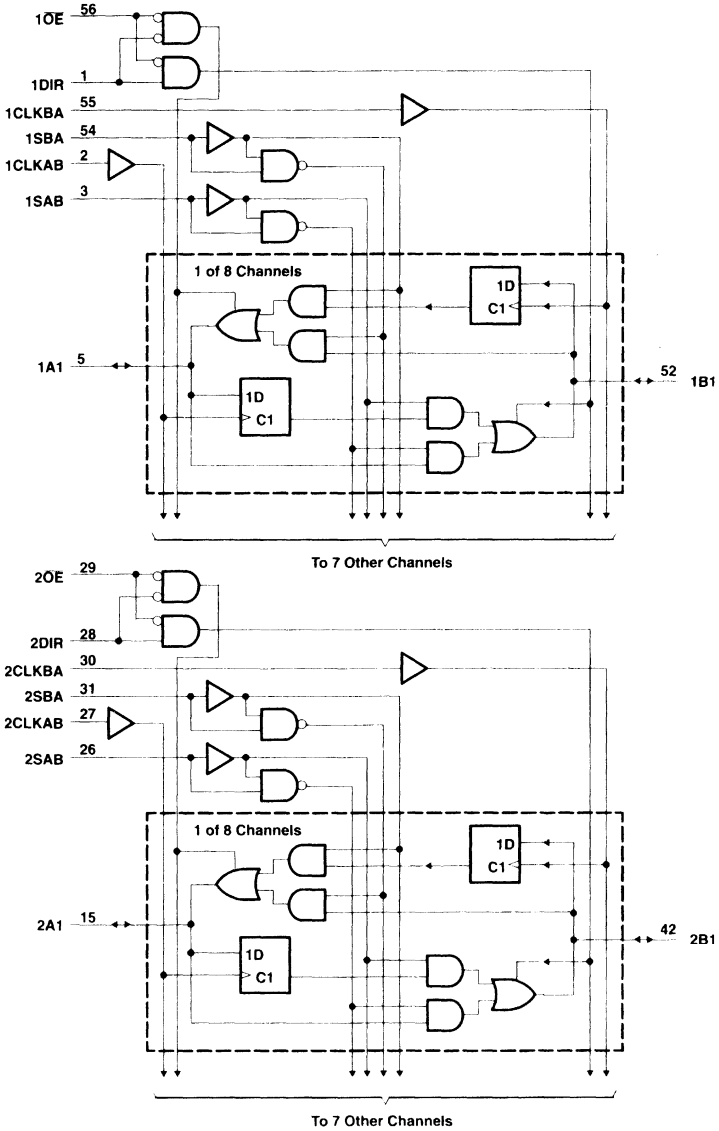


PRODUCT PREVIEW

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN74ALVC16646
16-BIT BUS TRANSCEIVER AND REGISTER
WITH 3-STATE OUTPUTS
 JANUARY 1993

logic diagram (positive logic)



PRODUCT PREVIEW

SN74ALVC16646

16-BIT BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

JANUARY 1993

FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION
OE	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	↑	X	X	X	input	Unspecified [†]	Store A, B unspecified [†]
X	X	X	↑	X	X	Unspecified [†]	Input	Store B, A unspecified [†]
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	L	L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	L	X	H	X	Input	Output	Stored A data to B bus

[†] The data output functions may be enabled or disabled by various signals at the OE and DIR inputs. Data input functions are always enabled. i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[‡]

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1)	-0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DGG package	0.7 W
DL package	1 W
Storage temperature range	-65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7$ V		-12
		$V_{CC} = 3$ V		-24 [§]
I_{OL}	Low-level output current	$V_{CC} = 2.7$ V		12
		$V_{CC} = 3$ V		24 [§]
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	-40	85	°C

NOTE 3. Unused or floating pins (input or I/O) must be held high or low.

[§] Current duty cycle < 50%, $f > 1$ kHz

PRODUCT PREVIEW

SN74ALVC16646
16-BIT BUS TRANSCEIVER AND REGISTER
WITH 3-STATE OUTPUTS

JANUARY 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC} [†]	MIN	TYP	MAX	UNIT
V _{IK}		I _I = -18 mA	2.7 V			-1.2	V
V _{OH}		I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2			V
		I _{OH} = -12 mA	2.7 V	2.2			
		I _{OH} = -24 mA	3 V	2.4			
V _{OL}		I _{OL} = 100 μA	MIN to MAX			0.2	V
		I _{OL} = 12 mA	2.7 V			0.4	
		I _{OL} = 24 mA	3 V			0.55	
I _I		V _I = V _{CC} or GND	3.6 V			±5	μA
I _{OZ} [‡]		V _O = V _{CC} or GND	3.6 V			±10	μA
I _{CC}		V _I = V _{CC} or GND, I _O = 0	3.6 V			20	μA
ΔI _{CC}		V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND				500	μA
C _I	Control inputs	V _I = V _{CC} or GND	3.3 V		TBD		pF
C _{I/O}	A or B ports	V _O = V _{CC} or GND	3.3 V		TBD		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

PRODUCT PREVIEW

SN74ALVC16652

16-BIT BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

JANUARY 1993

- Member of the Texas Instruments *Widebus™* Family
- *EPIC™* (Enhanced-Performance Implanted CMOS) Submicron Process
- Designed to Facilitate Incident Wave Switching for Line Impedances of 50 Ω or Greater
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages

DGG OR DL PACKAGE
(TOP VIEW)

1OEAB	1	56	1OEBA
1CLKAB	2	55	1CLKBA
1SAB	3	54	1SBA
GND	4	53	GND
1A1	5	52	1B1
1A2	6	51	1B2
V_{CC}	7	50	V_{CC}
1A3	8	49	1B3
1A4	9	48	1B4
1A5	10	47	1B5
GND	11	46	GND
1A6	12	45	1B6
1A7	13	44	1B7
1A8	14	43	1B8
2A1	15	42	2B1
2A2	16	41	2B2
2A3	17	40	2B3
GND	18	39	GND
2A4	19	38	2B4
2A5	20	37	2B5
2A6	21	36	2B6
V_{CC}	22	35	V_{CC}
2A7	23	34	2B7
2A8	24	33	2B8
GND	25	32	GND
2SAB	26	31	2SBA
2CLKAB	27	30	2CLKBA
2OEAB	28	29	2OEBA

description

This 16-bit bus transceiver and register is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74ALVC16652 consists of D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. The device can be used as two 8-bit transceivers or one 16-bit transceiver.

Complementary output-enable (OEAB and OEBA) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high input level selects stored data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the SN74ALVC16652.

Data on the A or B bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the levels on the select-control or output-enable inputs. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and OEBA. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus line are at high impedance, each set of bus lines remains at its last level configuration.

The SN74ALVC16652 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16652 is characterized for operation from -40°C to 85°C .

PRODUCT PREVIEW

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SN74ALVC16652
16-BIT BUS TRANSCEIVER AND REGISTER
WITH 3-STATE OUTPUTS
 JANUARY 1993

PRODUCT PREVIEW

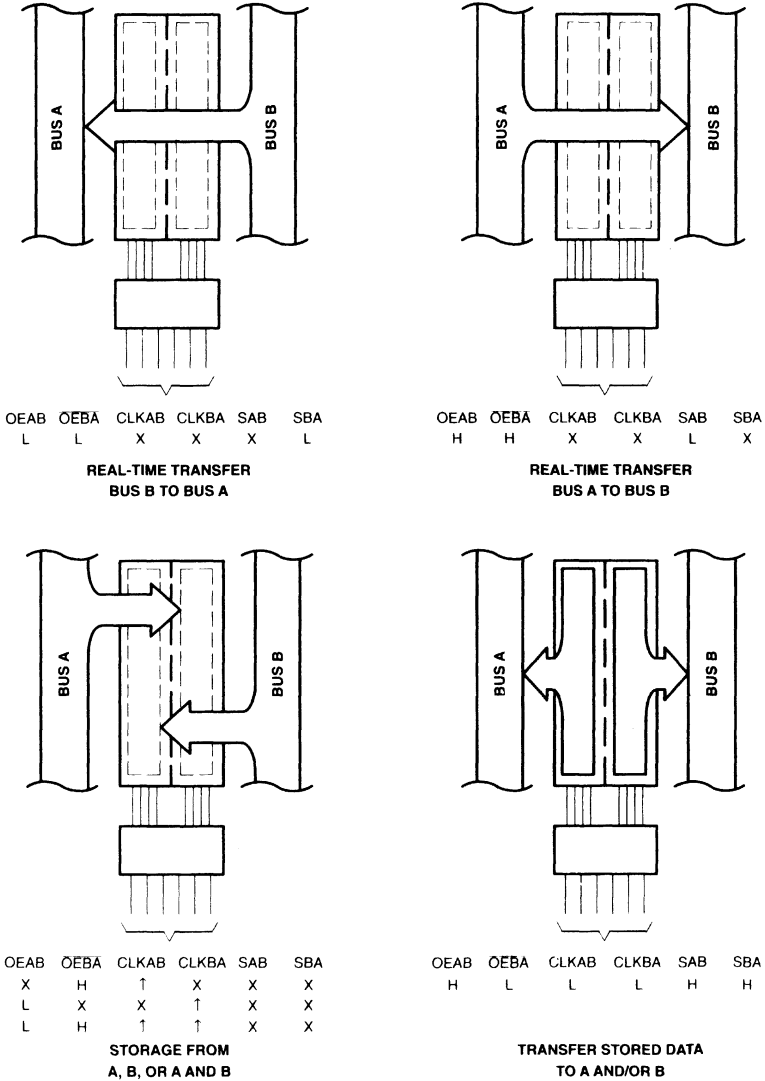
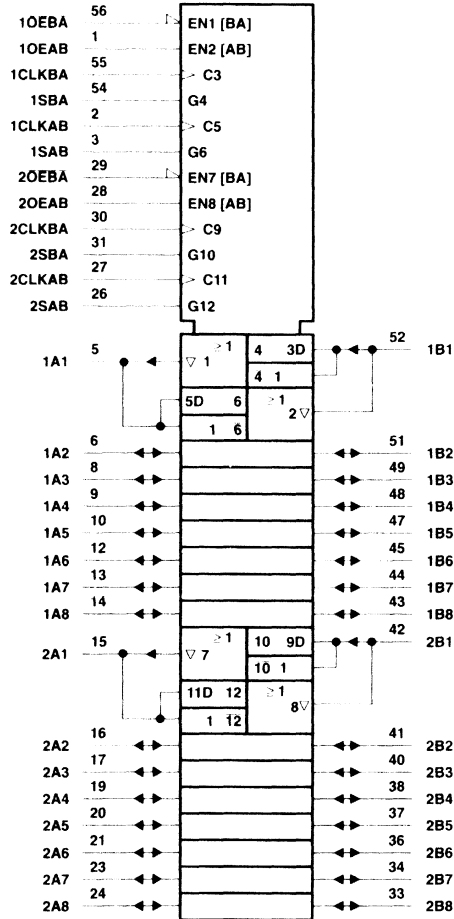


Figure 1. Bus-Management Functions

SN74ALVC16652
16-BIT BUS TRANSCEIVER AND REGISTER
WITH 3-STATE OUTPUTS
JANUARY 1993

logic symbol†

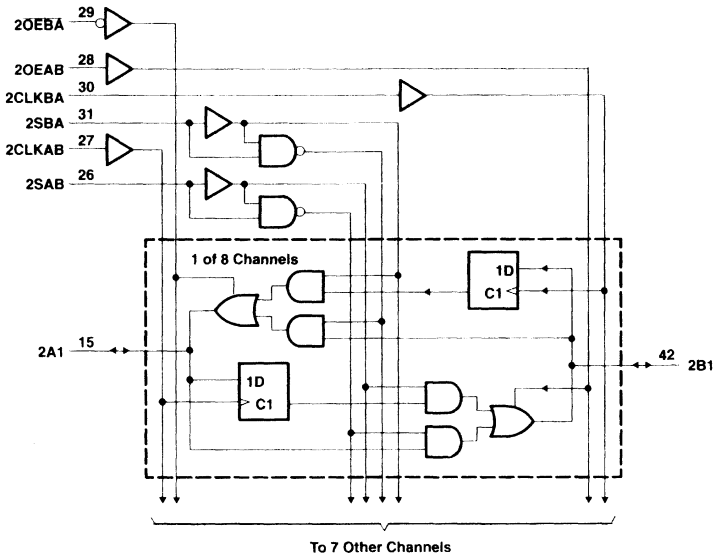
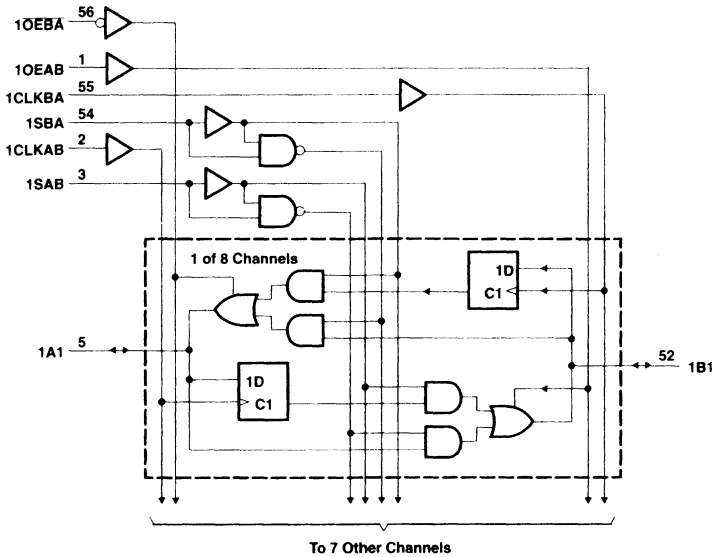


PRODUCT PREVIEW

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN74ALVC16652
16-BIT BUS TRANSCEIVER AND REGISTER
WITH 3-STATE OUTPUTS
 JANUARY 1993

logic diagram (positive logic)



PRODUCT PREVIEW



SN74ALVC16652
16-BIT BUS TRANSCEIVER AND REGISTER
WITH 3-STATE OUTPUTS

JANUARY 1993

FUNCTION TABLE

INPUTS						DATA I/O [†]		OPERATION OR FUNCTION
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
L	H	L	L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	L	X	X	Input	Unspecified [‡]	Store A, hold B
H	H	↑	↑	X [†]	X	Input	Output	Store A in both registers
L	X	L	↑	X	X	Unspecified [‡]	Input	Hold A, store B
L	L	↑	↑	X	X [†]	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	L	X	H	X	Input	Output	Stored A data to B bus
H	L	L	L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

[†] The data output functions may be enabled or disabled by a variety of level combinations at the OEAB or OEBA inputs. Data input functions are always enabled, i.e., data at the bus pins is stored on every low-to-high transition on the clock inputs.

[‡] Select control = L, clocks can occur simultaneously

Select control = H, clocks must be staggered in order to load both registers.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[§]

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1)	-0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DGG package	0.7 W
DL package	1 W
Storage temperature range	-65°C to 150°C

[§] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This value is limited to 4.6 V maximum.

PRODUCT PREVIEW

SN74ALVC16652
16-BIT BUS TRANSCEIVER AND REGISTER
WITH 3-STATE OUTPUTS

JANUARY 1993

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V _{CC}	Supply voltage	2.7	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V		V
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		V
V _I	Input voltage	0	V _{CC}	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2.7 V		-12
		V _{CC} = 3 V		-24 [†]
I _{OL}	Low-level output current	V _{CC} = 2.7 V		12
		V _{CC} = 3 V		24 [†]
Δt/Δv	Input transition rise or fall rate	0	10	ns/V
T _A	Operating free-air temperature	-40	85	C

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.

[†] Current duty cycle ≤ 50%, f ≥ 1 kHz

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} [‡]	MIN	TYP	MAX	UNIT
V _{IK}	I _I = -18 mA	2.7 V			-1.2	V
V _{OH}	I _{OH} = -100 μA	MIN to MAX	V _{CC} - 0.2			V
	I _{OH} = -12 mA	2.7 V	2.2			
		3 V	2.4			
	I _{OH} = -24 mA	3 V	2			
V _{OL}	I _{OL} = 100 μA	MIN to MAX			0.2	V
	I _{OL} = 12 mA	2.7 V			0.4	
	I _{OL} = 24 mA	3 V			0.55	
I _I	V _I = V _{CC} or GND	3.6 V			+5	μA
I _{OZ} [§]	V _O = V _{CC} or GND	3.6 V			+10	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V			20	μA
ΔI _{CC}	V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND				500	μA
C _i	Control inputs, V _I = V _{CC} or GND	3.3 V		TBD		pF
C _{io}	A or B ports, V _O = V _{CC} or GND	3.3 V		TBD		pF

[‡] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

[§] For I/O ports, the parameter I_{OZ} includes the input leakage current.

PRODUCT PREVIEW

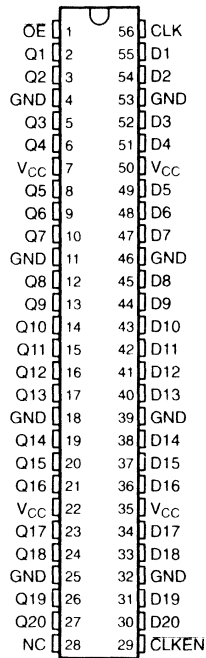


SN74ALVC16721
3.3-V 20-BIT FLIP-FLOP
WITH 3-STATE OUTPUTS

MARCH 1993

- Member of the Texas Instruments *Widebus*™ Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25$ C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25$ C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages

DGG OR DL PACKAGE
(TOP VIEW)



description

This 20-bit flip-flop is designed specifically for low-voltage 3.3-V V_{CC} operation.

The SN74ALVC16721's twenty flip-flops are edge-triggered D-type flip-flops with qualified clock storage. On the positive transition of the clock (CLK) input, the device provides true data at the Q outputs, provided that the clock-enable (CLKEN) input is low. If CLKEN is high, no data is stored.

A buffered output-enable (OE) input can be used to place the ten outputs in either a normal logic state (high or low level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (OE) input does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVC16721 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16721 is characterized for operation from -40°C to 85°C.

PRODUCT PREVIEW

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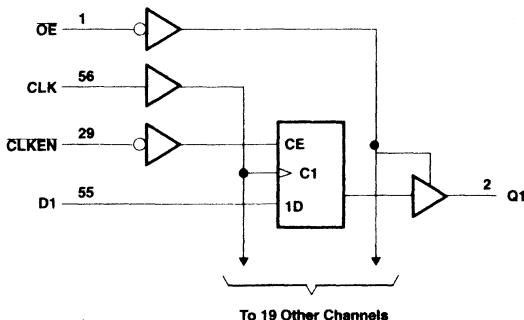
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SN74ALVC16721
3.3-V 20-BIT FLIP-FLOP
WITH 3-STATE OUTPUTS
 MARCH 1993

FUNCTION TABLE
 (each flip-flop)

INPUTS				OUTPUT
OE	CLKEN	CLK	D	Q
L	H	X	H	Q ₀
L	L	↑	H	H
L	L	↑	L	L
L	L	L	X	Q ₀
H	X	X	X	Z

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air):	
DGG package	0.7 W
DL package	1 W
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V _{CC}	Supply voltage	2.7	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V		2
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8
V _I	Input voltage	0	V _{CC}	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2.7 V		-12
		V _{CC} = 3 V		-24†
I _{OL}	Low-level output current	V _{CC} = 2.7 V		12
		V _{CC} = 3 V		24†
Δt/Δv	Input transition rise or fall rate	0	10	ns/V
T _A	Operating free-air temperature	-40	85	°C

NOTE 3: Unused or floating inputs must be held high or low.

† Current duty cycle ≤ 50%, f ≥ 1 kHz

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC} ‡	MIN	TYP	MAX	UNIT
V _{IK}	I _I = -18 mA		2.7 V			-1.2	V
V _{OH}	I _{OH} = -100 μA		MIN to MAX	V _{CC} - 0.2			V
	I _{OH} = -12 mA		2.7 V	2.2			
			3 V	2.4			
V _{OL}	I _{OH} = -24 mA		3 V	2			V
	I _{OL} = 100 μA		MIN to MAX	0.2			
	I _{OL} = 12 mA		2.7 V	0.4			
V _{OL}	I _{OL} = 24 mA		3 V	0.55			V
I _I	V _I = V _{CC} or GND		3.6 V	±5		μA	
I _{OZ}	V _O = V _{CC} or GND		3.6 V	±10		μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0		3.6 V	20		μA	
ΔI _{CC}	V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC} or GND		One input at V _{CC} - 0.6 V.		500	μA	
C _I	V _I = V _{CC} or GND		3.3 V	4		pF	
C _O	V _O = V _{CC} or GND		3.3 V	6		pF	

‡ For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		V _{CC} = 3.3 V ± 0.15 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	0	150	0	150	0	150	MHz
t _w	Pulse duration, CLK high or low							ns
t _{su}	Setup time	Data before CLK↑	High or low	3				ns
		CLKEN before CLK↑	High or low	3				
t _h	Hold time	Data after CLK↑	High or low	0				ns
		CLKEN after CLK↑	High or low	0				

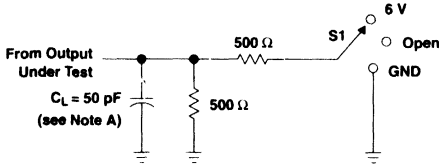
SN74ALVC16721
3.3-V 20-BIT FLIP-FLOP
WITH 3-STATE OUTPUTS
MARCH 1993

switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

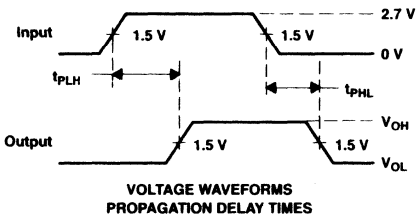
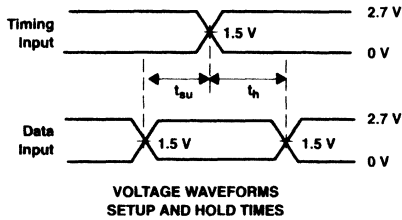
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3 V \pm 0.15 V$		$V_{CC} = 3.3 V \pm 0.3 V$		$V_{CC} = 2.7 V$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			150		150		150		MHz
t_{PLH}	CLK	Q	4		4.5				ns
t_{PHL}			4		4.5				
t_{PZH}	OE	Q	5		5.7				ns
t_{PZL}			5		5.7				
t_{PHZ}	OE	Q	4.5		4.5				ns
t_{PLZ}			4.5		4.5				

PRODUCT PREVIEW

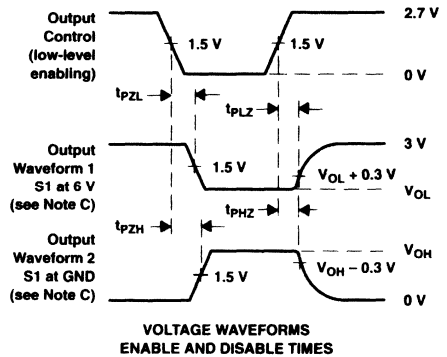
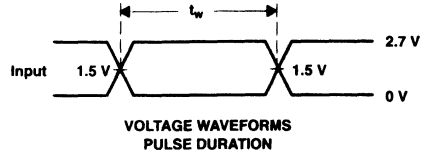
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR OUTPUTS



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



PRODUCT PREVIEW

- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- Member of the Texas Instruments *Widebus™* Family
- *EPIC™* (Enhanced-Performance Implanted CMOS) Submicron Process
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages

description

This 10-bit flip-flop is designed specifically for low-voltage 3.3-V V_{CC} operation.

The flip-flops of the SN74ALVC16820 are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the device provides true data at the Q outputs.

A buffered output-enable (\overline{OE}) input can be used to place the ten outputs in either a normal logic state (high or low level) or a high-impedance state.

In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

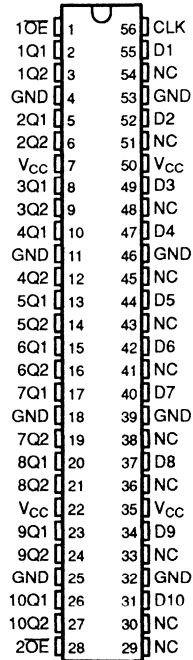
The output-enable (\overline{OE}) input does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVC16820 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16820 is characterized for operation from -40°C to 85°C .

DGG OR DL PACKAGE
(TOP VIEW)



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SN74ALVC16820
3.3-V 10-BIT FLIP-FLOP
WITH DUAL OUTPUTS

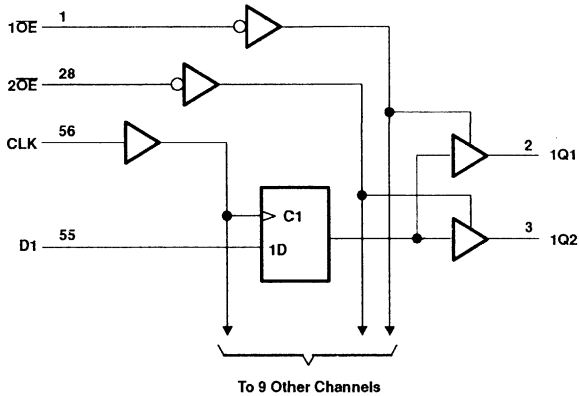
MARCH 1993

FUNCTION TABLE
 (each flip-flop)

INPUTS			OUTPUT
OE_n^\dagger	CLK	D	Q_n^\dagger
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

$^\dagger n = 1, 2$

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DGG package	0.7 W
DL package	1 W
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.

SN74ALVC16820
3.3-V 10-BIT FLIP-FLOP
WITH DUAL OUTPUTS

MARCH 1993

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V _{CC}	Supply voltage	2.7	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V		V
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		V
V _I	Input voltage	0	V _{CC}	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2.7 V		-12
		V _{CC} = 3 V		-24†
I _{OL}	Low-level output current	V _{CC} = 2.7 V		12
		V _{CC} = 3 V		24†
Δt/Δv	Input transition rise or fall rate	0	10	ns/V
T _A	Operating free-air temperature	-40	85	°C

NOTE 3: Unused or floating inputs must be held high or low.

† Current duty cycle ≤ 50%, f ≥ 1 kHz

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} ‡	MIN	TYP	MAX	UNIT
V _{IK}	I _I = -18 mA	2.7 V			-1.2	V
V _{OH}	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2			V
	I _{OH} = -12 mA	2.7 V	2.2			
		3 V	2.4			
	I _{OH} = -24 mA	3 V	2			
V _{OL}	I _{OL} = 100 μA	MIN to MAX			0.2	V
	I _{OL} = 12 mA	2.7 V			0.4	
	I _{OL} = 24 mA	3 V			0.55	
I _I	V _I = V _{CC} or GND	3.6 V			±5	μA
I _{OZ}	V _O = V _{CC} or GND	3.6 V			±10	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V			20	μA
ΔI _{CC}	V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC} or GND, One input at V _{CC} - 0.6 V,				500	μA
C _I	V _I = V _{CC} or GND	3.3 V			4	pF
C _O	V _O = V _{CC} or GND	3.3 V			6	pF

‡ For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		V _{CC} = 3.3 V ± 0.15 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	0	150	0	150	0	150	MHz
t _w	Pulse duration, CLK high or low							ns
t _{su}	Setup time, data before CLK↑	High or low	0.8	1				ns
t _h	Hold time, data after CLK↑	High or low	2	2				ns



SN74ALVC16820
3.3-V 10-BIT FLIP-FLOP
WITH DUAL OUTPUTS

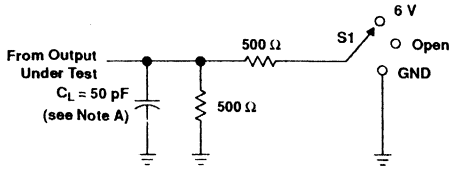
MARCH 1993

switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3 V \pm 0.15 V$		$V_{CC} = 3.3 V \pm 0.3 V$		$V_{CC} = 2.7 V$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			150		150		150		MHz
t_{PLH}	CLK	Q		4		4.5			ns
t_{PHL}				4		4.5			
t_{PZH}	OE	Q		5		5.7			ns
t_{PZL}				5		5.7			
t_{PHZ}	OE	Q		4.5		4.5			ns
t_{PLZ}				4.5		4.5			

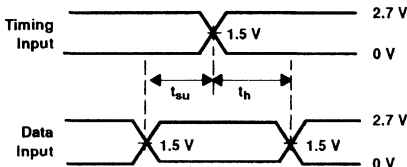
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

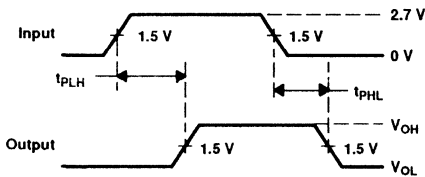


LOAD CIRCUIT FOR OUTPUTS

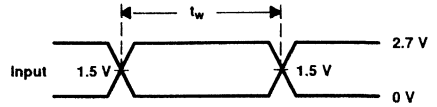
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



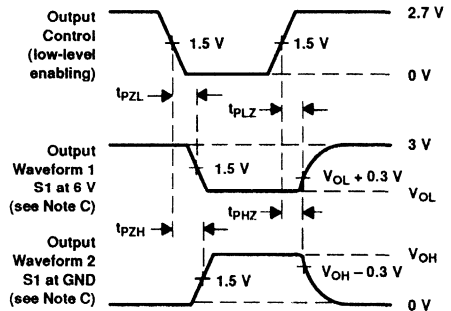
VOLTAGE WAVEFORMS
 SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
 PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
 PULSE DURATION



VOLTAGE WAVEFORMS
 ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

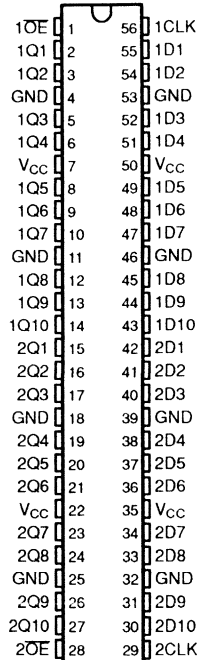
SN74ALVC16821

3.3-V 20-BIT BUS-INTERFACE FLIP-FLOP WITH 3-STATE OUTPUTS

MARCH 1993

- Member of the Texas Instruments *Widebus™* Family
- *EPIC™* (Enhanced-Performance Implanted CMOS) Submicron Process
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages

DGG OR DL PACKAGE
(TOP VIEW)



description

This 20-bit bus-interface flip-flop is designed specifically for low-voltage 3.3-V V_{CC} operation.

The SN74ALVC16821 can be used as two 10-bit flip-flops or one 20-bit flip-flop. The twenty flip-flops are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the device provides true data at the Q outputs.

A buffered output-enable (\overline{OE}) input can be used to place the ten outputs in either a normal logic state (high or low level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (\overline{OE}) input does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVC16821 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16821 is characterized for operation from -40°C to 85°C .

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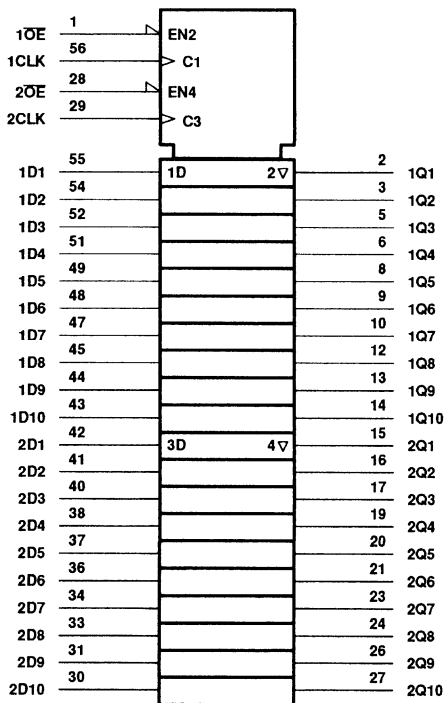
SN74ALVC16821
3.3-V 20-BIT BUS-INTERFACE FLIP-FLOP
WITH 3-STATE OUTPUTS

MARCH 1993

FUNCTION TABLE
 (each 10-bit stage)

INPUTS			OUTPUT
OE	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q ₀
H	X	X	Z

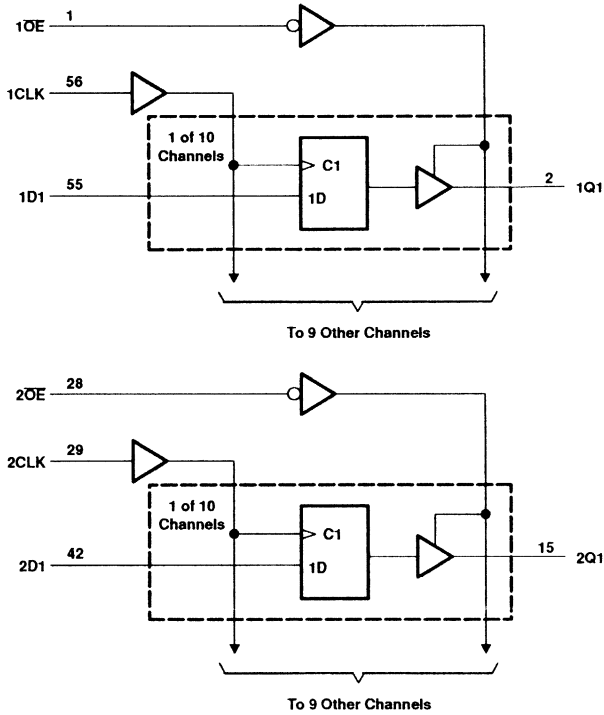
logic symbol†



PRODUCT PREVIEW

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DGG package	0.7 W
DL package	1 W
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.

SN74ALVC16821
3.3-V 20-BIT BUS-INTERFACE FLIP-FLOP
WITH 3-STATE OUTPUTS

MARCH 1993

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$		V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7\text{ V}$		-12
		$V_{CC} = 3\text{ V}$		-24†
I_{OL}	Low-level output current	$V_{CC} = 2.7\text{ V}$		12
		$V_{CC} = 3\text{ V}$		24†
$\Delta V/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	-40	85	°C

NOTE 3: Unused or floating inputs must be held high or low.

† Current duty cycle $\leq 50\%$, $f \geq 1\text{ kHz}$

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}^\ddagger	MIN	TYP	MAX	UNIT
V_{IK}	$I_I = -18\text{ mA}$	2.7 V			-1.2	V
V_{OH}	$I_{OH} = -100\ \mu\text{A}$	MIN to MAX	$V_{CC}-0.2$			V
	$I_{OH} = -12\text{ mA}$	2.7 V	2.2			
	$I_{OH} = -24\text{ mA}$	3 V	2.4			
V_{OL}	$I_{OL} = 100\ \mu\text{A}$	MIN to MAX			0.2	V
	$I_{OL} = 12\text{ mA}$	2.7 V			0.4	
	$I_{OL} = 24\text{ mA}$	3 V			0.55	
I_I	$V_I = V_{CC}$ or GND	3.6 V			± 5	μA
I_{OZ}	$V_O = V_{CC}$ or GND	3.6 V			± 10	μA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			20	μA
ΔI_{CC}	$V_{CC} = 3\text{ V to }3.6\text{ V}$, Other inputs at V_{CC} or GND One input at $V_{CC} - 0.6\text{ V}$,				500	μA
C_i	$V_I = V_{CC}$ or GND	3.3 V			4	pF
C_o	$V_O = V_{CC}$ or GND	3.3 V			6	pF

‡ For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		$V_{CC} = 3.3\text{ V} \pm 0.15\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	150	0	150	0	150	MHz
t_w	Pulse duration, CLK high or low							ns
t_{su}	Setup time, data before CLK↑	High or low		3				ns
t_h	Hold time, data after CLK↑	High or low		0				ns



SN74ALVC16821
3.3-V 20-BIT BUS-INTERFACE FLIP-FLOP
WITH 3-STATE OUTPUTS

MARCH 1993

switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

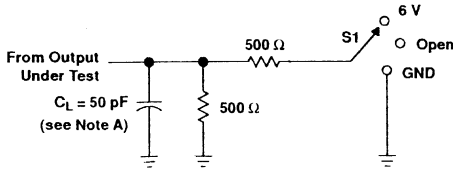
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3 V \pm 0.15 V$		$V_{CC} = 3.3 V \pm 0.3 V$		$V_{CC} = 2.7 V$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			150		150		150		MHz
t_{PLH}	CLK	Q		4		4.5			ns
t_{PHL}				4		4.5			
t_{PZH}	OE	Q		5		5.7		ns	
t_{PZL}				5		5.7			
t_{PHZ}	OE	Q		4.5		4.5		ns	
t_{PLZ}				4.5		4.5			

PRODUCT PREVIEW

SN74ALVC16821
3.3-V 20-BIT BUS-INTERFACE FLIP-FLOP
WITH 3-STATE OUTPUTS

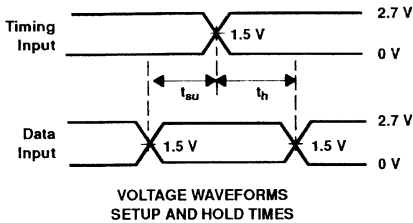
MARCH 1993

PARAMETER MEASUREMENT INFORMATION

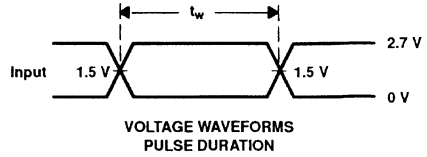


LOAD CIRCUIT FOR OUTPUTS

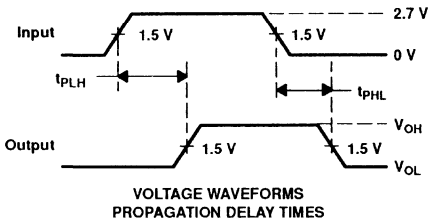
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



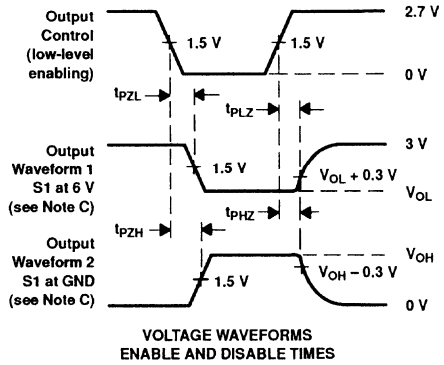
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW



SN74ALVC16823

18-BIT BUS-INTERFACE FLIP-FLOP WITH 3-STATE OUTPUTS

JANUARY 1993

- Member of the Texas Instruments *Widebus™* Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Designed to Facilitate Incident Wave Switching for Line Impedances of 50 Ω or Greater
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ$ C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ$ C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages

description

This 18-bit bus-interface flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74ALVC16823 features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

The SN74ALVC16823 can be used as two 9-bit flip-flops or one 18-bit flip-flop. With the clock-enable (CLKEN) input low, the D-type flip-flops enter data on the low-to-high transitions of the clock. Taking CLKEN high disables the clock buffer, thus latching the outputs. Taking the clear (CLR) input low causes the Q outputs to go low independently of the clock.

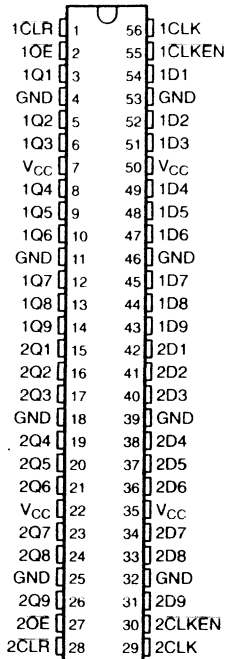
A buffered output-enable (OE) input can be used to place the nine outputs in either a normal logic state (high or low level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (OE) input does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74ALVC16823 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16823 is characterized for operation from -40° C to 85° C.

DGG OR DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

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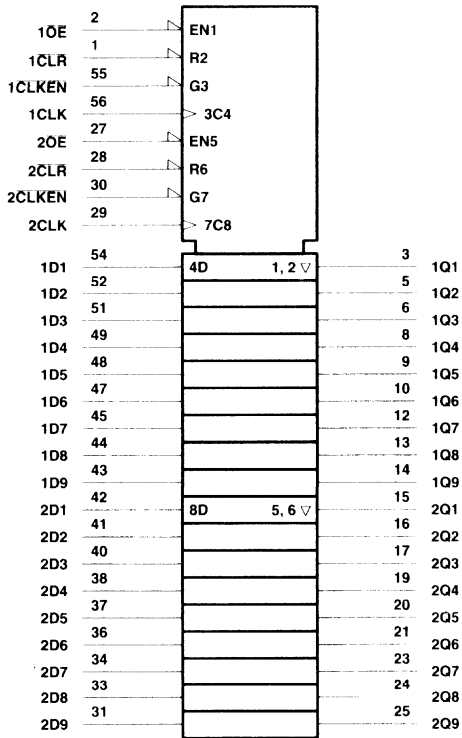
SN74ALVC16823
18-BIT BUS-INTERFACE FLIP-FLOP
WITH 3-STATE OUTPUTS

JANUARY 1993

FUNCTION TABLE
 (each 9-bit stage)

INPUTS					OUTPUT
OE	CLR	CLKEN	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	L	L	X	Q ₀
L	H	H	X	X	Q ₀
H	X	X	X	X	Z

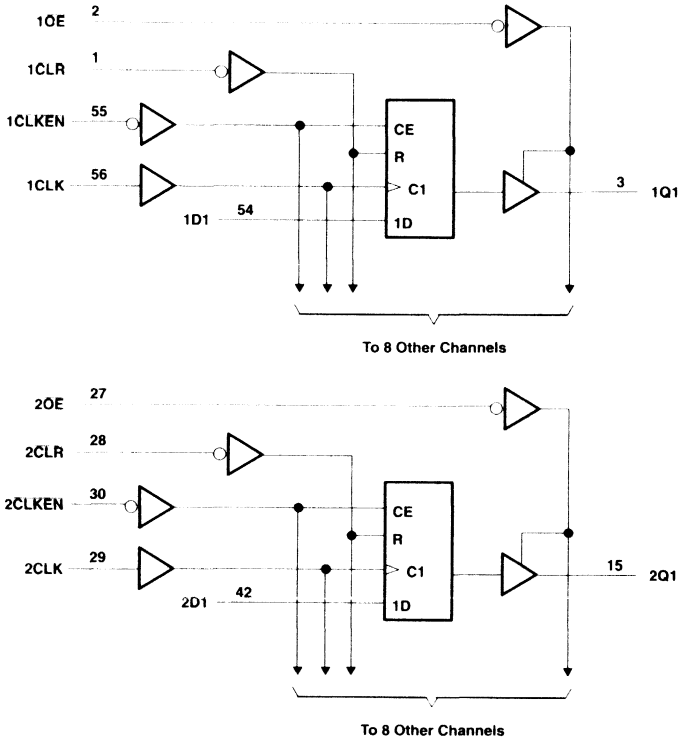
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DGG package	0.7 W
DL package	1 W
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.

SN74ALVC16823
18-BIT BUS-INTERFACE FLIP-FLOP
WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$		V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7\text{ V}$	-12	mA
		$V_{CC} = 3\text{ V}$	-24†	
I_{OL}	Low-level output current	$V_{CC} = 2.7\text{ V}$	12	mA
		$V_{CC} = 3\text{ V}$	24†	
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	-40	85	°C

NOTE 3: Unused or floating inputs must be held high or low.

† Current duty cycle $\leq 50\%$, $f > 1\text{ kHz}$

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}^\ddagger	MIN	TYP	MAX	UNIT
V_{IK}	$I_I = -18\text{ mA}$	2.7 V			-1.2	V
V_{OH}	$I_{OH} = -100\ \mu\text{A}$	MIN to MAX	$V_{CC} - 0.2$			V
	$I_{OH} = -12\text{ mA}$	2.7 V	2.2			
	$I_{OH} = -24\text{ mA}$	3 V	2.4			
V_{OL}	$I_{OL} = 100\ \mu\text{A}$	MIN to MAX			0.2	V
	$I_{OL} = 12\text{ mA}$	2.7 V			0.4	
	$I_{OL} = 24\text{ mA}$	3 V			0.55	
I_I	$V_I = V_{CC}$ or GND	3.6 V			± 5	μA
I_{OZ}	$V_O = V_{CC}$ or GND	3.6 V			± 10	μA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			20	μA
ΔI_{CC}	$V_{CC} = 3\text{ V to }3.6\text{ V}$, Other inputs at V_{CC} or GND				500	μA
C_i	$V_I = V_{CC}$ or GND	3.3 V		TBD		pF
C_o	$V_O = V_{CC}$ or GND	3.3 V		TBD		pF

‡ For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW



SN74ALVC16827
20-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS

JANUARY 1993

- Member of the Texas Instruments *Widebus™* Family
- *EPIC™* (Enhanced-Performance Implanted CMOS) Submicron Process
- Designed to Facilitate Incident Wave Switching for Line Impedances of 50 Ω or Greater
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages

description

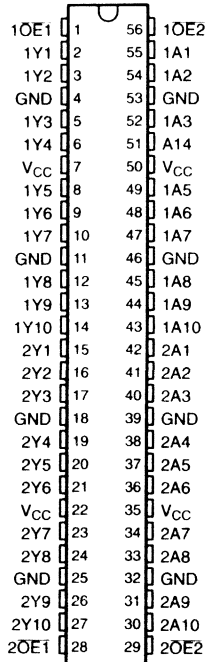
This 20-bit noninverting buffer/driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74ALVC16827 is composed of two 10-bit sections with separate output-enable signals. For either 10-bit buffer section, the two output-enable (1OE1 and 1OE2 or 2OE1 and 2OE2) inputs must both be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 10-bit buffer section are in the high-impedance state.

The SN74ALVC16827 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16827 is characterized for operation from -40°C to 85°C .

DGG OR DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

FUNCTION TABLE
(each 10-bit section)

INPUTS			OUTPUT
OE1	OE2	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

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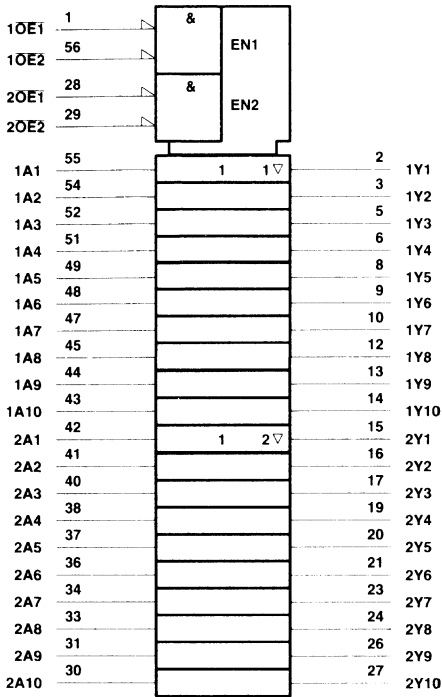
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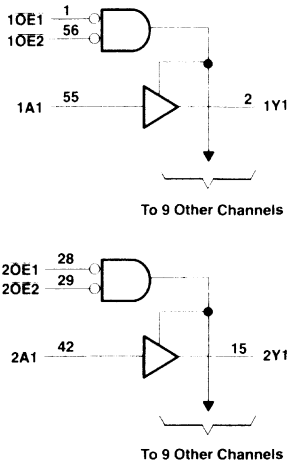
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SN74ALVC16827
20-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS
 JANUARY 1993

logic symbol†



logic diagram (positive logic)



PRODUCT PREVIEW

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DGG package	0.7 W
DL package	1 W
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7$ V		-12
		$V_{CC} = 3$ V		-24 [‡]
I_{OL}	Low-level output current	$V_{CC} = 2.7$ V		12
		$V_{CC} = 3$ V		24 [‡]
$\Delta V/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	-40	85	°C

NOTE 3: Unused or floating inputs must be held high or low.

[‡] Current duty cycle < 50%, $f > 1$ kHz

PRODUCT PREVIEW

SN74ALVC16827
20-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS

JANUARY 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} [†]	MIN	TYP	MAX	UNIT
V _{IK}	I _I = -18 mA	2.7 V			-1.2	V
V _{OH}	I _{OH} = -100 μA	MIN to MAX	V _{CC} - 0.2			V
	I _{OH} = -12 mA	2.7 V	2.2			
		3 V	2.4			
	I _{OH} = -24 mA	3 V	2			
V _{OL}	I _{OL} = 100 μA	MIN to MAX			0.2	V
	I _{OL} = 12 mA				0.4	
	I _{OL} = 24 mA	3 V			0.55	
I _I	V _I = V _{CC} or GND	3.6 V			+5	μA
I _{OZ}	V _O = V _{CC} or GND	3.6 V			±10	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V			20	μA
ΔI _{CC}	V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND				500	μA
C _i	V _I = V _{CC} or GND	3.3 V		TBD		pF
C _o	V _O = V _{CC} or GND	3.3 V		TBD		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW



SN74ALVC16828
20-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS

JANUARY 1993

- Member of the Texas Instruments *Widebus™* Family
- *EPIC™* (Enhanced-Performance Implanted CMOS) Submicron Process
- Designed to Facilitate Incident Wave Switching for Line Impedances of 50 Ω or Greater
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ$ C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ$ C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages

description

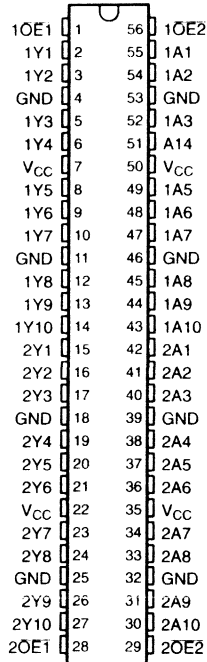
This 20-bit inverting buffer/driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74ALVC16828 is composed of two 10-bit sections with separate output-enable signals. For either 10-bit buffer section, the two output-enable (1OE1 and 1OE2 or 2OE1 and 2OE2) inputs must both be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 10-bit buffer section are in the high-impedance state.

The SN74ALVC16828 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16828 is characterized for operation from -40° C to 85° C.

DGG OR DL PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each 10-bit section)

INPUTS			OUTPUT	
OE1	OE2	A	Y	Y
L	L	L	H	H
L	L	H	L	L
H	X	X	Z	Z
X	H	X	Z	Z

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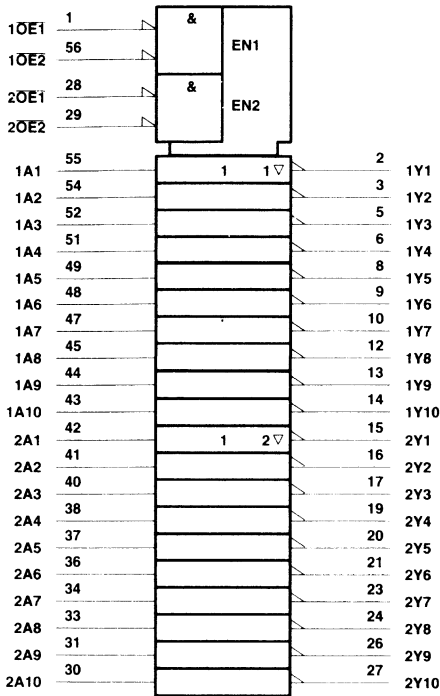
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PRODUCT PREVIEW

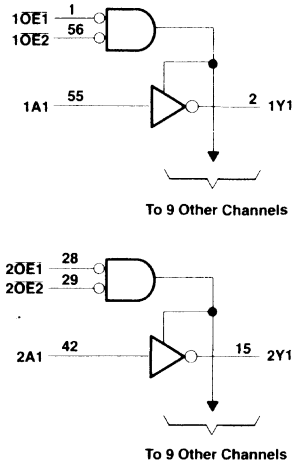
SN74ALVC16828
20-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS
 JANUARY 1993

PRODUCT PREVIEW

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DGG package	0.7 W
DL package	1 W
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7$ V		mA
		$V_{CC} = 3$ V		
I_{OL}	Low-level output current	$V_{CC} = 2.7$ V		mA
		$V_{CC} = 3$ V		
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	-40	85	°C

NOTE 3: Unused or floating inputs must be held high or low.

[‡] Current duty cycle < 50%. f > 1 kHz

PRODUCT PREVIEW

SN74ALVC16828
20-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS

JANUARY 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}^{\dagger}	MIN	TYP	MAX	UNIT
V_{IK}	$I_I = -18 \text{ mA}$	2.7 V			-1.2	V
V_{OH}	$I_{OH} = -100 \mu\text{A}$	MIN to MAX	$V_{CC} - 0.2$			V
	$I_{OH} = -12 \text{ mA}$	2.7 V	2.2			
		3 V	2.4			
	$I_{OH} = -24 \text{ mA}$	3 V	2			
V_{OL}	$I_{OL} = 100 \mu\text{A}$	MIN to MAX			0.2	V
	$I_{OL} = 12 \text{ mA}$	2.7 V			0.4	
	$I_{OL} = 24 \text{ mA}$	3 V			0.55	
I_I	$V_I = V_{CC}$ or GND	3.6 V			±5	μA
I_{OZ}	$V_O = V_{CC}$ or GND	3.6 V			±10	μA
I_{CC}	$V_I = V_{CC}$ or GND. $I_O = 0$	3.6 V			20	μA
ΔI_{CC}	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$. Other inputs at V_{CC} or GND				500	μA
C_i	$V_I = V_{CC}$ or GND	3.3 V		TBD		pF
C_o	$V_O = V_{CC}$ or GND	3.3 V		TBD		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

SN74ALVC16841

20-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS

JANUARY 1993

- Member of the Texas Instruments *Widebus™* Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Designed to Facilitate Incident Wave Switching for Line Impedances of 50 Ω or Greater
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages

description

This 20-bit bus-interface D-type latch is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74ALVC16841 features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The SN74ALVC16841 can be used as two 10-bit latches or one 20-bit latch. The twenty latches are transparent D-type latches. The device has noninverting data (D) inputs and provides true data at its outputs. While the latch-enable (1LE or 2LE) input is high, the Q outputs of the corresponding 10-bit latch follow the D inputs. When LE is taken low, the Q outputs are latched at the levels that were set up at the D inputs.

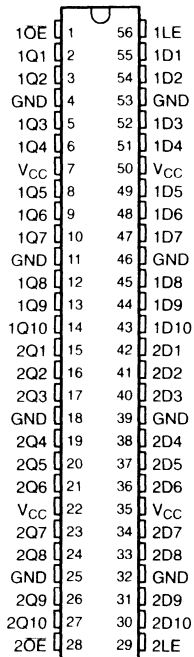
A buffered output-enable ($1OE$ or $2OE$) input can be used to place the outputs of the corresponding 10-bit latch in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly.

The output-enable (OE) input does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74ALVC16841 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16841 is characterized for operation from -40°C to 85°C .

DGG OR DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

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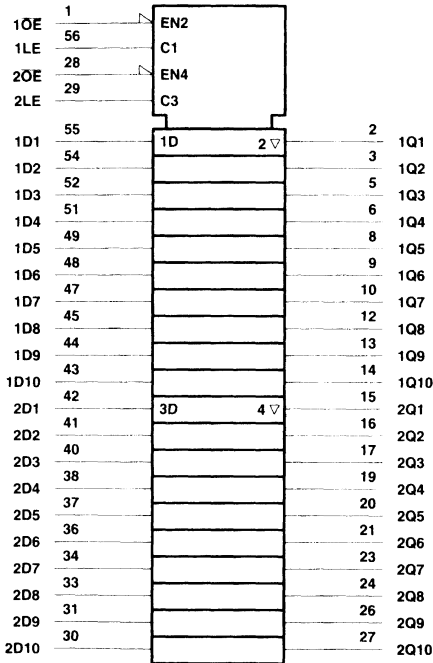
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SN74ALVC16841
20-BIT BUS-INTERFACE D-TYPE LATCH
WITH 3-STATE OUTPUTS
 JANUARY 1993

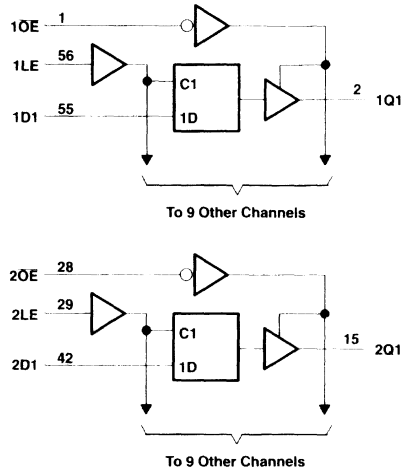
FUNCTION TABLE
 (each 10-bit latch)

INPUTS			OUTPUT
OE	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q ₀
H	X	X	Z

logic symbol†



logic diagram (positive logic)



PRODUCT PREVIEW

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN74ALVC16841

20-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS

JANUARY 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DGG package	0.7 W
DL package	1 W
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7$ V	-12	mA
		$V_{CC} = 3$ V	-24 [‡]	
I_{OL}	Low-level output current	$V_{CC} = 2.7$ V	12	mA
		$V_{CC} = 3$ V	24 [‡]	
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	-40	85	°C

NOTE 3: Unused or floating inputs must be held high or low.

[‡] Current duty cycle = 50%, $f > 1$ kHz

PRODUCT PREVIEW

SN74ALVC16841
20-BIT BUS-INTERFACE D-TYPE LATCH
WITH 3-STATE OUTPUTS

JANUARY 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} [†]	MIN	TYP	MAX	UNIT
V _{IK}	I _I = -18 mA	2.7 V			-1.2	V
V _{OH}	I _{OH} = -100 μA	MIN to MAX	V _{CC} - 0.2			V
	I _{OH} = -12 mA	2.7 V	2.2			
	I _{OH} = -24 mA	3 V	2.4			
V _{OL}	I _{OL} = 100 μA	MIN to MAX			0.2	V
	I _{OL} = 12 mA	2.7 V			0.4	
	I _{OL} = 24 mA	3 V			0.55	
I _I	V _I = V _{CC} or GND	3.6 V			±5	μA
I _{OZ}	V _O = V _{CC} or GND	3.6 V			±10	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V			20	μA
ΔI _{CC}	V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC} or GND, One input at V _{CC} - 0.6 V.				500	μA
C _I	V _I = V _{CC} or GND	3.3 V		TBD		pF
C _O	V _O = V _{CC} or GND	3.3 V		TBD		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

SN74ALVC16843

18-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS

JANUARY 1993

- Member of the Texas Instruments *Widebus™* Family
- *EPIC™* (Enhanced-Performance Implanted CMOS) Submicron Process
- Designed to Facilitate Incident Wave Switching for Line Impedances of 50 Ω or Greater
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages

description

This 18-bit bus-interface D-type latch is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74ALVC16843 features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The SN74ALVC16843 can be used as two 9-bit latches or one 18-bit latch. The eighteen latches are transparent D-type latches. The device has noninverting data (D) inputs and provides true data at its outputs.

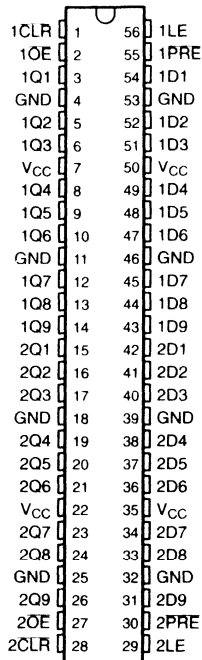
A buffered output-enable (OE) input can be used to place the nine outputs in either a normal logic state (high or low levels) or a high-impedance state. The outputs are also in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered down. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (OE) input does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74ALVC16843 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16843 is characterized for operation from -40°C to 85°C .

DGG OR DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

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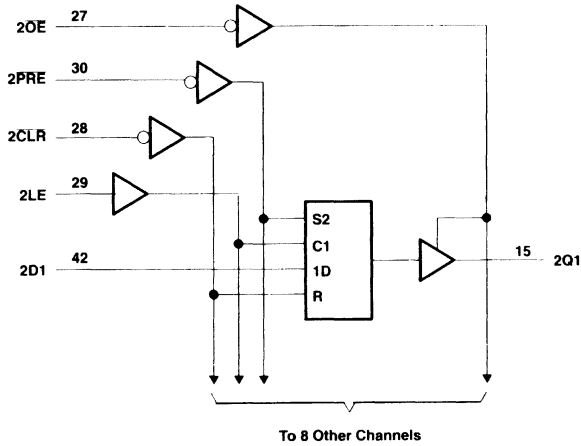
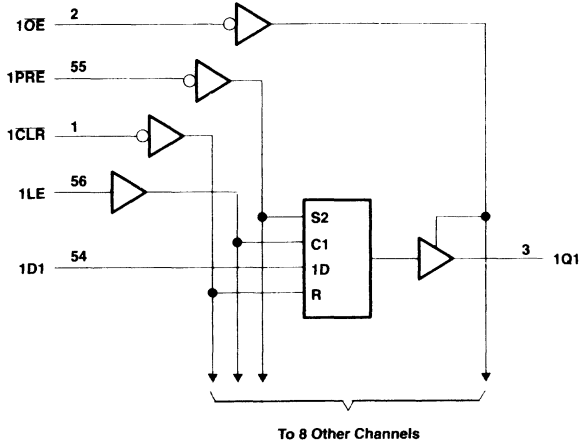
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SN74ALVC16843
18-BIT BUS-INTERFACE D-TYPE LATCH
WITH 3-STATE OUTPUTS
 JANUARY 1993

logic diagram (positive logic)



PRODUCT PREVIEW

SN74ALVC16843
18-BIT BUS-INTERFACE D-TYPE LATCH
WITH 3-STATE OUTPUTS

JANUARY 1993

FUNCTION TABLE
(each 9-bit latch)

INPUTS					OUTPUT
PRE	CLR	OE	LE	D	Q
L	X	L	X	X	H
H	L	L	X	X	L
H	H	L	H	L	L
H	H	L	H	H	H
H	H	L	L	X	Q ₀
X	X	H	X	X	Z

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}	-0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	-0.5 V to 4.6 V
Output voltage range, V _O (see Notes 1 and 2)	-0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	-50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±50 mA
Continuous current through V _{CC} or GND pins	±100 mA
Maximum power dissipation at T _A = 55°C (in still air): DGG package	0.7 W
DL package	1 W
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V _{CC}	Supply voltage	2.7	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V		V
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		V
V _I	Input voltage	0	V _{CC}	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2.7 V		-12
		V _{CC} = 3 V		-24 [‡]
I _{OL}	Low-level output current	V _{CC} = 2.7 V		12
		V _{CC} = 3 V		24 [‡]
ΔV/Δv	Input transition rise or fall rate	0	10	ns/V
T _A	Operating free-air temperature	-40	85	°C

NOTE 3: Unused or floating inputs must be held high or low.

[‡] Current duty cycle ≤ 50%, f ≥ 1 kHz

PRODUCT PREVIEW

SN74ALVC16843
18-BIT BUS-INTERFACE D-TYPE LATCH
WITH 3-STATE OUTPUTS

JANUARY 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}^{\dagger}	MIN	TYP	MAX	UNIT
V_{IK}	$I_I = -18 \text{ mA}$	2.7 V			-1.2	V
V_{OH}	$I_{OH} = -100 \mu\text{A}$	MIN to MAX	$V_{CC} - 0.2$			V
	$I_{OH} = -12 \text{ mA}$	2.7 V	2.2			
		3 V	2.4			
V_{OL}	$I_{OH} = -24 \text{ mA}$	3 V	2			V
	$I_{OL} = 100 \mu\text{A}$	MIN to MAX			0.2	
	$I_{OL} = 12 \text{ mA}$	2.7 V			0.4	
	$I_{OL} = 24 \text{ mA}$	3 V			0.55	
I_I	$V_I = V_{CC}$ or GND	3.6 V			± 5	μA
I_{OZ}	$V_O = V_{CC}$ or GND	3.6 V			± 10	μA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			20	μA
ΔI_{CC}	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$, Other inputs at V_{CC} or GND	One input at $V_{CC} - 0.6 \text{ V}$.			500	μA
C_i	$V_I = V_{CC}$ or GND	3.3 V		TBD		pF
C_o	$V_O = V_{CC}$ or GND	3.3 V		TBD		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

SN74ALVC16952 16-BIT REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

JANUARY 1993

- Member of the Texas Instruments *Widebus™* Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Designed to Facilitate Incident Wave Switching for Line Impedances of 50 Ω or Greater
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages

description

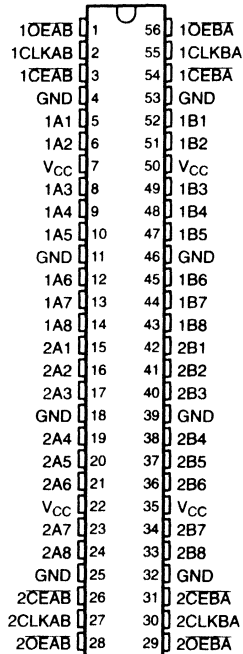
This 16-bit registered transceiver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74ALVC16952 contains two sets of D-type flip-flops for temporary storage of data flowing in either direction. It can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock (CLKAB or CLKBA) input provided that the clock-enable (CEAB or CEBA) input is low. Taking the output-enable (\overline{OEAB} or \overline{OEBA}) input low accesses the data on either port.

The SN74ALVC16952 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16952 is characterized for operation from -40°C to 85°C .

DGG OR DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

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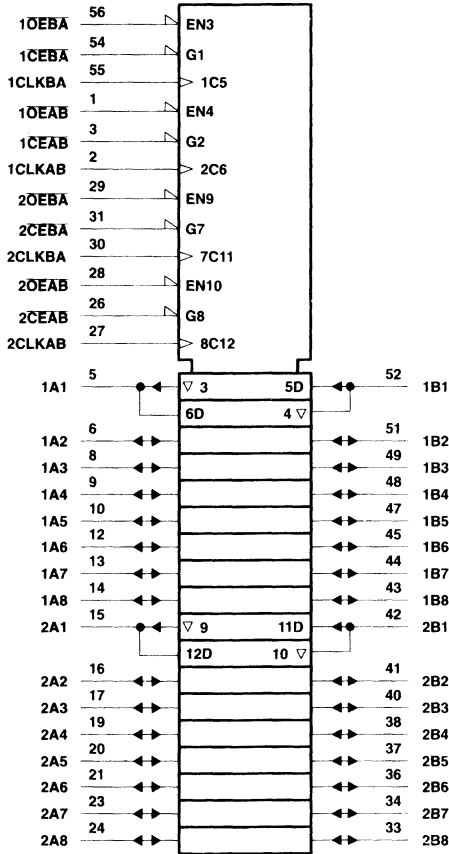
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SN74ALVC16952
16-BIT REGISTERED TRANSCEIVER
WITH 3-STATE OUTPUTS
 JANUARY 1993

logic symbol†

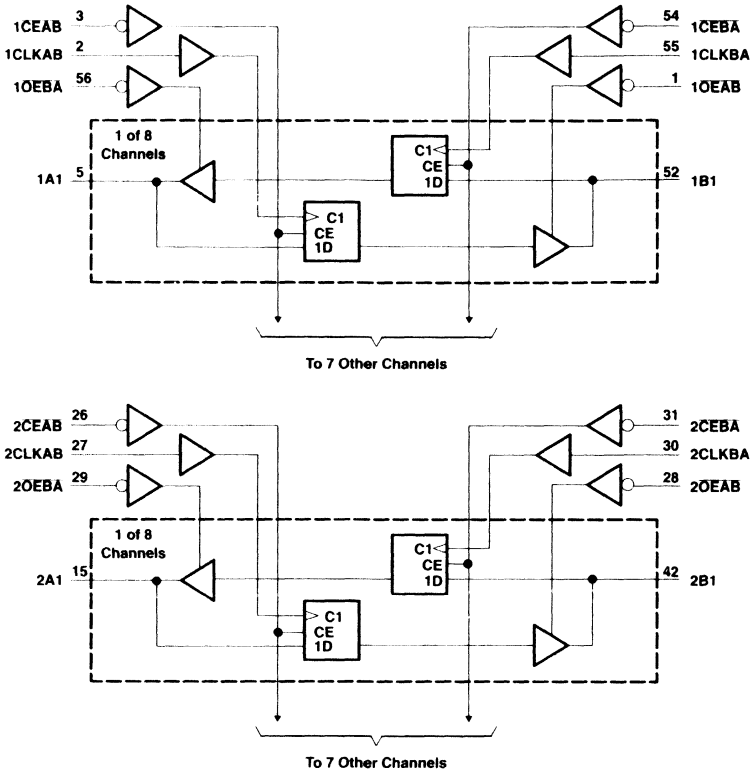


PRODUCT PREVIEW

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN74ALVC16952
16-BIT REGISTERED TRANSCEIVER
WITH 3-STATE OUTPUTS
 JANUARY 1993

logic diagram (positive logic)



FUNCTION TABLE†

INPUTS				OUTPUT
CEAB	CLKAB	OEAB	A	B
H	X	L	X	B ₀ †
X	L	L	X	B ₀ ‡
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	Z

† A-to-B data flow is shown; B-to-A data flow is similar but uses \overline{CEBA} , \overline{CLKBA} , and \overline{OEBA} .

‡ Level of B before the indicated steady-state input conditions were established.

PRODUCT PREVIEW

SN74ALVC16952
16-BIT REGISTERED TRANSCEIVER
WITH 3-STATE OUTPUTS

JANUARY 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1)	-0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DGG package	0.7 W
DL package	1 W
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed
 2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7$ V		-12
		$V_{CC} = 3$ V		-24 [‡]
I_{OL}	Low-level output current	$V_{CC} = 2.7$ V		12
		$V_{CC} = 3$ V		24 [‡]
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	-40	85	°C

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.

[‡] Current duty cycle ≤ 50%, $f \geq 1$ kHz

PRODUCT PREVIEW



SN74ALVC16952
16-BIT REGISTERED TRANSCEIVER
WITH 3-STATE OUTPUTS

JANUARY 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}^{\dagger}	MIN	TYP	MAX	UNIT
V_{IK}		$I_I = -18 \text{ mA}$	2.7 V			-1.2	V
V_{OH}		$I_{OH} = -100 \mu\text{A}$	MIN to MAX	$V_{CC} - 0.2$			V
		$I_{OH} = -12 \text{ mA}$	2.7 V	2.2			
		$I_{OH} = -24 \text{ mA}$	3 V	2.4			
V_{OL}		$I_{OL} = 100 \mu\text{A}$	MIN to MAX			0.2	V
		$I_{OL} = 12 \text{ mA}$	2.7 V			0.4	
		$I_{OL} = 24 \text{ mA}$	3 V			0.55	
I_I		$V_I = V_{CC}$ or GND	3.6 V			+5	μA
I_{OZ}^{\ddagger}		$V_O = V_{CC}$ or GND	3.6 V			: 10	μA
I_{CC}		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			20	μA
ΔI_{CC}		$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$, Other inputs at V_{CC} or GND				500	μA
C_i	Control inputs	$V_I = V_{CC}$ or GND	3.3 V		TBD		pF
C_{io}	A or B ports	$V_O = V_{CC}$ or GND	3.3 V		TBD		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

[§] For I/O ports, the parameter I_{OZ} includes the input leakage current.

PRODUCT PREVIEW

74ALVC164245

16-BIT TRANSCEIVER, 3.3V TO 5V LEVEL SHIFTER WITH 3-STATE OUTPUTS

SEPTEMBER 1993

- Members of the Texas Instruments *Widebus™* Family
- *EPIC™* (Enhanced-Performance Implanted CMOS) Sub-Micron Process
- Packaged in Plastic 300-mil Shrink Small-Outline Packages (DL) and 380-mil Fine-Pitch Ceramic Flat Packages (WD) Using 25-mil Center-to-Center Spacings
- Inputs Are TTL-Voltage Compatible
- Noninverting Outputs
- Two 16-Bit, Back-to-Back Registers Store Data Flowing in Both Directions
- Flow-Through Architecture Optimizes PCB Layout
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- 500-mA Typical Latch-Up Immunity at 125°C

description

The 'ALVC164245 is a 16-bit transceiver that contains two separate supply rails, B port has V_{CC1} which is set at 5V and the A port has V_{CC2} which is set to operate at 3.3 V. This allows for translation from a 3.3V to a 5 V environment, and visa-versa.

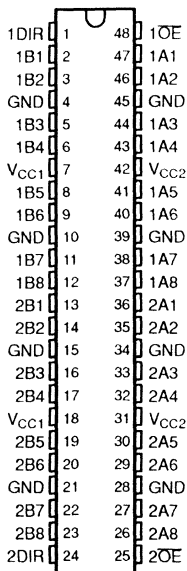
The 'ALVC164245 is a 16-bit (dual-octal) noninverting 3-state transceiver designed for synchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so that the buses are effectively isolated.

The 74ALVC164245 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 74ALVC164245 is characterized for operation from -40°C to 85°C .

DGG OR DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
\overline{OE}	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

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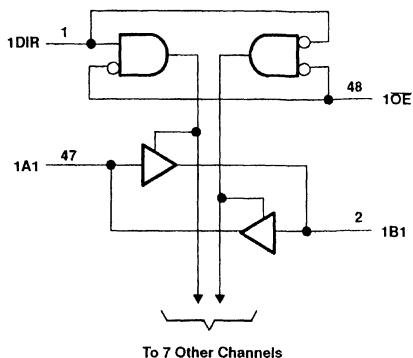
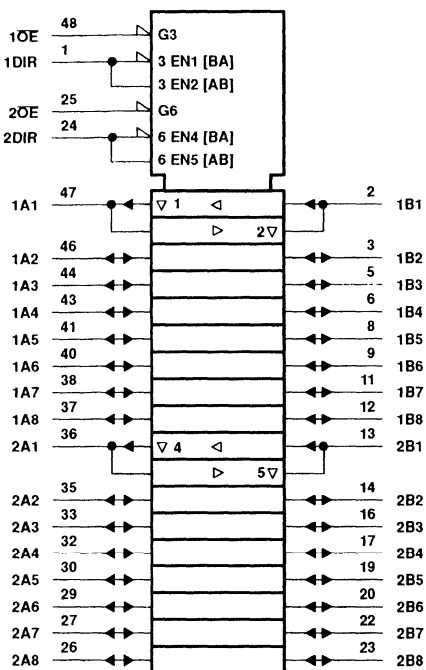


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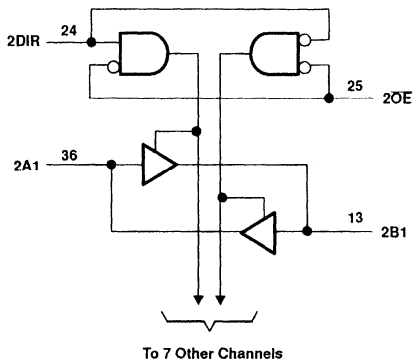
74ALVC164245
16-BIT TRANSCEIVER, 3.3V TO 5V LEVEL SHIFTER
WITH 3-STATE OUTPUTS

SEPTEMBER 1993

logic diagram (positive logic)



To 7 Other Channels



To 7 Other Channels

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

74ALVC164245
16-BIT TRANSCEIVER, 3.3V TO 5V LEVEL SHIFTER
WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range for V_{CC1} at 5V (unless otherwise noted)[†]

Supply voltage range, V_{CC1}	-0.5 V to 6 V
Input voltage range, V_I (see Note 1)	-0.5 V to $V_{CC1} + 0.5$ V
Output voltage range, V_O (see Note 1)	-0.5 V to $V_{CC1} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC1}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC1}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC1})	± 50 mA
Continuous current through V_{CC1} or GND pins	± 100 mA

absolute maximum ratings over operating free-air temperature range for V_{CC2} at 3.3V (unless otherwise noted)[†]

Supply voltage range, V_{CC2}	-0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1)	-0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Note 1), (see Note 2)	-0.5 V to $V_{CC2} + 0.5$ V
Output voltage range, V_O (see Note 1), (see Note 2)	-0.5 V to $V_{CC2} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC2}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC2})	± 50 mA
Continuous current through V_{CC2} or GND pins	± 100 mA

absolute maximum ratings over operating free-air temperature range for V_{CC1} at 5V or for V_{CC2} at 3.3V (unless otherwise noted)[†]

Maximum power package dissipation at $T_A = 55^\circ\text{C}$ (in still air): DGG	0.6 W
..... DL	0.85 W
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

NOTE 2: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

NOTE 3: This value is limited to 4.6 V maximum.

recommended operating conditions for V_{CC1} at 5V (see Note 2)

		74ALVC164245			UNIT
		MIN	NOM	MAX	
V_{CC1}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC1}	V
V_O	Output voltage	0		V_{CC1}	V
I_{OH}	High-level output current			-24	mA
I_{OL}	Low-level output current			24	mA
$\Delta V/\Delta V$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	-40		85	°C

NOTE 4: Unused or floating pins (input or I/O) must be held high or low.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



74ALVC164245
16-BIT TRANSCEIVER, 3.3V TO 5V LEVEL SHIFTER
WITH 3-STATE OUTPUTS

SEPTEMBER 1993

recommended operating conditions for V_{CC2} at 3.3V (see Note 3)

			MIN	NOM	MAX	UNIT
V_{CC2}	Supply voltage		2.7		3.6	V
V_{IH}	High-level input voltage	$V_{CC2} = 2.7\text{ V to }3.6\text{ V}$		2		V
V_{IL}	Low-level input voltage	$V_{CC2} = 2.7\text{ V to }3.6\text{ V}$			0.8	V
V_I	Input voltage		0		V_{CC2}	V
V_O	Output voltage		0		V_{CC2}	V
I_{OH}	High-level output current	$V_{CCB} = 2.7\text{ V}$				mA
		$V_{CCB} = 3\text{ V}$				
I_{OL}	Low-level output current	$V_{CCB} = 2.7\text{ V}$				mA
		$V_{CCB} = 3\text{ V}$				
$\Delta t/\Delta V$	Input transition rise or fall rate		0		10	ns/V
T_A	Operating free air temperature		-40		85	$^{\circ}\text{C}$

NOTE 5: Unused or floating pins (input or I/O) must be held high or low.
 § Current duty cycle $\leq 50\%$, $t \geq 1\text{ kHz}$

electrical characteristics over recommended operating free-air temperature range for V_{CC1} at 5V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	74ALVC164245		UNIT
			MIN	MAX	
V_{OH}	$I_{OH} = -200\ \mu\text{A}$	4.5 V	4.3		V
		5.5 V	5.3		
	$I_{OH} = -24\ \text{mA}$	4.5 V	3.7		
		5.5 V	4.7		
V_{OL}	$I_{OL} = 200\ \mu\text{A}$	4.5 V		0.2	V
		5.5 V		0.2	
	$I_{OL} = 24\ \text{mA}$	4.5 V		0.55	
		5.5 V		0.55	
I_I	Control inputs $V_I = V_{CC}$ or GND	5.5 V			μA
I_{OZ}^{\dagger}	A or B ports $V_O = V_{CC}$ or GND	5.5 V			μA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			μA
ΔI_{CC}^{\S}	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			mA
C_i	Control inputs $V_I = V_{CC}$ or GND	5 V			pF
C_{io}	A or B ports $V_O = V_{CC}$ or GND	5 V			pF

\dagger For I/O ports, the parameter I_{OZ} includes the input leakage current.
 \S This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC} .
 \ddagger For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.
 \ddagger For I/O ports, the parameter I_{OZ} includes the input leakage current.

Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

\ddagger For I/O ports, the parameter I_{OZ} includes the input leakage current.
 \S This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC} .
 \ddagger For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.
 \ddagger For I/O ports, the parameter I_{OZ} includes the input leakage current.

PRODUCT PREVIEW

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74ALVC164245
16-BIT TRANSCEIVER, 3.3V TO 5V LEVEL SHIFTER
WITH 3-STATE OUTPUTS

SEPTEMBER 1993

electrical characteristics over recommended operating free-air temperature range for V_{CC2} at 3.3V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = -40 \text{ TO } 85^\circ\text{C}$			UNIT
			MIN	TYP	MAX	
V_{IK}	$I_I = -18 \text{ mA}$	2.7 V			-1.2	V
V_{OH}	$I_{OH} = -100 \mu\text{A}$	V_{CC}^\dagger	$V_{CC} - 0.2$			V
	$I_{OH} = -12 \text{ mA}$	2.7 V	2.2			
	$I_{OH} = -12 \text{ mA}$	3 V	2.4			
	$I_{OH} = -24 \text{ mA}$	3 V	2			
V_{OL}	$I_{OL} = 100 \mu\text{A}$	V_{CC}^\dagger	0.2			V
	$I_{OL} = 12 \text{ mA}$	2.7 V	0.4			
	$I_{OL} = 24 \text{ mA}$	3 V	0.55			
I_I	$V_I = V_{CC}$ or GND	3.6 V				μA
I_{OZ}	$V_O = V_{CC}$ or GND	3.6 V				μA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V				μA
ΔI_{CC}	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$, one input at $V_{CC} - 0.6 \text{ V}$, other inputs at V_{CC} or GND					μA
C_i	Control inputs $V_I = V_{CC}$ or GND	3.3 V	TBD			pF
C_{iO}	A or B ports $V_O = V_{CC}$ or GND	3.3 V	TBD			pF

$^\dagger V_{CC} = \text{Min to Max}$

‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

switching characteristics over recommended operating free-air temperature range, $V_{CC1} = 5 \text{ V} \pm 0.5 \text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	74ALVC164245		UNIT
			MIN	MAX	
t_{max}					MHz
t_{pd}	A or B	B or A			ns
t_{en}	OEBA or OEAB	A or B			ns
t_{dis}					

operating characteristics, $V_{CC2} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	$C_L = 50 \text{ pF}$, $f = 1 \text{ MHz}$		pF
		Outputs disabled			

switching characteristics over recommended operating free-air temperature range, for V_{CC2} at 3.3V, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$			$V_{CC} = 2.7 \text{ V}$	UNIT
			MIN	TYP	MAX	MAX	
t_{pd}	A or B	B or A				ns	
t_{en}	OE	A or B				ns	
t_{disS}							

operating characteristics, $V_{CC2} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	$C_L = 50 \text{ pF}$, $f = 10 \text{ MHz}$		pF
		Outputs disabled			

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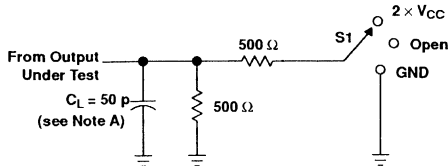


74ALVC164245
16-BIT TRANSCEIVER, 3.3V TO 5V LEVEL SHIFTER
WITH 3-STATE OUTPUTS

SEPTEMBER 1993

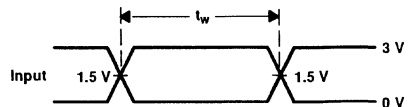
PARAMETER MEASUREMENT INFORMATION

$V_{CC1} = 5\text{ V}$

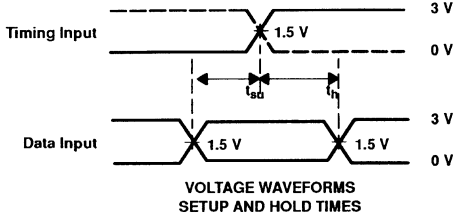


LOAD CIRCUIT FOR OUTPUTS

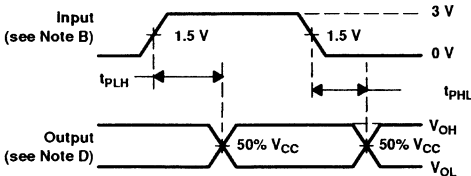
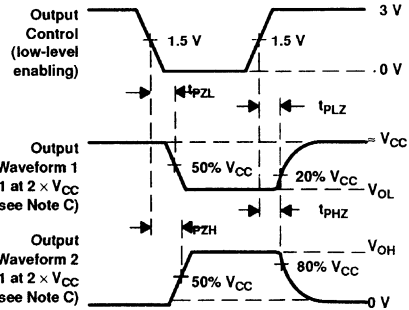
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



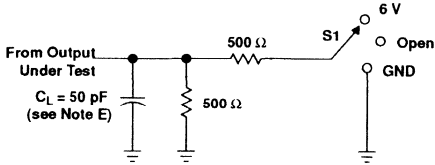
- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_o = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one transition per measurement.

PRODUCT PREVIEW



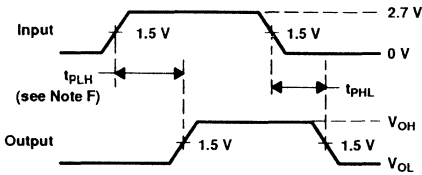
PARAMETER MEASUREMENT INFORMATION, CONTINUED

$V_{CC2} = 3.3V$

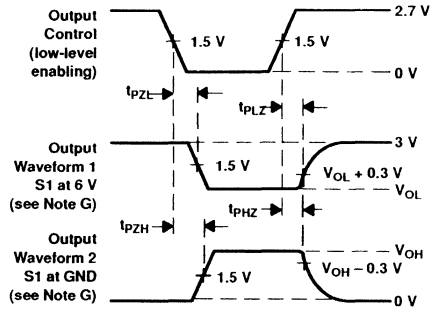


LOAD CIRCUIT FOR OUTPUTS

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES**

NOTES: E. C_L includes probe and jig capacitance.

F. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_o = 50 \Omega$, $t_r \leq 3$ ns, $t_f \leq 3$ ns. For testing pulse duration: $t_w = t_f = 1$ to 3 ns. Pulse polarity can be either high-to-low-to-high or low-to-high-to-low.

G. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

H. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW



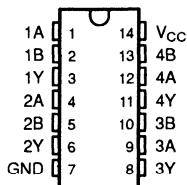
General Information	1
LVT Octals and Widebus™	2
LVC MSI, Octals and Widebus™	3
ALVC Widebus™	4
LV MSI and Octals	5
GTL Widebus™	6
CBT Bus Switches and 5-V/3-V Volt. Translators	7
Application Notes	8
LVT Characterization Information	9
Mechanical Data	10

SN74LV00 QUADRUPLE 2-INPUT POSITIVE-NAND GATE

FEBRUARY 1983 – REVISED JUNE 1983

- **Space-Saving Package Option:
Shrink Small-Outline Package (DB)
Features EIAJ 0.65-mm Lead Pitch**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 2-μm Process**
- **Typical V_{OLP} (Output Ground Bounce)
< 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **Typical V_{OHV} (Output V_{OH} Undershoot)
> 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline and Thin Shrink Small-Outline Packages**

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This quadruple 2-input positive-NAND gate is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV00 performs the Boolean functions $Y = \overline{A} \cdot \overline{B}$ or $Y = \overline{A + B}$ in positive logic.

The SN74LV00 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV00 is characterized for operation from -40°C to 85°C .

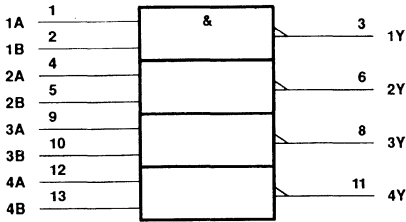
FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

SN74LV00 QUADRUPLE 2-INPUT POSITIVE-NAND GATE

FEBRUARY 1993 – REVISED JUNE 1993

logic symbol†



logic diagram, each gate (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND pins	± 50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air):		
D package	0.7 W
DB package	0.4 W
PW package	0.4 W
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.
2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.3	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		2	V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			-6	mA
I_{OL}	Low-level output current			6	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		100	ns/V
T_A	Operating free-air temperature	-40		85	$^\circ\text{C}$

NOTE 3: Unused or floating inputs must be held high or low.

SN74LV00 QUADRUPLE 2-INPUT POSITIVE-NAND GATE

FEBRUARY 1993 – REVISED JUNE 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} [†]	MIN	TYP	MAX	UNIT
V _{OH}	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2			V
	I _{OH} = -6 mA	3 V	2.4			
V _{OL}	I _{OL} = 100 μA	MIN to MAX	0.2			V
	I _{OL} = 6 mA	3 V	0.4			
I _I	V _I = V _{CC} or GND	3.6 V	±1			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V	20			μA
ΔI _{CC}	V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND		500			μA
C _I	V _I = V _{CC} or GND	3.3 V	2.5			pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

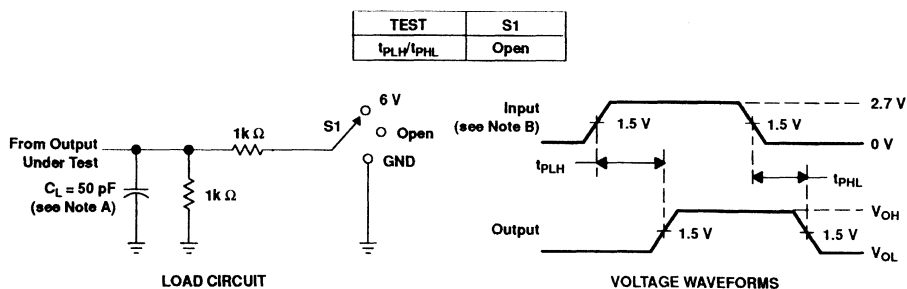
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V	UNIT
			MIN	TYP	MAX	MAX	
t _{pd}	A	Y	9	18	23	ns	

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance per gate	C _L = 50 pF, f = 10 MHz	23	pF

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
 C. The outputs are measured one at a time with one transition per measurement.

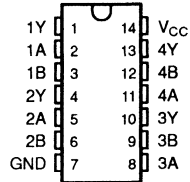
Figure 1. Load Circuit and Voltage Waveforms

SN74LV02 QUADRUPLE 2-INPUT POSITIVE-NOR GATE

FEBRUARY 1993 – REVISED JUNE 1993

- **Space-Saving Package Option: Shrink Small-Outline Package (DB) Features EIAJ 0.65-mm Lead Pitch**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 2- μ m Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline and Thin Shrink Small-Outline Packages**

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This quadruple 2-input positive-NOR gate is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV02 performs the Boolean functions $Y = \overline{A + B}$ or $Y = \overline{A} \cdot \overline{B}$ in positive logic.

The SN74LV02 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV02 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

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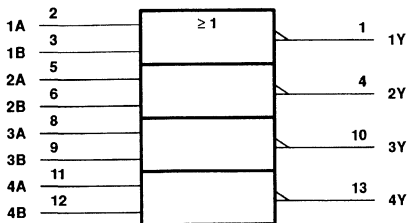


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SN74LV02 QUADRUPLE 2-INPUT POSITIVE-NOR GATE

FEBRUARY 1993 – REVISED JUNE 1993

logic symbol†



logic diagram, each gate (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND pins	± 50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air):		
D package	0.7 W
DB package	0.4 W
PW package	0.4 W
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.3	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		2	V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			-6	mA
I_{OL}	Low-level output current			6	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	100		ns/V
T_A	Operating free-air temperature	-40		85	$^\circ\text{C}$

NOTE 3: Unused or floating inputs must be held high or low.

SN74LV02 QUADRUPLE 2-INPUT POSITIVE-NOR GATE

FEBRUARY 1993 – REVISED JUNE 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}^\dagger	MIN	TYP	MAX	UNIT
V_{OH}	$I_{OH} = -100 \mu A$	MIN to MAX	$V_{CC} - 0.2$			V
	$I_{OH} = -6 \text{ mA}$	3 V	2.4			
V_{OL}	$I_{OL} = 100 \mu A$	MIN to MAX	0.2			V
	$I_{OL} = 6 \text{ mA}$	3 V	0.4			
I_I	$V_I = V_{CC}$ or GND	3.6 V	± 1			μA
I_{CC}	$V_I = V_{CC}$ or GND, $I_Q = 0$	3.6 V	20			μA
ΔI_{CC}	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$, Other inputs at V_{CC} or GND	One input at $V_{CC} - 0.6 \text{ V}$,	500			μA
C_I	$V_I = V_{CC}$ or GND	3.3 V	2.5			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

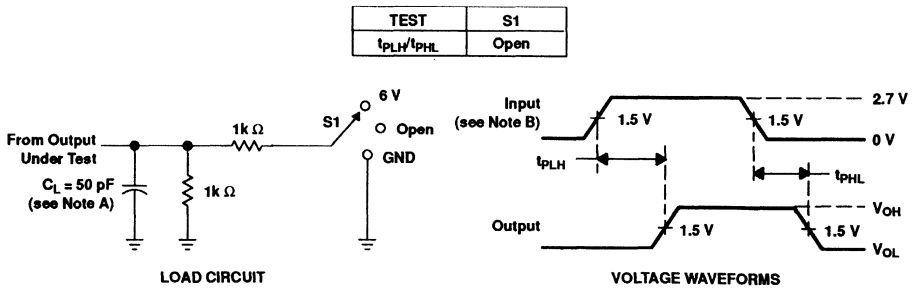
switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$			$V_{CC} = 2.7 \text{ V}$	UNIT
			MIN	TYP	MAX	MAX	
t_{pd}	A	Y	9	16	20	ns	

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ C$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	16	pF

PARAMETER MEASUREMENT INFORMATION

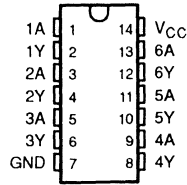


- NOTES:
- C_I includes probe and jig capacitance.
 - All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Space-Saving Package Option:**
Shrink Small-Outline Package (DB)
Features EIAJ 0.65-mm Lead Pitch
- **EPIC™ (Enhanced-Performance Implanted CMOS) 2-μm Process**
- **Typical V_{OLP} (Output Ground Bounce)**
< 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- **Typical V_{OHV} (Output V_{OH} Undershoot)**
> 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (D) and Thin Shrink Small-Outline (PW) Packages**

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This hex inverter is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV04 contains six independent inverters. The device performs the Boolean function $Y = \bar{A}$.

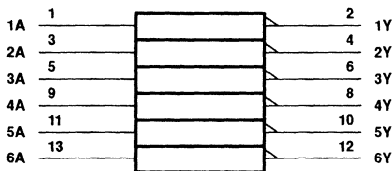
The SN74LV04 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV04 is characterized for operation from -40°C to 85°C .

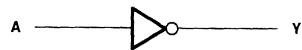
FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

logic symbol†



logic diagram, each inverter (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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 **TEXAS
INSTRUMENTS**

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SN74LV04 HEX INVERTER

MAY 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND pins	± 50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air):	
D package	0.7 W
DB package	0.4 W
PW package	0.4 W
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.3	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		2	V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			-6	mA
I_{OL}	Low-level output current			6	mA
$\Delta V/\Delta v$	Input transition rise or fall rate	0		100	ns/V
T_A	Operating free-air temperature	-40		85	°C

NOTE 3: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = -40^\circ\text{C}$ to 85°C			UNIT
			MIN	TYP	MAX	
V_{OH}	$I_{OH} = -100$ μA	MIN to MAX‡	$V_{CC} - 0.2$			V
	$I_{OH} = -6$ mA	3 V	2.4			
V_{OL}	$I_{OL} = 100$ μA	MIN to MAX†	0.2			V
	$I_{OL} = 6$ mA	3 V	0.4			
I_I	$V_I = V_{CC}$ or GND	3.6 V	± 1			μA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V	20			μA
ΔI_{CC}	$V_{CC} = 3$ V to 3.6 V, Other inputs at V_{CC} or GND	One input at $V_{CC} - 0.6$ V,	500			μA
C_i	$V_I = V_{CC}$ or GND	3.3 V	2.5			pF

‡ For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.



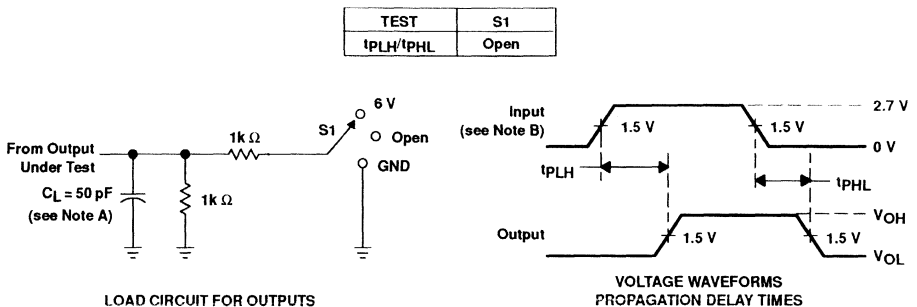
switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CC} = 2.7 \text{ V}$	UNIT
			MIN	TYP	MAX	
t_{pd}	A	Y	7	15	19	ns

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	$C_L = 50 \text{ pF}$, $f = 10 \text{ MHz}$	18	pF

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 C. The outputs are measured one at a time with one transition per measurement.

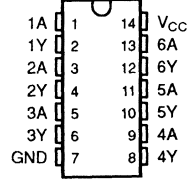
Figure 1. Load Circuit and Voltage Waveforms

SN74LVU04 HEX INVERTER

FEBRUARY 1993 – REVISED JUNE 1993

- **Space-Saving Package Option:**
Shrink Small-Outline Package (DB)
Features EIAJ 0.65-mm Lead Pitch
- **EPIC™ (Enhanced-Performance Implanted CMOS) 2- μ m Process**
- **Typical V_{OLP} (Output Ground Bounce)**
< 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- **Typical V_{OHV} (Output V_{OH} Undershoot)**
> 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline and Thin Shrink Small-Outline Packages**

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This hex inverter is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVU04 contains six independent inverters with unbuffered outputs. The device performs the Boolean function $Y = \bar{A}$.

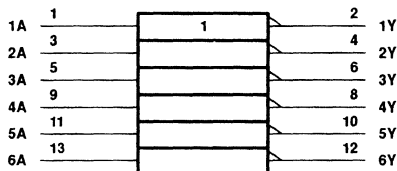
The SN74LVU04 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LVU04 is characterized for operation from -40°C to 85°C .

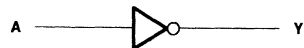
FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

logic symbol†



logic diagram, each inverter (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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INSTRUMENTS**

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SN74LVU04 HEX INVERTER

FEBRUARY 1993 – REVISED JUNE 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND pins	± 50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air):	
D package	0.7 W
DB package	0.4 W
PW package	0.4 W
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.3	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		2.4	V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		0.5	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			-6	mA
I_{OL}	Low-level output current			6	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		100	ns/V
T_A	Operating free-air temperature	-40		85	$^\circ\text{C}$

NOTE 3: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}^\ddagger	$T_A = -40^\circ\text{C}$ to 85°C			UNIT
				MIN	TYP	MAX	
V_{OH}	$V_I = V_{IL}$	$I_{OH} = -100 \mu\text{A}$	MIN to MAX	$V_{CC} - 0.5$			V
	$V_I = \text{GND}$	$I_{OH} = -6 \text{ mA}$	3 V	2.4			
V_{OL}	$V_I = V_{IH}$	$I_{OL} = 100 \mu\text{A}$	MIN to MAX	0.5			V
	$V_I = V_{CC}$	$I_{OL} = 6 \text{ mA}$	3 V	0.4			
I_I	$V_I = V_{CC}$ or GND		3.6 V	± 1			μA
I_{CC}	$V_I = V_{CC}$ or GND	$I_O = 0$	3.6 V	20			μA
ΔI_{CC}	$V_{CC} = 3$ V to 3.6 V, Other inputs at V_{CC} or GND	One input at $V_{CC} - 0.6$ V		500			μA
C_i	$V_I = V_{CC}$ or GND		3.3 V	7			pF

‡ For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

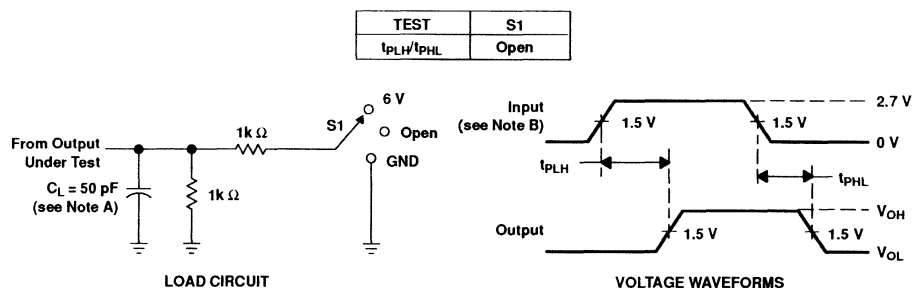
switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CC} = 2.7 \text{ V}$	UNIT
			MIN	TYP	MAX	
t_{pd}	A	Y	6	14	18	ns

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance per inverter	$C_L = 50$ pF, $f = 10$ MHz	7	pF

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 - C. The outputs are measured one at a time with one transition per measurement.

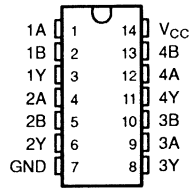
Figure 1. Load Circuit and Voltage Waveforms

SN74LV08 QUADRUPLE 2-INPUT POSITIVE-AND GATE

FEBRUARY 1993 – REVISED JUNE 1993

- **Space-Saving Package Option: Shrink Small-Outline Package (DB)**
Features EIAJ 0.65-mm Lead Pitch
- **EPIC™ (Enhanced-Performance Implanted CMOS) 2-μm Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline and Thin Shrink Small-Outline Packages**

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This quadruple 2-input positive-AND gate is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV08 performs the Boolean functions $Y = A \cdot B$ or $Y = \overline{A + B}$ in positive logic.

The SN74LV08 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV08 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

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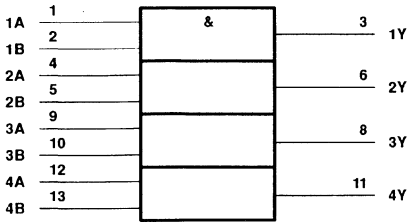


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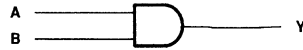
SN74LV08 QUADRUPLE 2-INPUT POSITIVE-AND GATE

FEBRUARY 1993 – REVISED JUNE 1993

logic symbol†



logic diagram, each gate (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND pins	± 50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): D package	0.7 W
..... PW package	0.4 W
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.3	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		2	V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			-6	mA
I_{OL}	Low-level output current			6	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		100	ns/V
T_A	Operating free-air temperature	-40		85	$^\circ\text{C}$

NOTE 3: Unused or floating inputs must be held high or low.

SN74LV08 QUADRUPLE 2-INPUT POSITIVE-AND GATE

FEBRUARY 1993 – REVISED JUNE 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}^\dagger	MIN	TYP	MAX	UNIT
V_{OH}	$I_{OH} = -100 \mu A$	MIN to MAX	$V_{CC} - 0.2$			V
	$I_{OH} = -6 \text{ mA}$	3 V	2.4			
V_{OL}	$I_{OL} = 100 \mu A$	MIN to MAX				V
	$I_{OL} = 6 \text{ mA}$	3 V	0.2 0.4			
I_I	$V_I = V_{CC}$ or GND	3.6 V	± 1			μA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V	20			μA
ΔI_{CC}	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$, Other inputs at V_{CC} or GND	One input at $V_{CC} - 0.6 \text{ V}$,	500			μA
C_i	$V_I = V_{CC}$ or GND	3.3 V	2.5			pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

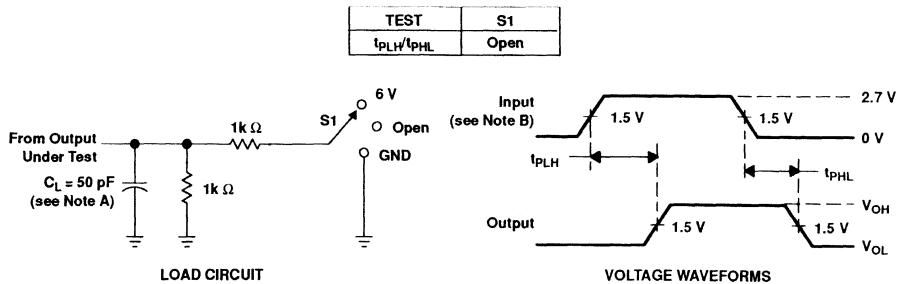
switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$			$V_{CC} = 2.7 \text{ V}$	UNIT
			MIN	TYP	MAX	MAX	
t_{pd}	A	Y	10	18	23	ns	

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ \text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance per gate	$C_L = 50 \text{ pF}$, $f = 10 \text{ MHz}$	24	pF

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 C. The outputs are measured one at a time with one transition per measurement.

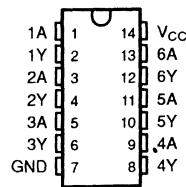
Figure 1. Load Circuit and Voltage Waveforms

SN74LV14 HEX SCHMITT-TRIGGER INVERTER

FEBRUARY 1993

- **Space-Saving Package Option:**
Shrink Small-Outline Package (DB)
Features EIAJ 0.65-mm Lead Pitch
- **EPIC™ (Enhanced-Performance Implanted CMOS) 2-μm Process**
- **Typical V_{OLP} (Output Ground Bounce)**
< 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- **Typical V_{OHV} (Output V_{OH} Undershoot)**
> 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline and Thin Shrink Small-Outline Packages**

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This hex Schmitt-trigger inverter is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV14 contains six independent inverters. The device performs the Boolean function $Y = \bar{A}$.

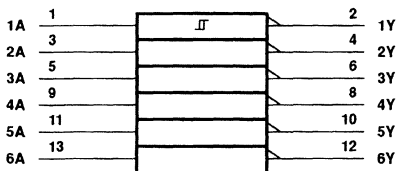
The SN74LV14 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV14 is characterized for operation from -40°C to 85°C .

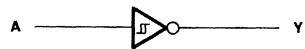
FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

logic symbol†



logic diagram, each inverter (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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 **TEXAS
INSTRUMENTS**

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SN74LV14

HEX SCHMITT-TRIGGER INVERTER

FEBRUARY 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND pins	± 50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air):	
D package	0.7 W
DB package	0.4 W
PW package	0.4 W
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.3	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		2.4	V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		0.4	V
V_I	Input voltage	0	V_{CC}		V
V_O	Output voltage	0	V_{CC}		V
I_{OH}	High-level output current			-6	mA
I_{OL}	Low-level output current			6	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	100		ns/V
T_A	Operating free-air temperature	-40	85		$^\circ\text{C}$

NOTE 3: Unused or floating inputs must be held high or low.

SN74LV14 HEX SCHMITT-TRIGGER INVERTER

FEBRUARY 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} †			UNIT
		MIN	TYP	MAX	
V _{T+}	Positive-going threshold	2.7 V	1	2	V
		3 V	1.2	2.2	
		3.6 V	1.5	2.4	
V _{T-}	Negative-going threshold	2.7 V	0.4	1.4	V
		3 V	0.6	1.5	
		3.6 V	0.8	1.8	
ΔV _T	Hysteresis (V _{T+} - V _{T-})	2.7 V	0.3	1.1	V
		3 V	0.4	1.2	
		3.6 V	0.4	1.2	
V _{OH}	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		V
	I _{OH} = -6 mA	3 V	2.4		
V _{OL}	I _{OL} = 100 μA	MIN to MAX	0.2		V
	I _{OL} = 6 mA	3 V	0.4		
I _i	V _i = V _{CC} or GND	3.6 V	±1		μA
I _{CC}	V _i = V _{CC} or GND, I _O = 0	3.6 V	20		μA
ΔI _{CC}	V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND		500		μA
C _i	V _i = V _{CC} or GND	3.3 V	2.5		pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V	UNIT
			MIN	TYP	MAX	MAX	
t _{pd}	A	Y		13	30	36	ns

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

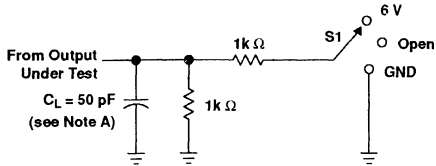
PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance	C _L = 50 pF, f = 10 MHz	22	pF

SN74LV14 HEX SCHMITT-TRIGGER INVERTER

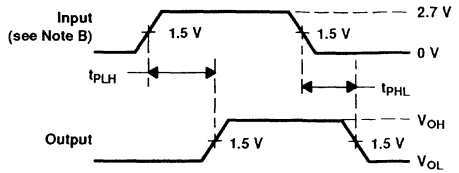
FEBRUARY 1993

PARAMETER MEASUREMENT INFORMATION

TEST	S1
t_{PLH}/t_{PHL}	Open



LOAD CIRCUIT FOR OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 C. The outputs are measured one at a time with one transition per measurement.

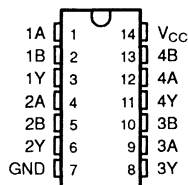
Figure 1. Load Circuit and Voltage Waveforms

SN74LV32 QUADRUPLE 2-INPUT POSITIVE-OR GATE

FEBRUARY 1993 – REVISED JUNE 1993

- **Space-Saving Package Option:**
Shrink Small-Outline Package (DB)
Features EIAJ 0.65-mm Lead Pitch
- **EPIC™ (Enhanced-Performance Implanted CMOS) 2-μm Process**
- **Typical V_{OLP} (Output Ground Bounce)**
< 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- **Typical V_{OHV} (Output V_{OH} Undershoot)**
> 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline and Thin Shrink Small-Outline Packages**

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This quadruple 2-input positive-OR gate is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV32 performs the Boolean functions $Y = A + B$ or $Y = \overline{A} \cdot \overline{B}$ in positive logic.

The SN74LV32 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV32 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

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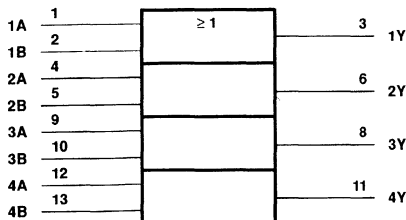


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SN74LV32 QUADRUPLE 2-INPUT POSITIVE-OR GATE

FEBRUARY 1993 – REVISED JUNE 1993

logic symbol†



logic diagram, each gate (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND pins	± 50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air):	
D package	0.7 W
DB package	0.4 W
PW package	0.4 W
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.3	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		2	V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			-6	mA
I_{OL}	Low-level output current			6	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	100		ns/V
T_A	Operating free-air temperature	-40		85	$^\circ\text{C}$

NOTE 3: Unused or floating inputs must be held high or low.

SN74LV32 QUADRUPLE 2-INPUT POSITIVE-OR GATE

FEBRUARY 1993 – REVISED JUNE 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}^{\dagger}	MIN	TYP	MAX	UNIT
V_{OH}	$I_{OH} = -100 \mu A$	MIN to MAX	$V_{CC} - 0.2$			V
	$I_{OH} = -6 \text{ mA}$	3 V	2.4			
V_{OL}	$I_{OL} = 100 \mu A$	MIN to MAX	0.2			V
	$I_{OL} = 6 \text{ mA}$	3 V	0.4			
I_I	$V_I = V_{CC}$ or GND	3.6 V	± 1			μA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V	20			μA
ΔI_{CC}	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$, Other inputs at V_{CC} or GND	One input at $V_{CC} - 0.6 \text{ V}$,	500			μA
C_i	$V_I = V_{CC}$ or GND	3.3 V	2.5			pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

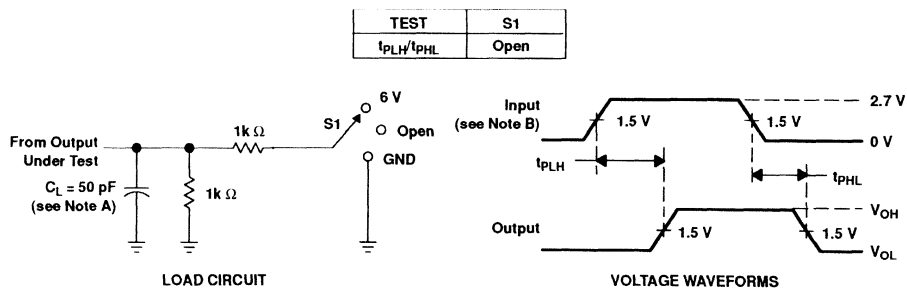
switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$			$V_{CC} = 2.7 \text{ V}$	UNIT
			MIN	TYP	MAX	MAX	
t_{pd}	A	Y	8	17	22	ns	

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance per gate	$C_L = 50 \text{ pF}$, $f = 10 \text{ MHz}$	23	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.

C. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

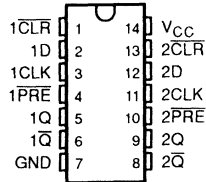
SN74LV74

DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

MAY 1993

- **Space-Saving Package Option:**
Shrink Small-Outline Package (DB)
Features EIAJ 0.65-mm Lead Pitch
- **EPIC™ (Enhanced-Performance Implanted CMOS) 2-μm Process**
- **Typical V_{OLP} (Output Ground Bounce)**
< 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- **Typical V_{OHV} (Output V_{OH} Undershoot)**
> 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline and Thin Shrink Small-Outline Packages**

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This dual positive-edge-triggered D-type flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation.

A low level at the preset ($\overline{\text{PRE}}$) or clear ($\overline{\text{CLR}}$) inputs sets or resets the outputs regardless of the levels of the other inputs. When $\overline{\text{PRE}}$ and $\overline{\text{CLR}}$ are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input may be changed without affecting the levels at the outputs.

The SN74LV74 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV74 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

INPUTS				OUTPUTS	
PRE	CLR	CLK	D	Q	\overline{Q}
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	\overline{Q}_0

† This configuration is nonstable; that is, it will not persist when $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ returns to its inactive (high) level.

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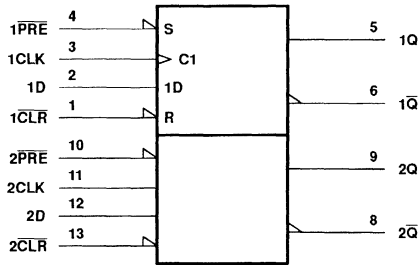
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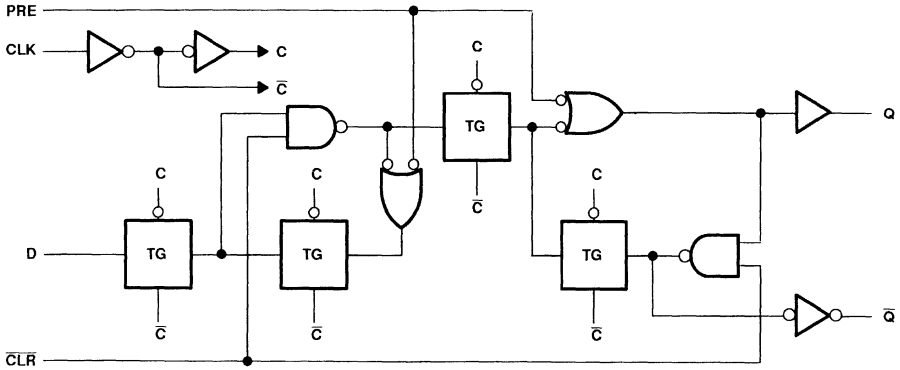
SN74LV74
DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP
WITH CLEAR AND PRESET
 MAY 1993

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each flip-flop (positive logic)



SN74LV74

DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

MAY 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND pins	± 50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air):		
D package	0.7 W
DB package	0.4 W
PW package	0.4 W
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.3	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		2	V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			-6	mA
I_{OL}	Low-level output current			6	mA
$\Delta t_{\Delta v}$	Input transition rise or fall rate	0		100	ns/V
T_A	Operating free-air temperature	-40		85	$^\circ\text{C}$

NOTE 3: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}^\ddagger	MIN	TYP	MAX	UNIT
V_{OH}	$I_{OH} = -100$ μA		MIN to MAX	$V_{CC} - 0.2$			V
	$I_{OH} = -6$ mA		3 V	2.4			
V_{OL}	$I_{OL} = 100$ μA		MIN to MAX			0.2	V
	$I_{OL} = 6$ mA		3 V			0.4	
I_I	$V_I = V_{CC}$ or GND		3.6 V			± 1	μA
I_{CC}	$V_I = V_{CC}$ or GND,	$I_O = 0$	3.6 V			20	μA
ΔI_{CC}	$V_{CC} = 3$ V to 3.6 V, Other inputs at V_{CC} or GND	One input at $V_{CC} - 0.6$ V,				500	μA
C_i	$V_I = V_{CC}$ or GND		3.3 V		2.5		pF

‡ For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions

SN74LV74
DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP
WITH CLEAR AND PRESET
MAY 1993

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			$V_{CC} = 2.7\text{ V}$		UNIT
		MIN	TYP	MAX	MIN	MAX	
f_{clock}	Clock frequency	0		24	0	19	MHz
t_w	Pulse duration	PRE or CLR low		20	25		ns
		CLK high or low		20	25		
t_{su}	Setup time before CLK↑	Data		13	16		ns
		PRE or CLR inactive		8	10		
t_h	Hold time, data after CLK↑	3			3		ns

switching characteristics over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			$V_{CC} = 2.7\text{ V}$		UNIT
			MIN	TYP	MAX	MIN	MAX	
f_{max}			24	100		19		MHz
t_{pd}	PRE or CLR	Q or \bar{Q}		16	34		43	ns
t_{pd}	CLK	Q or \bar{Q}		15	28		35	ns

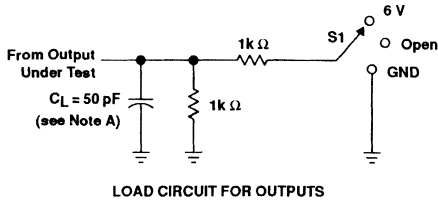
operating characteristics, $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	32	pF

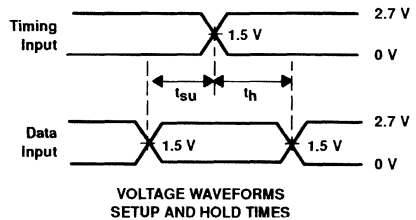
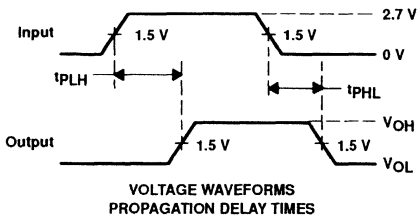
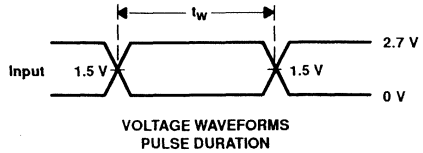
SN74LV74 DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

MAY 1993

PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLH}/t_{PHL}	Open



- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_o = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 C. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

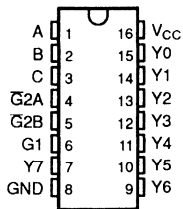
SN74LV138

3-LINE TO 8-LINE DECODER/DEMULTIPLEXER

FEBRUARY 1993 – REVISED JULY 1993

- **Space-Saving Package Option: Shrink Small-Outline Package (DB) Features EIAJ 0.65-mm Lead Pitch**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 2- μ m Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline and Thin Shrink Small-Outline Packages**

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This 3-line to 8-line decoder/demultiplexer is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV138 is designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, this decoder can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The conditions at the binary-select inputs and the three enable inputs select one of eight input lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The SN74LV138 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV138 is characterized for operation from -40°C to 85°C .

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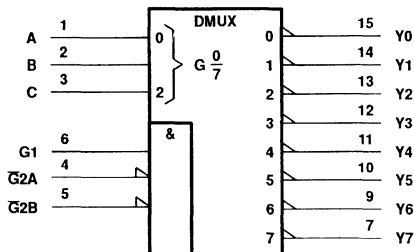
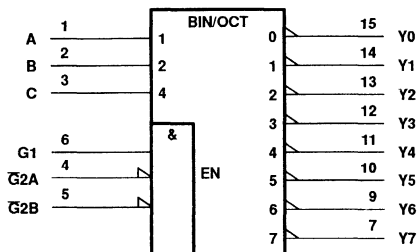
SN74LV138 3-LINE TO 8-LINE DECODER/DEMULTIPLEXER

FEBRUARY 1993 – REVISED JULY 1993

FUNCTION TABLE

ENABLE INPUTS			SELECT INPUTS			OUTPUTS							
G1	G2A	G2B	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

logic symbols (alternatives)†

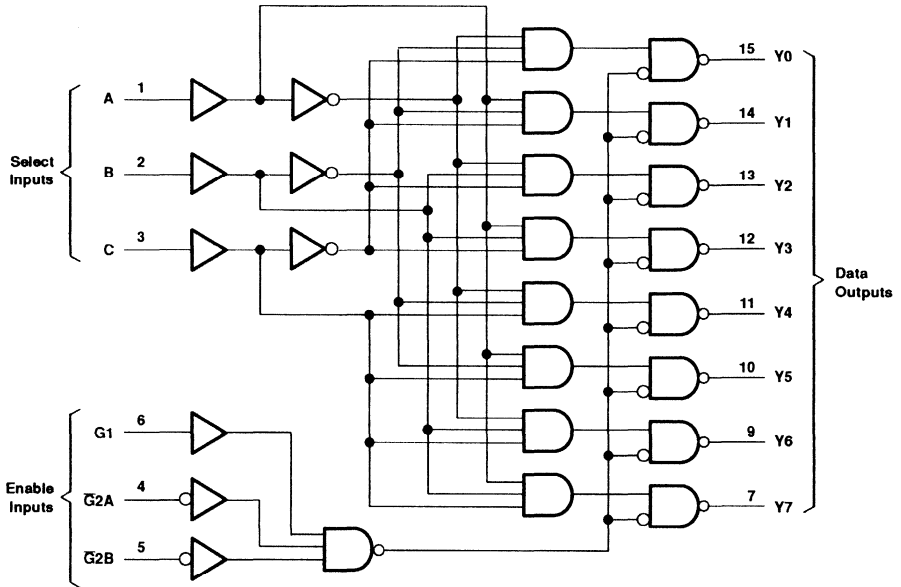


† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN74LV138 3-LINE TO 8-LINE DECODER/DEMULTIPLEXER

FEBRUARY 1993 – REVISED JULY 1993

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND pins	± 50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air):	
D package	0.7 W
DB package	0.4 W
PW package	0.4 W
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.

SN74LV138

3-LINE TO 8-LINE DECODER/DEMULTIPLEXER

FEBRUARY 1993 – REVISED JULY 1993

recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.3	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$		2	V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$		0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			-6	mA
I_{OL}	Low-level output current			6	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		100	ns/V
T_A	Operating free-air temperature	-40		85	°C

NOTE 3: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}^\dagger	MIN	TYP	MAX	UNIT
V_{OH}	$I_{OH} = -100\ \mu\text{A}$	MIN to MAX	$V_{CC} - 0.2$			V
	$I_{OH} = -6\ \text{mA}$	3 V	2.4			
V_{OL}	$I_{OL} = 100\ \mu\text{A}$	MIN to MAX			0.2	V
	$I_{OL} = 6\ \text{mA}$	3 V			0.4	
I_I	$V_I = V_{CC}$ or GND	3.6 V			± 1	μA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			20	μA
ΔI_{CC}	$V_{CC} = 3\text{ V to }3.6\text{ V}$, Other inputs at V_{CC} or GND	One input at $V_{CC} - 0.6\text{ V}$,			500	μA
C_i	$V_I = V_{CC}$ or GND	3.3 V		2.5		pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, $C_L = 50\ \text{pF}$ (unless otherwise noted) (see Figure 1)

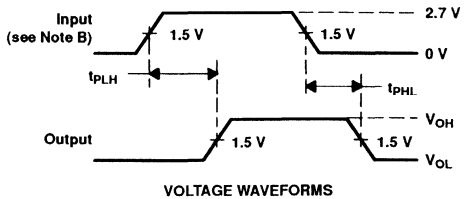
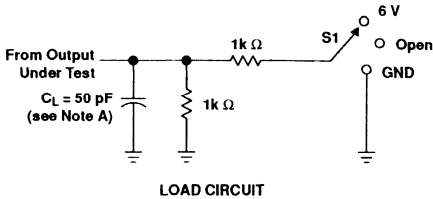
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			$V_{CC} = 2.7\text{ V}$	UNIT
			MIN	TYP	MAX	MAX	
t_{pd}	A, B or C	Y	14	29	36	ns	
t_{pd}	Enable	Y	16	33	41	ns	

operating characteristics, $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per channel $C_L = 50\ \text{pF}$, $f = 10\ \text{MHz}$	47	pF

PARAMETER MEASUREMENT INFORMATION

TEST	S1
t_{PLH}/t_{PHL}	Open



- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 C. The outputs are measured one at a time with one transition per measurement.

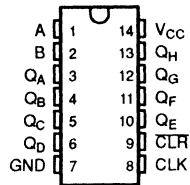
Figure 1. Load Circuit and Voltage Waveforms

SN74LV164 8-BIT PARALLEL-OUT SERIAL SHIFT REGISTER

NOVEMBER 1993

- **Space-Saving Package Option: Shrink Small-Outline Package (DB)**
Features EIAJ 0.65-mm Lead Pitch
- **EPIC™ (Enhanced-Performance Implanted CMOS) 2-μm Process**
- **Typical V_{OLP} (Output Ground Bounce)**
< 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- **Typical V_{OHV} (Output V_{OH} Undershoot)**
> 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline and Thin Shrink Small-Outline Packages**

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This 8-bit parallel-out serial shift register is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV164 features AND-gated serial (A and B) inputs and an asynchronous clear ($\overline{\text{CLR}}$) input. The gated serial inputs permit complete control over incoming data as a low at either input inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input, which then determines the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, provided the minimum setup time requirements are met. Clocking occurs on the low-to-high-level transition of the clock (CLK) input.

The SN74LV164 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV164 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

INPUTS				OUTPUTS		
CLR	CLK	A	B	Q_A	$Q_B \dots Q_H$	
L	X	X	X	L	L	L
H	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	↑	H	H	H	Q_{An}	Q_{Gn}
H	↑	L	X	L	Q_{An}	Q_{Gn}
H	↑	X	L	L	Q_{An}	Q_{Gn}

Q_{A0} , Q_{B0} , Q_{H0} = the level of Q_A , Q_B , or Q_H , respectively, before the indicated steady-state inputs conditions were established.

Q_{An} , Q_{Gn} = the level of Q_A or Q_G before the most recent ↑ transition of the clock; indicates a one-bit shift.

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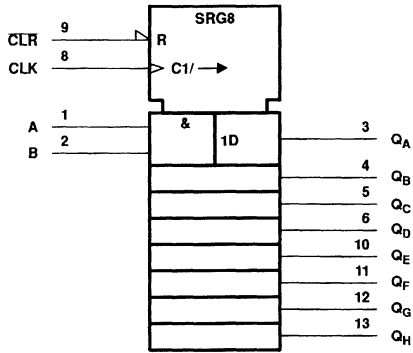
PRODUCT PREVIEW

SN74LV164

8-BIT PARALLEL-OUT SERIAL SHIFT REGISTER

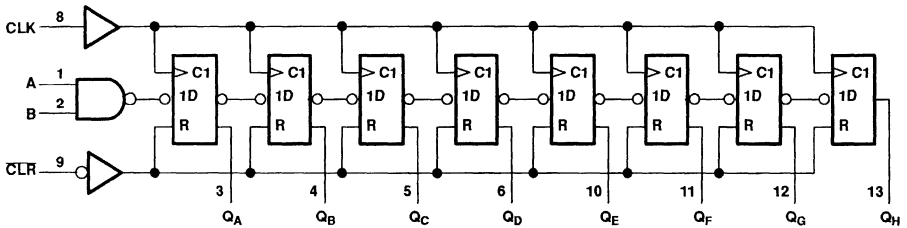
NOVEMBER 1993

logic symbol†



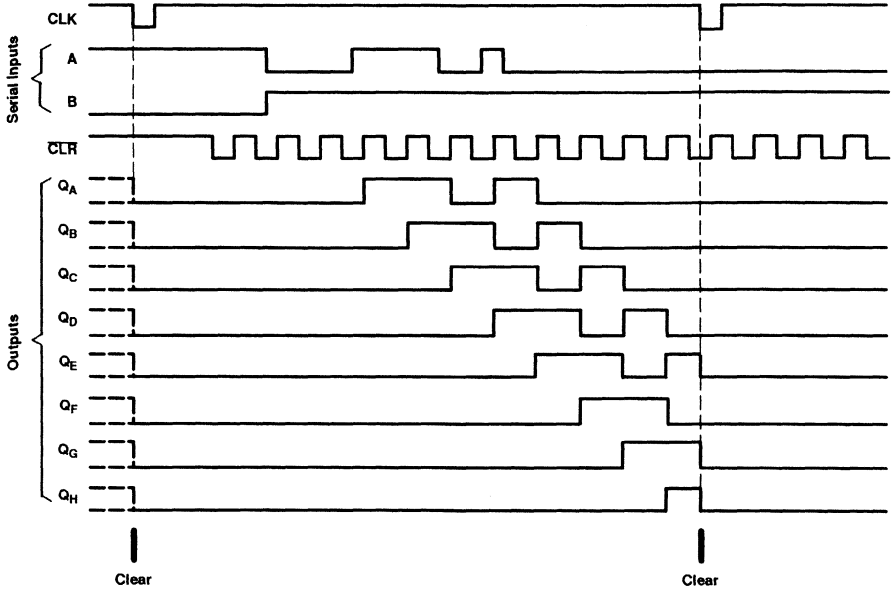
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

typical clear, shift, and clear sequences



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND pins	± 50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air):	
D package	0.7 W
DB package	0.4 W
PW package	0.4 W
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.

PRODUCT PREVIEW

SN74LV164

8-BIT PARALLEL-OUT SERIAL SHIFT REGISTER

NOVEMBER 1993

recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.3	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$		2	V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$		0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			-6	mA
I_{OL}	Low-level output current			6	mA
$\Delta V/\Delta t$	Input transition rise or fall rate	0		100	ns/V
T_A	Operating free-air temperature	-40		85	°C

NOTE 3: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}^\dagger	MIN	TYP	MAX	UNIT
V_{OH}	$I_{OH} = -100\ \mu\text{A}$	MIN to MAX	$V_{CC} - 0.2$			V
	$I_{OH} = -6\ \text{mA}$	3 V	2.4			
V_{OL}	$I_{OL} = 100\ \mu\text{A}$	MIN to MAX			0.2	V
	$I_{OL} = 6\ \text{mA}$	3 V			0.4	
I_I	$V_I = V_{CC}$ or GND	3.6 V			± 1	μA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			20	μA
ΔI_{CC}	$V_{CC} = 3\text{ V to }3.6\text{ V}$, Other inputs at V_{CC} or GND	One input at $V_{CC} - 0.6\text{ V}$,			500	μA
C_i	$V_I = V_{CC}$ or GND	3.3 V	TBD			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		UNIT
		MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency					MHz
t_w	Pulse duration	CLR low				ns
		CLK high or low				
t_{su}	Setup time before CLK \uparrow	Data				ns
		CLR inactive				
t_h	Hold time, data after CLK \uparrow					ns

SN74LV164 8-BIT PARALLEL-OUT SERIAL SHIFT REGISTER

NOVEMBER 1993

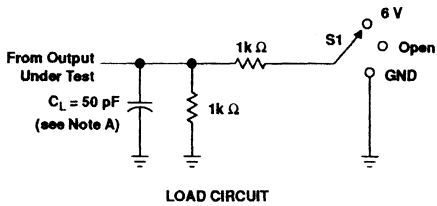
switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$			$V_{CC} = 2.7 \text{ V}$		UNIT
			MIN	TYP	MAX	MIN	MAX	
f_{max}								MHz
t_{pd}	CLR	Q						ns
	CLK							

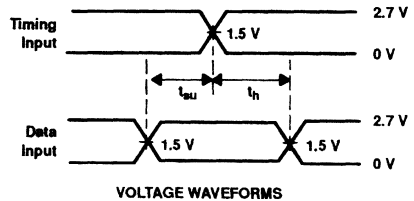
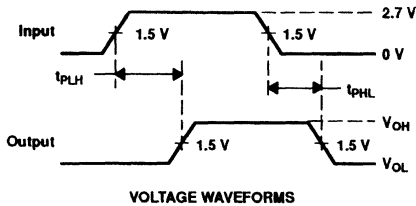
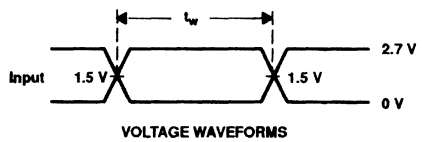
operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance per flip-flop	$C_L = 50$ pF, $f = 10$ MHz		pF

PARAMETER MEASUREMENT INFORMATION



TEST	S1
$t_{\text{PLH}}/t_{\text{PHL}}$	Open



- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 C. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

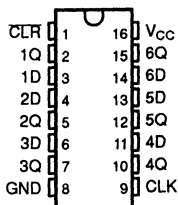
PRODUCT PREVIEW

SN74LV174 HEX D-TYPE FLIP-FLOP WITH CLEAR

FEBRUARY 1993 – REVISED JULY 1993

- **EPIC™ (Enhanced-Performance Implanted CMOS) 2- μ m Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (SOIC), Shrink Small-Outline (SSOP), and Thin Shrink Small-Outline (TSSOP) Packages**

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This hex D-type flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV174 is a monolithic positive-edge-triggered flip-flop with a direct clear ($\overline{\text{CLR}}$) input. Information at the data (D) inputs meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going edge of the clock pulse. When the clock input is at either the high or low level, the D-input signal has no effect at the output.

The SN74LV174 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV174 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

INPUTS			OUTPUT
CLR	CLK	D	Q
L	X	X	L
H	\uparrow	H	H
H	\uparrow	L	L
H	L	X	Q_0

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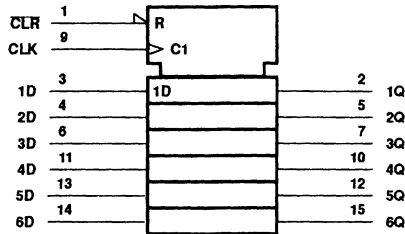
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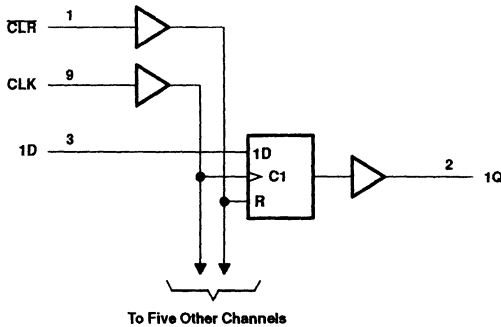
SN74LV174
HEX D-TYPE FLIP-FLOP
WITH CLEAR
 FEBRUARY 1993 – REVISED JULY 1993

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND pins	± 50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air):	
D package	0.7 W
DB package	0.4 W
PW package	0.4 W
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.



recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	2.7	3.3	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V		2	V
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	V
V _I	Input voltage	0	V _{CC}		V
V _O	Output voltage	0	V _{CC}		V
I _{OH}	High-level output current			-6	mA
I _{OL}	Low-level output current			6	mA
Δt/Δv	Input transition rise or fall rate	0	100		ns/V
T _A	Operating free-air temperature	-40	85		°C

NOTE 3: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} †	MIN	TYP	MAX	UNIT
V _{OH}	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2			V
	I _{OH} = -6 mA	3 V	2.4			
V _{OL}	I _{OL} = 100 μA	MIN to MAX			0.2	V
	I _{OL} = 6 mA	3 V			0.4	
I _I	V _I = V _{CC} or GND	3.6 V			±1	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V			20	μA
ΔI _{CC}	V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND				500	μA
C _I	V _I = V _{CC} or GND	3.3 V	2.5			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT
		MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	0	24	0	19	MHz
t _w	Pulse duration	CLR low	20	25		ns
		CLK high or low	20	25		
t _{su}	Setup time before CLK↑	Data	13	16		ns
		CLR inactive	5	5		
t _h	Hold time, data after CLK↑	5	5		ns	

SN74LV174
HEX D-TYPE FLIP-FLOP
WITH CLEAR

FEBRUARY 1993 – REVISED JULY 1993

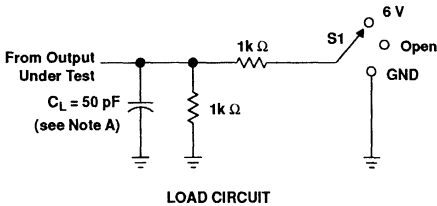
switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$			$V_{CC} = 2.7 \text{ V}$		UNIT
			MIN	TYP	MAX	MIN	MAX	
f_{max}			24	80		19		MHz
t_{pd}	CLR	Q		12	26		33	ns
	CLK			13	33		41	

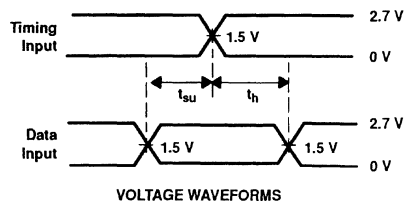
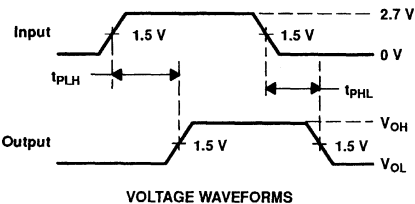
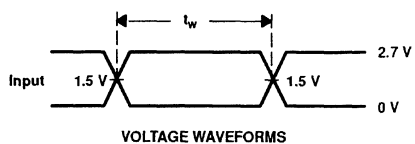
operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance per flip-flop	$C_L = 50 \text{ pF}$, $f = 10 \text{ MHz}$	24	pF

PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLH}/t_{PHL}	Open



- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 C. The outputs are measured one at a time with one transition per measurement.

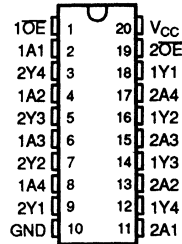
Figure 1. Load Circuit and Voltage Waveforms



SN74LV240
OCTAL BUFFER/DRIVER
WITH 3-STATE OUTPUTS
 FEBRUARY 1993

- **Space-Saving Package Option:**
 Shrink Small-Outline Package (DB)
 Features EIAJ 0.65-mm Lead Pitch
- **EPIC™ (Enhanced-Performance Implanted CMOS) 2- μ m Process**
- **Typical V_{OLP} (Output Ground Bounce)**
 < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- **Typical V_{OHV} (Output V_{OH} Undershoot)**
 > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline and Thin Shrink Small-Outline Packages**

DB, DW, OR PW PACKAGE
 (TOP VIEW)



description

This octal buffer/driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV240 is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The SN74LV240 is organized as two 4-bit buffers/line drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

The SN74LV240 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV240 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
 (each buffer)

INPUTS		OUTPUT
\overline{OE}	A	Y
L	H	L
L	L	H
H	X	Z

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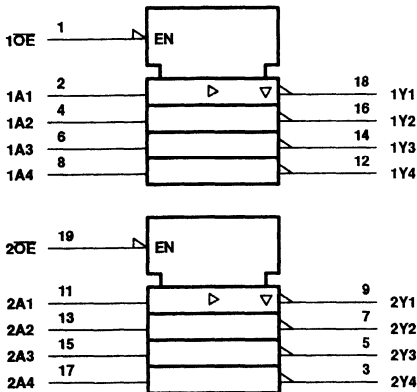
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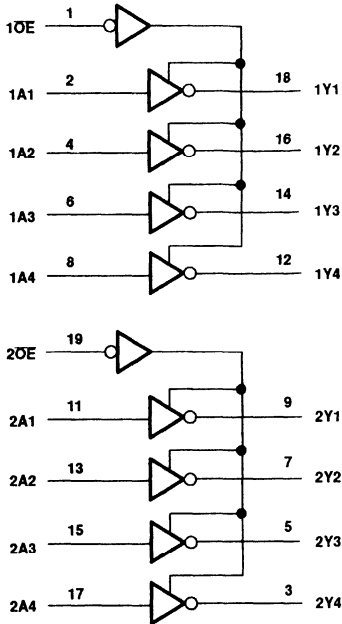
SN74LV240
OCTAL BUFFER/DRIVER
WITH 3-STATE OUTPUTS
 FEBRUARY 1993

logic symbol



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 35 mA
Continuous current through V_{CC} or GND pins	± 70 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air):	
DB package	0.5 W
DW package	0.85 W
PW package	0.5 W
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.

SN74LV240
OCTAL BUFFER/DRIVER
WITH 3-STATE OUTPUTS
FEBRUARY 1993

recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	2.7	3.3	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V		2	V
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	V
V _I	Input voltage	0	V _{CC}		V
V _O	Output voltage	0	V _{CC}		V
I _{OH}	High-level output current			-8	mA
I _{OL}	Low-level output current			8	mA
Δt/Δv	Input transition rise or fall rate	0	100		ns/V
T _A	Operating free-air temperature	-40		85	°C

NOTE 3: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} †	MIN	TYP	MAX	UNIT
V _{OH}	I _{OH} = -100 μA	MIN to MAX	V _{CC} - 0.2			V
	I _{OH} = -8 mA	3 V	2.4			
V _{OL}	I _{OL} = 100 μA	MIN to MAX			0.2	V
	I _{OL} = 8 mA	3 V			0.4	
I _I	V _I = V _{CC} or GND	3.6 V			±1	μA
I _{OZ}	V _O = V _{CC} or GND	3.6 V			±5	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V			20	μA
ΔI _{CC}	V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND				500	μA
C _I	V _I = V _{CC} or GND	3.3 V		3		pF
C _O	V _O = V _{CC} or GND	3.3 V		8		pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

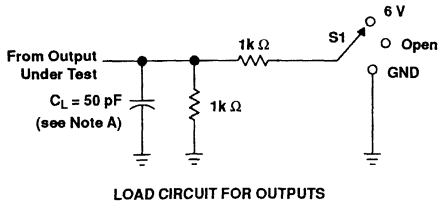
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V	UNIT
			MIN	TYP	MAX	
t _{pd}	A	Y		21	26	ns
t _{gn}	OE	Y		28	35	ns
t _{dis}				27	33	

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

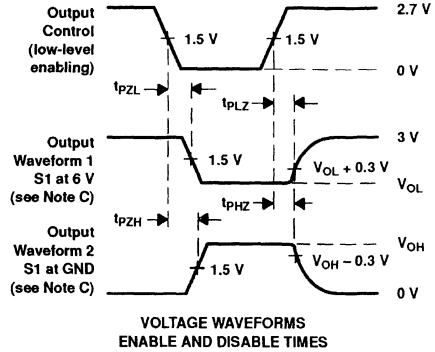
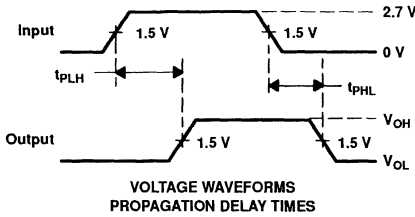
PARAMETER		TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance	Outputs enabled	45	pF
		Outputs disabled	2.5	

C_L = 50 pF, f = 10 MHz

PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

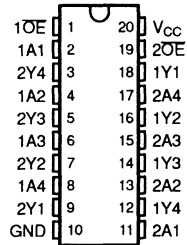
SN74LV244

OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUTS

FEBRUARY 1993

- **Space-Saving Package Option:**
Shrink Small-Outline Package (DB)
Features EIAJ 0.65-mm Lead Pitch
- **EPIC™ (Enhanced-Performance Implanted CMOS) 2-μm Process**
- **Typical V_{OLP} (Output Ground Bounce)**
< 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- **Typical V_{OHV} (Output V_{OH} Undershoot)**
> 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (DW) and Thin Shrink Small-Outline (PW) Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal buffer/line driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV244 is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The SN74LV244 is organized as two 4-bit line drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

The SN74LV244 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV244 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
\overline{OE}	A	Y
L	H	H
L	L	L
H	X	Z

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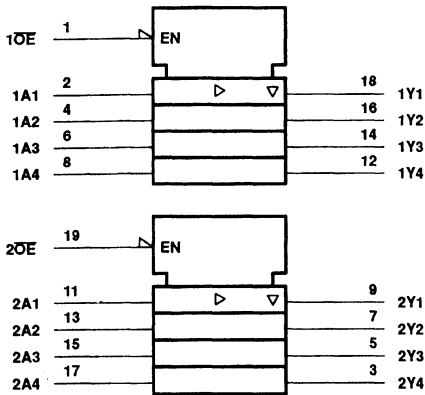
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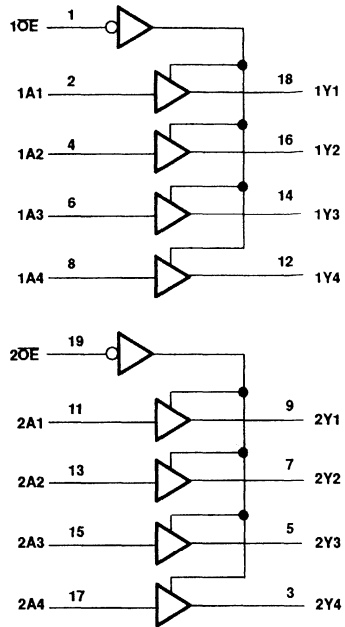
SN74LV244
OCTAL BUFFER/LINE DRIVER
WITH 3-STATE OUTPUTS
 FEBRUARY 1993

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 35 mA
Continuous current through V_{CC} or GND pins	± 70 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air):	
DB package	0.5 W
DW package	0.85 W
PW package	0.5 W
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	2.7	3.3	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V		2	V
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	V
V _I	Input voltage	0	V _{CC}		V
V _O	Output voltage	0	V _{CC}		V
I _{OH}	High-level output current			-8	mA
I _{OL}	Low-level output current			8	mA
ΔV/ΔV	Input transition rise or fall rate	0	100		ns/V
T _A	Operating free-air temperature	-40	85		°C

NOTE 3: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = -40°C to 85°C			UNIT
			MIN	TYP	MAX	
V _{OH}	I _{OH} = -100 μA	MIN to MAX†	V _{CC} - 0.2			V
	I _{OH} = -8 mA	3 V	2.4			
V _{OL}	I _{OL} = 100 μA	MIN to MAX†	0.2			V
	I _{OL} = 8 mA	3 V	0.4			
I _I	V _I = V _{CC} or GND	3.6 V	±1			μA
I _{OZ}	V _O = V _{CC} or GND	3.6 V	±5			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V	20			μA
ΔI _{CC}	V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND		500			μA
C _I	V _I = V _{CC} or GND	3.3 V	3			pF
C _O	V _O = V _{CC} or GND	3.3 V	8			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

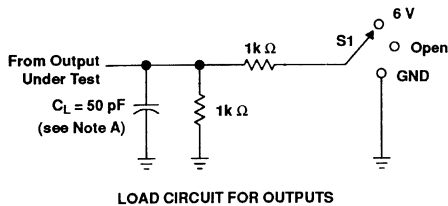
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V	UNIT
			MIN	TYP	MAX	MAX	
t _{pd}	A	Y	10	19	24	ns	
t _{on}	OE	Y	14	26	33	ns	
			15	26	32		

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

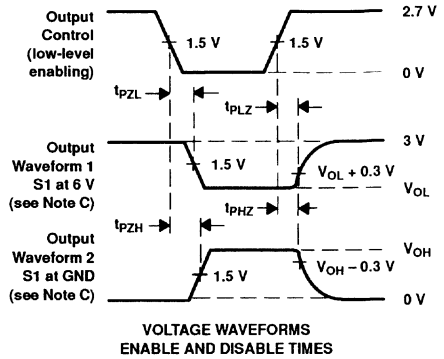
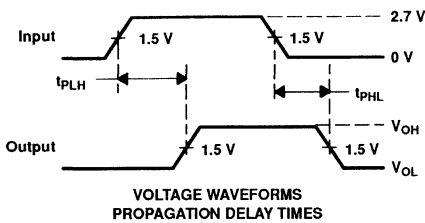
PARAMETER		TEST CONDITIONS		TYP	UNIT
C _{pd}	Power dissipation capacitance	Outputs enabled	C _L = 50 pF, f = 10 MHz	40	pF
		Outputs disabled		4	

SN74LV244
OCTAL BUFFER/LINE DRIVER
WITH 3-STATE OUTPUTS
 FEBRUARY 1993

PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_0 = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one transition per measurement.

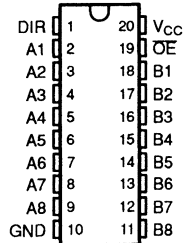
Figure 1. Load Circuit and Voltage Waveforms

SN74LV245 OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCLS075A – JANUARY 1991 – REVISED AUGUST 1993

- EPIC™ (Enhanced-Performance Implanted CMOS) 2- μ m Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (SOIC) and Thin Shrink Small-Outline (TSSOP) Packages

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal bus transceiver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV245 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so the buses are effectively isolated.

The SN74LV245 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV245 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

INPUTS		OPERATION
\overline{OE}	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

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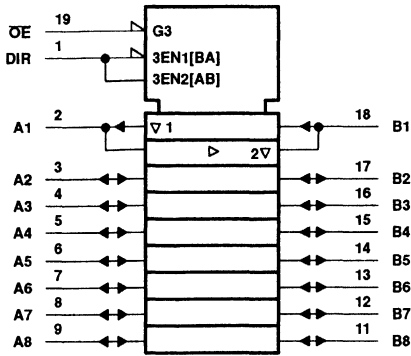


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SN74LV245
OCTAL BUS TRANSCEIVER
WITH 3-STATE OUTPUTS

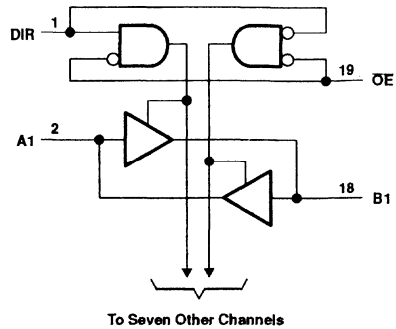
SCLS075A – JANUARY 1991 – REVISED AUGUST 1993

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 35 mA
Continuous current through V_{CC} or GND pins	± 70 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DB package	0.5 W
..... DW package	0.85 W
..... PW package	0.5 W
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.

SN74LV245
OCTAL BUS TRANSCEIVER
WITH 3-STATE OUTPUTS

SCLS075A – JANUARY 1991 – REVISED AUGUST 1993

recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.3	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$		2	V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$		0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			-8	mA
I_{OL}	Low-level output current			8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		50	ns/V
T_A	Operating free-air temperature	-40		85	°C

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}^\dagger	MIN	TYP	MAX	UNIT
V_{OH}	$I_{OH} = -100\ \mu\text{A}$	MIN to MAX	$V_{CC} - 0.2$			V
	$I_{OH} = -8\ \text{mA}$	3 V	2.4			
V_{OL}	$I_{OL} = 100\ \mu\text{A}$	MIN to MAX			0.2	V
	$I_{OL} = 8\ \text{mA}$	3 V			0.4	
I_I	$V_I = V_{CC}$ or GND	3.6 V			± 1	μA
I_{OZ}^\ddagger	$V_O = V_{CC}$ or GND	3.6 V			± 5	μA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			20	μA
ΔI_{CC}	$V_{CC} = 3\text{ V to }3.6\text{ V}$, Other inputs at V_{CC} or GND	One input at $V_{CC} - 0.6\text{ V}$,			500	μA
C_I	Control inputs	$V_I = V_{CC}$ or GND	3.3 V		2.5	pF
$C_{I/O}$	A or B ports	$V_O = V_{CC}$ or GND	3.3 V		7	pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

switching characteristics over recommended operating free-air temperature range, $C_L = 50\ \text{pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			$V_{CC} = 2.7\text{ V}$	UNIT
			MIN	TYP	MAX	MAX	
t_{pd}	A or B	B or A		8	18	23	ns
t_{en}	OE	A or B		13	23	29	ns
t_{dis}	OE	A or B		14	26	32	ns

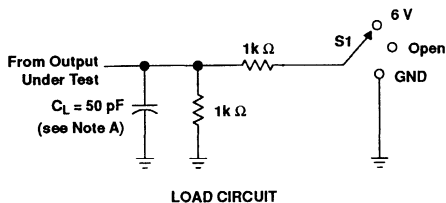
operating characteristics, $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	$C_L = 50\ \text{pF}$, $f = 10\ \text{MHz}$	pF
	Outputs enabled		
	Outputs disabled		4

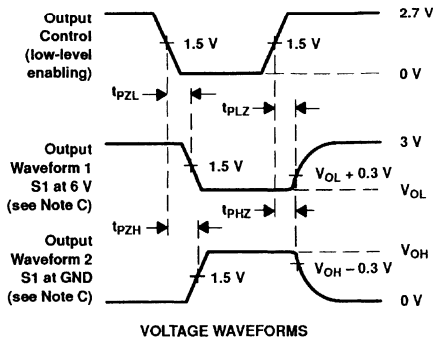
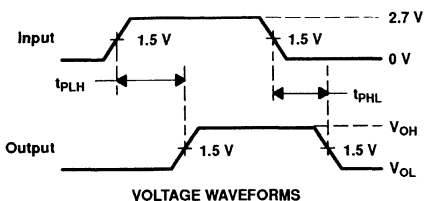
SN74LV245
OCTAL BUS TRANSCEIVER
WITH 3-STATE OUTPUTS

SCLS075A – JANUARY 1991 – REVISED AUGUST 1993

PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

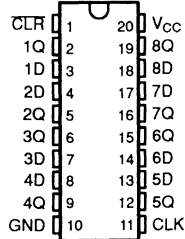


- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Space-Saving Package Option:**
 Shrink Small-Outline Package (DB)
 Features EIAJ 0.65-mm Lead Pitch
- **EPIC™ (Enhanced-Performance Implanted CMOS) 2-µm Process**
- **Typical V_{OLP} (Output Ground Bounce)**
 $< 0.8\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$
- **Typical V_{OHV} (Output V_{OH} Undershoot)**
 $> 2\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ($C = 200\text{ pF}$, $R = 0$)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline and Thin Shrink Small-Outline Packages**

DB, DW, OR PW PACKAGE
 (TOP VIEW)



description

This octal D-type flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV273 is a positive-edge-triggered flip-flop with a direct clear input. Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock (CLK) input is at either the high or low level, the D-input signal has no effect at the output.

The SN74LV273 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV273 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
 (each flip-flop)

INPUTS			OUTPUT
CLR	CLK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

PRODUCT PREVIEW

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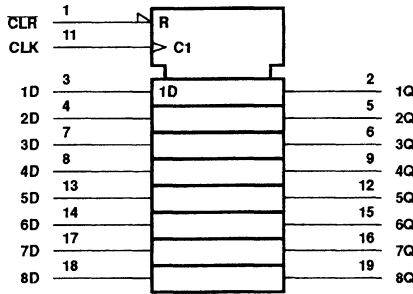
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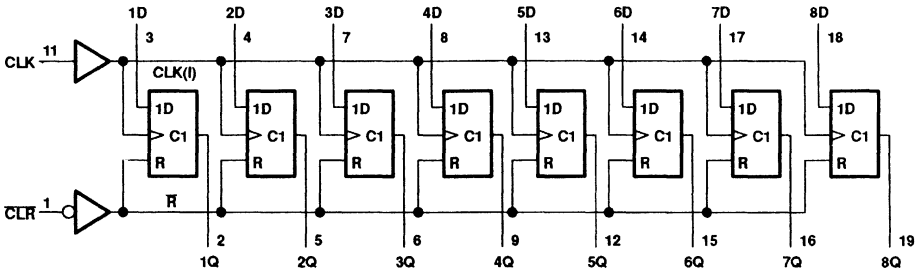
SN74LV273
OCTAL D-TYPE FLIP-FLOP
WITH CLEAR
 NOVEMBER 1993

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 35 mA
Continuous current through V_{CC} or GND pins	± 70 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air):	
DB package	0.5 W
DW package	0.85 W
PW package	0.5 W
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.



recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.3	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$		2	V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$		0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			-8	mA
I_{OL}	Low-level output current			8	mA
$\Delta V/\Delta V$	Input transition rise or fall rate	0		100	ns/V
T_A	Operating free-air temperature	-40		85	°C

NOTE 3: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}^\dagger	MIN	TYP	MAX	UNIT
V_{OH}	$I_{OH} = -100\ \mu\text{A}$	MIN to MAX	$V_{CC} - 0.2$			V
	$I_{OH} = -6\ \text{mA}$	3 V	2.4			
V_{OL}	$I_{OL} = 100\ \mu\text{A}$	MIN to MAX			0.2	V
	$I_{OL} = 6\ \text{mA}$	3 V			0.4	
I_I	$V_I = V_{CC}$ or GND	3.6 V			± 1	μA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			20	μA
ΔI_{CC}	$V_{CC} = 3\text{ V to }3.6\text{ V}$, Other inputs at V_{CC} or GND One input at $V_{CC} - 0.6\text{ V}$,				500	μA
C_I	$V_I = V_{CC}$ or GND	3.3 V		TBD		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		UNIT
		MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency					MHz
t_w	Pulse duration	CLR low				ns
		CLK high or low				
t_{su}	Setup time before CLK \uparrow	Data				ns
		CLR inactive				
t_h	Hold time, data after CLK \uparrow					ns

PRODUCT PREVIEW

SN74LV273
OCTAL D-TYPE FLIP-FLOP
WITH CLEAR
 NOVEMBER 1993

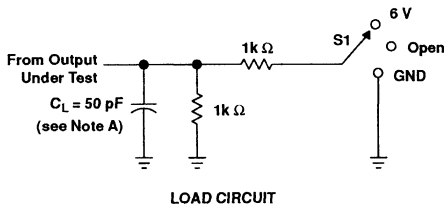
switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$			$V_{CC} = 2.7 \text{ V}$		UNIT
			MIN	TYP	MAX	MIN	MAX	
f_{max}								MHz
t_{pd}	CLR	Q						ns
	CLK							

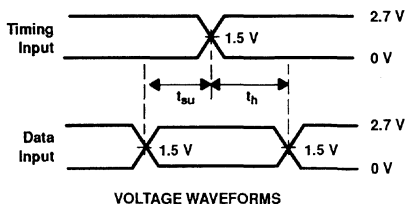
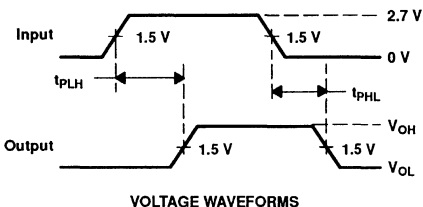
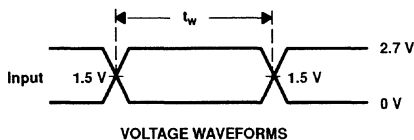
operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance per flip-flop	$C_L = 50 \text{ pF}$, $f = 10 \text{ MHz}$		pF

PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLH}/t_{PHL}	Open



- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 C. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

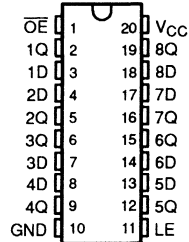
SN74LV373

OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

FEBRUARY 1993 – REVISED SEPTEMBER 1993

- **EPIC™ (Enhanced-Performance Implanted CMOS) 2- μ m Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (SOIC), Shrink Small-Outline (SSOP), and Thin Shrink Small-Outline (TSSOP) Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal transparent D-type latch is designed for 2.7-V to 3.6-V V_{CC} operation.

While the latch-enable (LE) input is high, the Q outputs will follow the data (D) inputs. When the latch enable is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (\overline{OE}) input does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74LV373 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV373 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each latch)

INPUTS			OUTPUT
\overline{OE}	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

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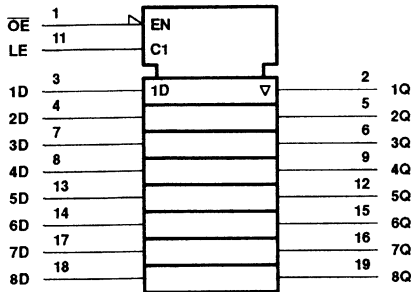
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



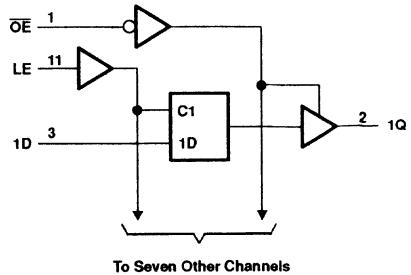
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SN74LV373
OCTAL TRANSPARENT D-TYPE LATCH
WITH 3-STATE OUTPUTS
 FEBRUARY 1993 - REVISED SEPTEMBER 1993

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 35 mA
Continuous current through V_{CC} or GND pins	± 70 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air):	
DB package	0.5 W
DW package	0.85 W
PW package	0.5 W
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.3	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		2	V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		0.8	V
V_I	Input voltage	0	V_{CC}		V
V_O	Output voltage	0	V_{CC}		V
I_{OH}	High-level output current			-8	mA
I_{OL}	Low-level output current			8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	100		ns/V
T_A	Operating free-air temperature	-40		85	$^\circ\text{C}$

NOTE 3: Unused or floating inputs must be held high or low.



SN74LV373
OCTAL TRANSPARENT D-TYPE LATCH
WITH 3-STATE OUTPUTS

FEBRUARY 1993 - REVISED SEPTEMBER 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} †	MIN	TYP	MAX	UNIT
V _{OH}	I _{OH} = -100 µA	MIN to MAX	V _{CC} -0.2			V
	I _{OH} = -8 mA	3 V	2.4			
V _{OL}	I _{OL} = 100 µA	MIN to MAX	0.2			V
	I _{OL} = 8 mA	3 V	0.4			
I _I	V _I = V _{CC} or GND	3.6 V	±1			µA
I _{OZ}	V _O = V _{CC} or GND	3.6 V	±5			µA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V	20			µA
ΔI _{CC}	V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC} or GND	One input at V _{CC} - 0.6 V,	500			µA
C _i	V _I = V _{CC} or GND	3.3 V	2.5			pF
C _o	V _O = V _{CC} or GND	3.3 V	7			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT	
		MIN	MAX	MIN	MAX		
t _w	Pulse duration, LE high	20		25		ns	
t _{SU}	Setup time, data before LE↓	High or low		10		13	ns
t _H	Hold time, data after LE↓	High or low		10		10	ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V	UNIT
			MIN	TYP	MAX	MAX	
t _{pd}	D	Q	11		25	31	ns
	LE		15		29	36	
t _{en}	OE	Q	15		29	36	ns
t _{dis}	OE	Q	15		29	36	ns

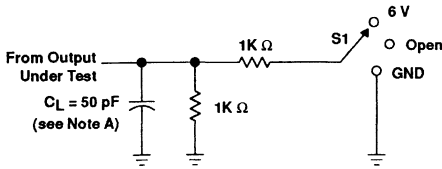
operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance per latch	Outputs enabled	47	pF
		Outputs disabled	29	

SN74LV373
OCTAL TRANSPARENT D-TYPE LATCH
WITH 3-STATE OUTPUTS

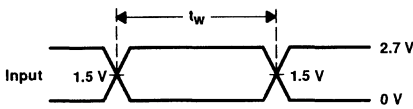
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PARAMETER MEASUREMENT INFORMATION

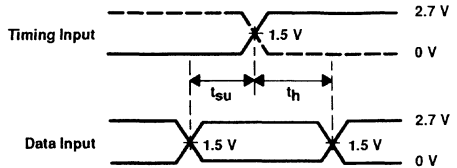


LOAD CIRCUIT FOR OUTPUTS

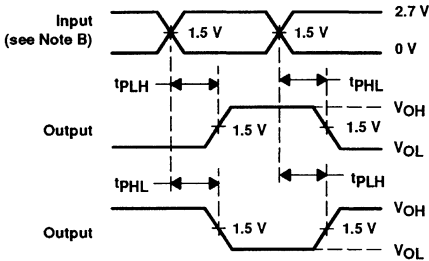
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



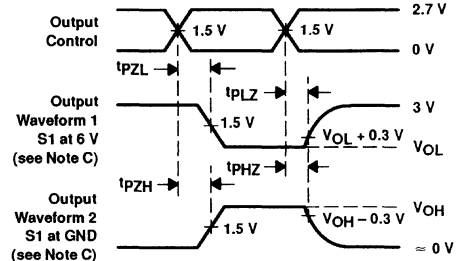
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

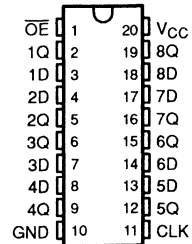
SN74LV374

OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

FEBRUARY 1993 – REVISED SEPTEMBER 1993

- **EPIC™** (Enhanced-Performance Implanted CMOS) 2- μ m Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (SOIC), Shrink Small-Outline (SSOP), and Thin Shrink Small-Outline (TSSOP) Packages

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal edge-triggered D-type flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV374 features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels that were set up at the data (D) inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components. The output-enable (\overline{OE}) input does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74LV374 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV374 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
\overline{OE}	CLK	D	Q
L	\uparrow	H	H
L	\uparrow	L	L
L	L	X	Q_0
H	X	X	Z

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PRODUCTION DATA Information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



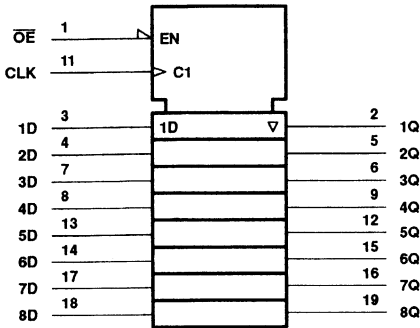
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SN74LV374

OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

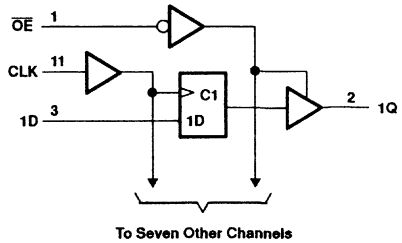
FEBRUARY 1993 – REVISED SEPTEMBER 1993

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 35 mA
Continuous current through V_{CC} or GND pins	± 70 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air):	
DB package	0.5 W
DW package	0.85 W
PW package	0.5 W
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.3	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		2	V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			-8	mA
I_{OL}	Low-level output current			8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		100	ns/V
T_A	Operating free-air temperature	-40		85	$^\circ\text{C}$

NOTE 3: Unused or floating inputs must be held high or low.



SN74LV374
OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP
WITH 3-STATE OUTPUTS

FEBRUARY 1993 – REVISED SEPTEMBER 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} †	MIN	TYP	MAX	UNIT
V _{OH}	I _{OH} = -100 µA	MIN to MAX	V _{CC} - 0.2		2.4	V
	I _{OH} = -8 mA	3 V				
V _{OL}	I _{OL} = 100 µA	MIN to MAX	0.2		0.4	V
	I _{OL} = 8 mA	3 V				
I _I	V _I = V _{CC} or GND	3.6 V	±1		µA	
I _{OZ}	V _O = V _{CC} or GND	3.6 V	±5		µA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V	20		µA	
ΔI _{CC}	V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC} or GND, One input at V _{CC} - 0.6 V,		500		µA	
C _i	V _I = V _{CC} or GND	3.3 V	2.5		pF	
C _o	V _O = V _{CC} or GND	3.3 V	7		pF	

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT
		MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	0	24	0	19	MHz
t _w	Pulse duration	CLK high or low		20	25	ns
t _{SU}	Setup time before CLK↑	High or low		13	16	ns
t _H	Hold time, data after CLK↑			5	5	ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		UNIT
			MIN	TYP	MAX	MIN	MAX	
t _{max}			24	75		19	MHz	
t _{pd}	CLK	Q		14	30		38	ns
t _{en}	\overline{OE}	Q		15	29		36	ns
t _{dis}	\overline{OE}	Q		15	29		36	ns

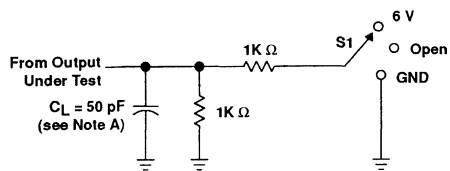
operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance per flip-flop	Outputs enabled	52	pF
		Outputs disabled	34	

SN74LV374 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

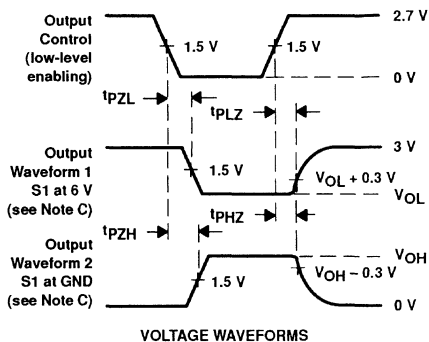
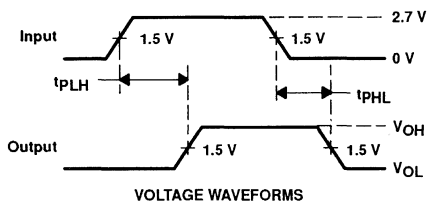
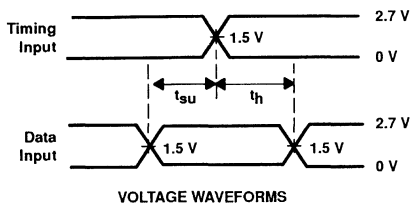
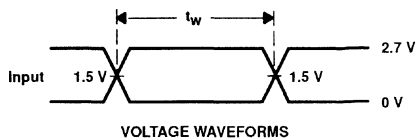
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PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



- NOTES:
- C_L includes probe and jig capacitance.
 - All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

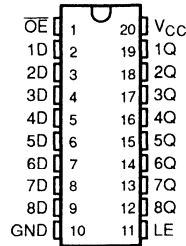
SN74LV573

OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

FEBRUARY 1993 – REVISED SEPTEMBER 1993

- **EPIC™ (Enhanced-Performance Implanted CMOS) 2- μ m Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (SOIC), Shrink Small-Outline (SSOP), and Thin Shrink Small-Outline (TSSOP) Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal transparent D-type latch is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV573 features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When the latch enable is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (\overline{OE}) input does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74LV573 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV573 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each latch)

INPUTS			OUTPUT
\overline{OE}	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

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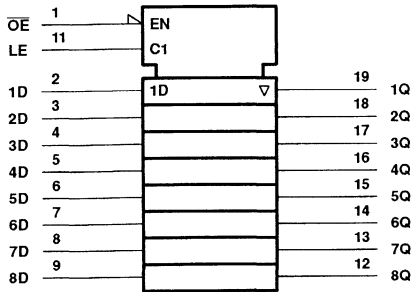
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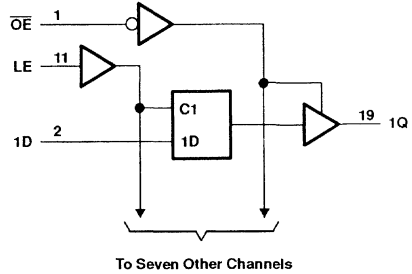
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SN74LV573
OCTAL TRANSPARENT D-TYPE LATCH
WITH 3-STATE OUTPUTS
 FEBRUARY 1993 – REVISED SEPTEMBER 1993

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 35 mA
Continuous current through V_{CC} or GND pins	± 70 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air):	
DB package	0.5 W
DW package	0.85 W
PW package	0.5 W
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.3	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		2	V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		0.8	V
V_I	Input voltage	0	V_{CC}		V
V_O	Output voltage	0	V_{CC}		V
I_{OH}	High-level output current			-8	mA
I_{OL}	Low-level output current			8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	100		ns/V
T_A	Operating free-air temperature	-40		85	$^\circ\text{C}$

NOTE 3: Unused or floating inputs must be held high or low.



SN74LV573
OCTAL TRANSPARENT D-TYPE LATCH
WITH 3-STATE OUTPUTS
 FEBRUARY 1993 – REVISED SEPTEMBER 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} †	MIN	TYP	MAX	UNIT
V _{OH}	I _{OH} = -100 µA	MIN to MAX	V _{CC} -0.2			V
	I _{OH} = -8 mA	3 V	2.4			
V _{OL}	I _{OL} = 100 µA	MIN to MAX	0.2			V
	I _{OL} = 8 mA	3 V	0.4			
I _I	V _I = V _{CC} or GND	3.6 V	±1			µA
I _{OZ}	V _O = V _{CC} or GND	3.6 V	±5			µA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V	20			µA
ΔI _{CC}	V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND		500			µA
C _i	V _I = V _{CC} or GND	3.3 V	2.5			pF
C _o	V _O = V _{CC} or GND	3.3 V	7			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	
t _w	Pulse duration	LE high	20		25		ns
t _{su}	Setup time before LE↓	Data	10		13		ns
t _h	Hold time, data after LE↓		8		8		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V	UNIT
			MIN	TYP	MAX	MAX	
t _{pd}	D	Q	11	29	36	ns	
	LE		15	30	38		
t _{en}	OE	Q	13	26	33	ns	
t _{dis}	OE	Q	15	32	39	ns	

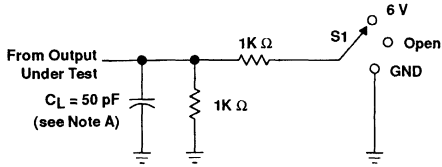
operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance per latch	Outputs enabled	30	pF
		Outputs disabled	14	

SN74LV573
OCTAL TRANSPARENT D-TYPE LATCH
WITH 3-STATE OUTPUTS

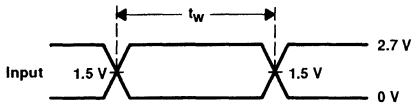
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PARAMETER MEASUREMENT INFORMATION

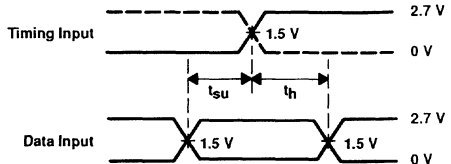


LOAD CIRCUIT FOR OUTPUTS

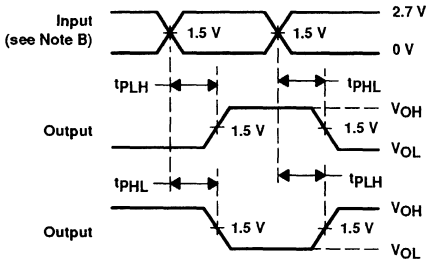
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



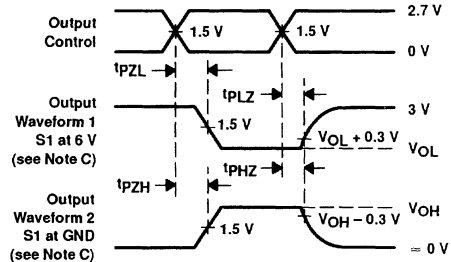
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

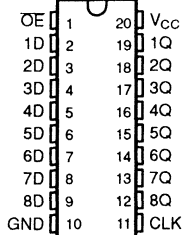
SN74LV574

OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

NOVEMBER 1993

- **Space-Saving Package Option:**
Shrink Small-Outline Package (DB)
Features EIAJ 0.65-mm Lead Pitch
- **EPIC™ (Enhanced-Performance Implanted CMOS) 2- μ m Process**
- **Typical V_{OLP} (Output Ground Bounce)**
< 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- **Typical V_{OHV} (Output V_{OH} Undershoot)**
> 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline and Thin Shrink Small-Outline Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal edge-triggered D-type flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV574 features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels that were set up at the data (D) inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (\overline{OE}) input does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74LV574 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV574 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
\overline{OE}	CLK	D	Q
L	\uparrow	H	H
L	\uparrow	L	L
L	L	X	Q_0
H	X	X	Z

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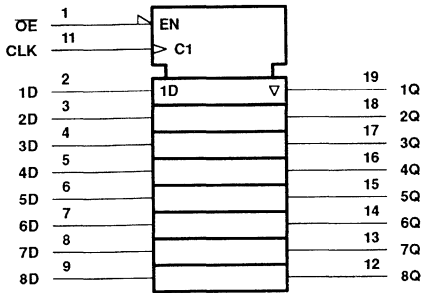


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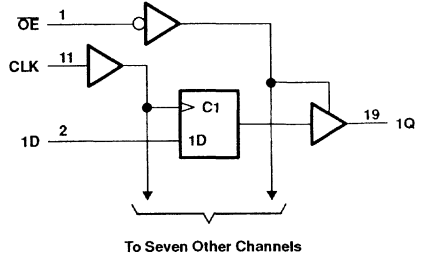
PRODUCT PREVIEW

SN74LV574
OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP
WITH 3-STATE OUTPUTS
 NOVEMBER 1993

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 35 mA
Continuous current through V_{CC} or GND pins	± 70 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air):	
DB package	0.5 W
DW package	0.85 W
PW package	0.5 W
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.3	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		2	V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			-8	mA
I_{OL}	Low-level output current			8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		100	ns/V
T_A	Operating free-air temperature	-40		85	$^\circ\text{C}$

NOTE 3: Unused or floating inputs must be held high or low.

PRODUCT PREVIEW

SN74LV574 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

NOVEMBER 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} [†]	MIN	TYP	MAX	UNIT
V _{OH}	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2			V
	I _{OH} = -6 mA	3 V	2.4			
V _{OL}	I _{OL} = 100 μA	MIN to MAX			0.2	V
	I _{OL} = 6 mA	3 V			0.4	
I _I	V _I = V _{CC} or GND	3.6 V			±1	μA
I _{OZ}	V _O = V _{CC} or GND	3.6 V			±5	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V			20	μA
ΔI _{CC}	V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND				500	μA
C _I	V _I = V _{CC} or GND	3.3 V			TBD	pF
C _O	V _O = V _{CC} or GND	3.3 V			TBD	pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT
		MIN	MAX	MIN	MAX	
t _{clock}	Clock frequency					MHz
t _w	Pulse duration	CLK high or low				ns
t _{su}	Setup time before CLK↑	High or low				ns
t _h	Hold time, data after CLK↑					ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		UNIT
			MIN	TYP	MAX	MIN	MAX	
f _{max}							MHz	
t _{pd}	CLK	Q					ns	
t _{en}	OE	Q					ns	
t _{dis}	OE	Q					ns	

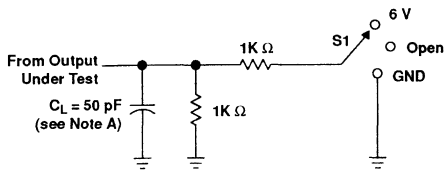
operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance per flip-flop	C _L = 50 pF, f = 10 MHz		pF
			Outputs enabled	
			Outputs disabled	

PRODUCT PREVIEW

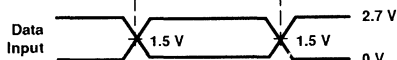
SN74LV574
OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP
WITH 3-STATE OUTPUTS
 NOVEMBER 1993

PARAMETER MEASUREMENT INFORMATION

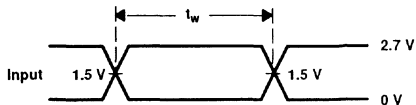


LOAD CIRCUIT

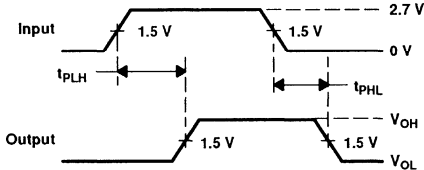
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



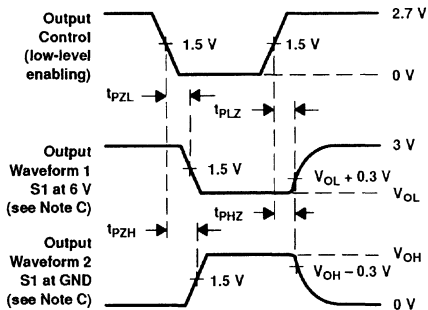
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

PRODUCT PREVIEW

- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

General Information	1
LVT Octals and Widebus™	2
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- Translates Between GTL Signal Levels and LVCMOS, LVTTTL, or 5-V TTL Signal Levels
- Member of the Texas Instruments *Widebus™* Family
- Supports Mixed-Mode Signal Operation on A Port (5-V Input and Output Voltages With 3.3-V V_{CC})
- State-of-the-Art BiCMOS Design for Low-Static Power Dissipation
- *UBT™* (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops With Qualified Storage Enable
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors on A Port
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Flow-Through Architecture Optimizes PCB Layout
- Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages

description

This 18-bit registered bus transceiver combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

The B port operates at GTL levels while the A port and control pins are compatible with LVCMOS, LVTTTL, or 5-V TTL logic levels.

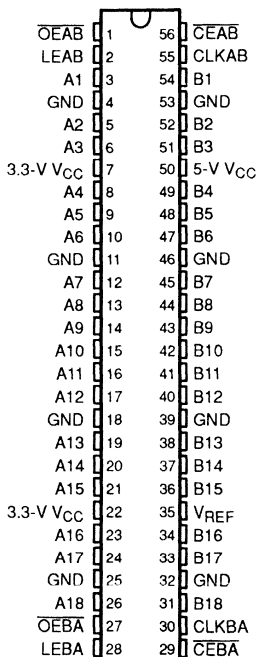
Data flow in each direction is controlled by output-enable (\overline{OEAB} and \overline{OEBA}), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock or latch-enable can be controlled by the chip-enable (\overline{CEAB} and \overline{CEBA}) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if \overline{CEAB} is low and CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB if \overline{CEAB} is also low. Output-enable \overline{OEAB} is active-low. When \overline{OEAB} is low, the outputs are active. When \overline{OEAB} is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that of A to B but uses \overline{OEBA} , LEBA, CLKBA, and \overline{CEBA} .

To ensure the high impedance state during power-up or power-down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT16611 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74LVT16611 is characterized for operation from 0°C to 70°C.

DGG OR DL PACKAGE
(TOP VIEW)



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SN74LVT16611 18-BIT GTL/LVT UNIVERSAL BUS TRANSCEIVER

MARCH 1993

FUNCTION TABLE

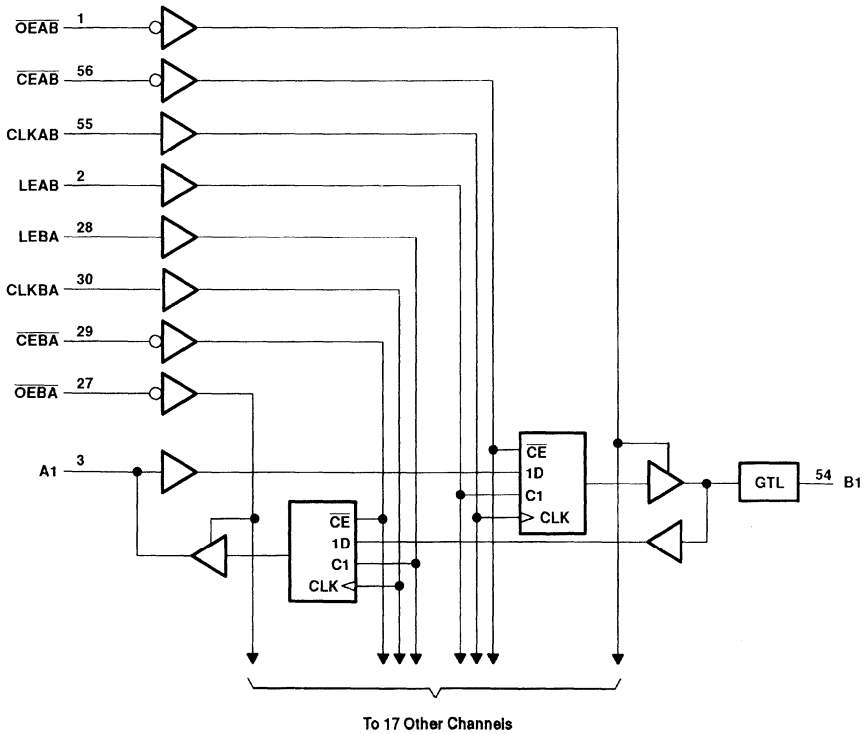
INPUTS					OUTPUT B	MODE
CEAB	OEAB	LEAB	CLKAB	A		
X	H	X	X	X	Z	Latched storage of A data
L	L	L	H	X	B ₀ [‡]	
L	L	L	L	X	B ₀ [§]	
X	L	H	X	L	L	Transparent
X	L	H	X	H	H	
L	L	L	↑	L	L	Clocked storage of A data
L	L	L	↑	H	H	
H	L	L	X	X	B ₀ [§]	Clock inhibit

† A-to-B data flow is shown: B-to-A data flow is similar but uses OEBA, LEBA, CLKBA, and CEBA.

‡ Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low.

§ Output level before the indicated steady-state input conditions were established.

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, 3.3-V V_{CC}	-0.5 V to 4.6 V
Supply voltage range, 5-V V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1)	-0.5 V to 7 V
Current into any A-port output in the low state, I_O	128 mA
Current into any B-port output in the low state, I_O	80 mA
Current into any A-port output in the high state, I_O (see Note 2)	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DGG package	1 W
DL package	1 W
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions

		MIN	NOM	MAX	UNIT	
V_{CC}	Supply voltage, 3.3 V	3.15	3.3	3.45	V	
	Supply voltage, 5 V	4.75	5	5.25		
V_{REF}	Supply voltage	0.8			V	
V_I	Input voltage	V_{CC}			V	
		Except B port				
V_{IH}	High-level input voltage	$V_{REF} + 50\text{ mV}$			V	
		2				
V_{IL}	Low-level input voltage	$V_{REF} - 50\text{ mV}$			V	
		0.8				
I_{IK}	Input clamp current	-18			mA	
I_{OH}	High-level output current	-32			mA	
		A port‡				
I_{OL}	Low-level output current	64			mA	
		B port				
T_A	Operating free air temperature	0			70	°C

‡ Current duty cycle $\leq 50\%$, $f \geq 1\text{ kHz}$

PRODUCT PREVIEW

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18-BIT GTL/LVT UNIVERSAL BUS TRANSCEIVER

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electrical characteristics over recommended operating free-air temperature range, $V_{REF} = 0.8\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT	
V_{IK}		$V_{CC} = 3.15\text{ V}$,	$I_I = -18\text{ mA}$			-1.2	V	
V_{OH}	A port	$V_{CC} = \text{MIN to MAX}^\ddagger$,	$I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC} - 0.2$			V	
		$V_{CC} = 3.15\text{ V}$	$I_{OH} = -8\text{ mA}$	2.4				
			$I_{OH} = -32\text{ mA}$	2				
V_{OL}	A port	$V_{CC} = 3.15\text{ V}$	$I_{OL} = -100\text{ }\mu\text{A}$			0.2	V	
			$I_{OL} = 16\text{ mA}$			0.4		
			$I_{OL} = 32\text{ mA}$			0.5		
			$I_{OL} = 64\text{ mA}$			0.55		
	B port	$V_{CC} = 3.15\text{ V}$,	$I_{OL} = 40\text{ mA}$			0.4		
I_I	Control pins	$V_{CC} = 0\text{ or MAX}^\ddagger$,	$V_I = 5.5\text{ V}$			10	μA	
	A port§	$V_{CC} = 3.45\text{ V}$	$V_I = 5.5\text{ V}$			20		
			$V_I = V_{CC}$			1		
			$V_I = 0$			-5		
B port	$V_{CC} = 3.45\text{ V}$	$V_I = V_{CC}$			5	μA		
		$V_I = 0$			-5			
I_{off}	A port	$V_{CC} = 0$	$V_I\text{ or }V_O = 0\text{ to }4.5\text{ V}$		100		μA	
	B port		$V_I\text{ or }V_O = 0\text{ to }1.2\text{ V}$		100			
$I_I(\text{hold})$	A port	$V_{CC} = 3.15\text{ V}$	$V_I = 0.8\text{ V}$		75		μA	
			$V_I = 2\text{ V}$		-75			
I_{OZH}	A port	$V_{CC} = 3.45\text{ V}$	$V_O = 3\text{ V}$		1		μA	
	B port		$V_O = 1.2\text{ V}$		10			
I_{OZL}	A port	$V_{CC} = 3.45\text{ V}$	$V_O = 0.5\text{ V}$		-1		μA	
	B port		$V_O = 0.4\text{ V}$		-10			
I_{CC}	A port to B port	$V_{CC} = 3.45\text{ V}$,	$V_I = V_{CC}\text{ or GND}$	$I_O = 0$,			mA	
	B port to A port							
	Outputs disabled							
ΔI_{CC}^\S		$V_{CC} = 3.45\text{ V}$,	One input at 2.7 V,				1	mA
C_i	Control pins	$V_I = 3.15\text{ V or }0$		4			pF	
C_{iO}	A port	$V_O = 3.15\text{ V or }0$		10			pF	
C_{iO}	B port	Per IEEE1194.0-1991		5			pF	

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ Unused pins at V_{CC} or GND

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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Timing requirements over recommended ranges of supply voltage and operating free-air temperature, $V_{REF} = 0.8\text{ V}$ (unless otherwise noted)

		MIN	MAX	UNIT
f_{clock}	Clock frequency	0	150	MHz
t_w	Pulse duration	LEAB or LEBA high		ns
		CLKAB or CLKBA high or low		
t_{su}	Setup time	A before CLKAB \uparrow	1.5	ns
		B before CLKAB \uparrow	3	
		A before LEAB \downarrow	0.5	
		B before LEBA \downarrow	1.5	
		\overline{CEAB} before CLKAB \uparrow		
		CEBA before CLKBA \uparrow		
		\overline{CEAB} before LEAB \downarrow		
		CEBA before LEBA \downarrow		
t_h	Hold time	A after CLKAB \uparrow	1	ns
		B after CLKAB \uparrow	0	
		A after LEAB \downarrow	2.5	
		B after LEBA \downarrow	2	
		\overline{CEAB} after CLKAB \uparrow		
		CEBA after CLKBA \uparrow		
		\overline{CEAB} after LEAB \downarrow		
		CEBA after LEBA \downarrow		

Switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $V_{REF} = 0.8\text{ V}$ (see Figure 1)

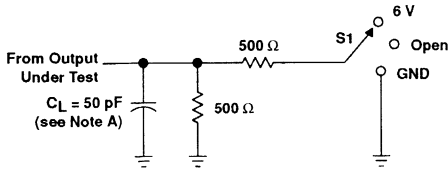
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT
f_{max}						MHz
t_{PLH}	A	B			3.2	ns
t_{PHL}					3.2	
t_{PLH}	LEAB	B			4	ns
t_{PHL}					4	
t_{PLH}	CLKAB	B			4.3	ns
t_{PHL}					4.3	
t_{PLH}	\overline{OEAB}	B			4.5	ns
t_{PHL}					4.5	
t_t	Transition time, B outputs (0.5 V to 1 V)			1.7		ns
t_t	Transition time, B outputs (1 V to 0.5 V)			0.6		ns
t_{PLH}	B	A			6.5	ns
t_{PHL}					6.5	
t_{PLH}	LEBA	A			6.3	ns
t_{PHL}					6.3	
t_{PLH}	CLKBA	A			6.3	ns
t_{PHL}					6.3	
t_{EN}	\overline{OEBA}	A			5.5	ns
t_{DIS}					6	

PRODUCT PREVIEW

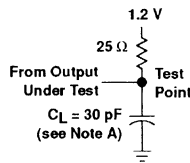
SN74LVT16611 18-BIT GTL/LVT UNIVERSAL BUS TRANSCEIVER

MARCH 1993

PARAMETER MEASUREMENT INFORMATION

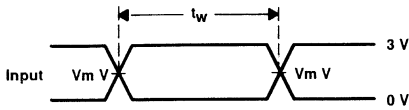


LOAD CIRCUIT FOR A OUTPUTS

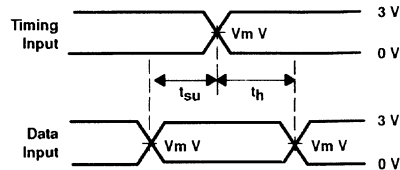


LOAD CIRCUIT FOR B OUTPUTS

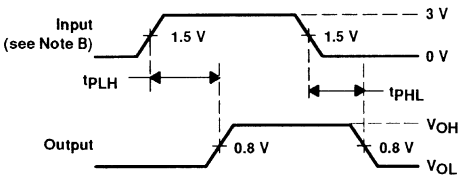
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{pLZ}/t_{pZL}	6 V
t_{PHZ}/t_{PZH}	GND



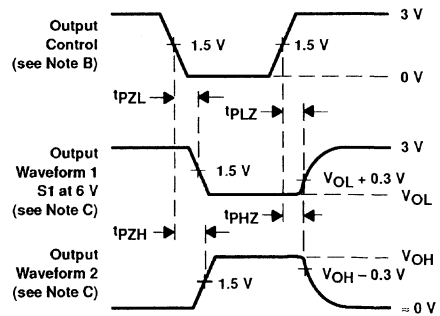
VOLTAGE WAVEFORMS
PULSE DURATION
($V_m = 1.5$ V for A port and 0.8 V for B port)



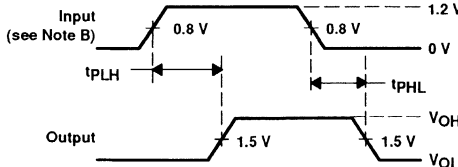
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
($V_m = 1.5$ V for A port and 0.8 V for B port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(A port to B port)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(A port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(B port to A port)

- NOTES:
- C_L includes probe and jig capacitance.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW



SN74LVT16615

17-BIT GTL/LVT UNIVERSAL BUS TRANSCEIVER WITH BUFFERED CLOCK OUTPUTS

MARCH 1993

- Translates Between GTL Signal Levels and LVCMOS, LVTTTL, or 5-V TTL Signal Levels
- Member of the Texas Instruments *Widebus™* Family
- Supports Mixed-Mode Signal Operation on A Port (5-V Input and Output Voltages With 3.3-V V_{CC})
- State-of-the-Art BiCMOS Design for Low-Static Power Dissipation
- *UBT™* (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops With Qualified Storage Enable
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors on A Port
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Flow-Through Architecture Optimizes PCB Layout
- Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages

description

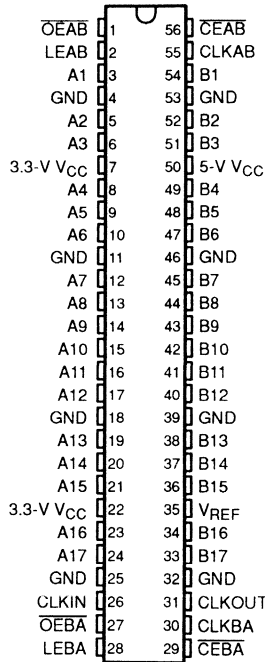
This 17-bit registered bus transceiver combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes. It provides for a copy of CLKAB at GTL logic levels (CLKOUT). It also provides a conversion of the GTL clock to a TTL environment (CLKIN).

The B port operates at GTL levels while the A port and control pins are compatible with LVCMOS, LVTTTL, or 5-V TTL logic levels.

Data flow in each direction is controlled by output-enable (\overline{OEAB} and \overline{OEBA}), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock or latch-enable can be controlled by the chip-enable (\overline{CEAB} and \overline{CEBA}) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if \overline{CEAB} is low and CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB if \overline{CEAB} is also low. Output-enable \overline{OEAB} is active-low. When \overline{OEAB} is low, the outputs are active. When \overline{OEAB} is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that of A to B but uses \overline{OEBA} , LEBA, CLKBA, and \overline{CEBA} .

To ensure the high-impedance state during power-up or power-down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

DGG OR DL PACKAGE
(TOP VIEW)



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SN74LVT16615
17-BIT GTL/LVT UNIVERSAL BUS TRANSCEIVER
WITH BUFFERED CLOCK OUTPUTS

MARCH 1993

description (continued)

The SN74LVT16615 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74LVT16615 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE†

INPUTS					OUTPUT B	MODE
CEAB	OEAB	LEAB	CLKAB	A		
X	H	X	X	X	Z	Latched storage of A data
L	L	L	H or L	X	B ₀ ‡	
L	L	L	H or L	X	B ₀ §	
X	L	H	X	L	L	Transparent
X	L	H	X	H	H	
L	L	L	↑	L	L	Clocked storage of A data
L	L	L	↑	H	H	
H	L	L	X	X	B ₀ §	Clock inhibit

† A-to-B data flow is shown. B-to-A data flow is similar but uses OEBA, LEBA, CLKB_A, and CEBA.

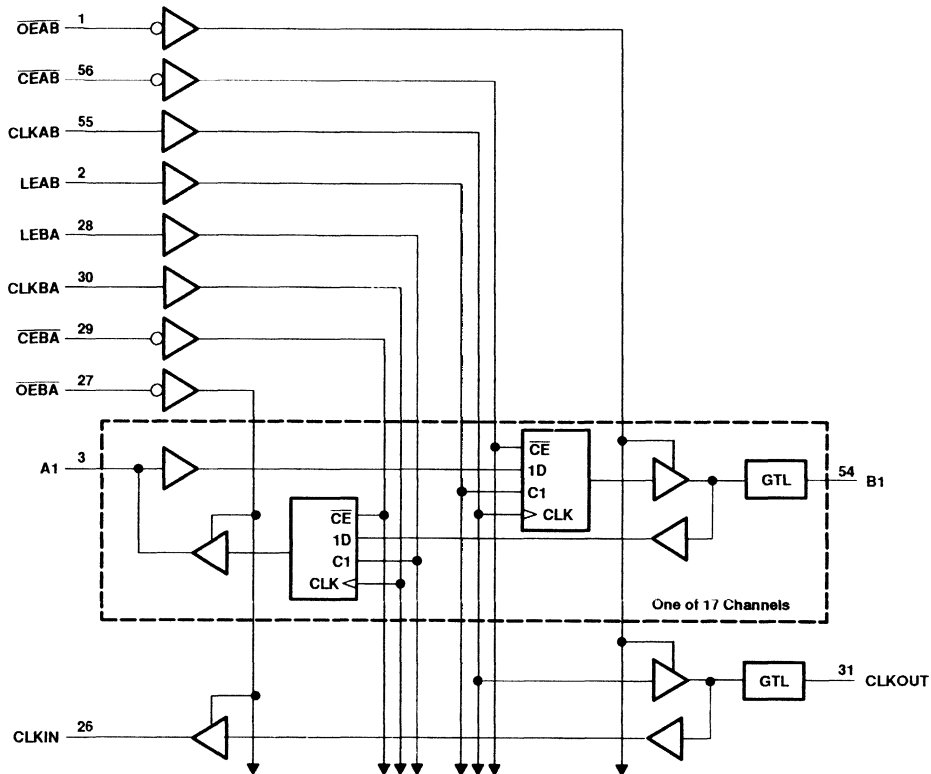
‡ Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low.

§ Output level before the indicated steady-state input conditions were established.

PRODUCT PREVIEW

SN74LVT16615
17-BIT GTL/LVT UNIVERSAL BUS TRANSCEIVER
WITH BUFFERED CLOCK OUTPUTS
MARCH 1993

logic diagram (positive logic)



PRODUCT PREVIEW

SN74LVT16615
17-BIT GTL/LVT UNIVERSAL BUS TRANSCEIVER
WITH BUFFERED CLOCK OUTPUTS

MARCH 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, 3.3 V, V_{CC}	-0.5 V to 4.6 V
Supply voltage range, 5 V, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1)	-0.5 V to 7 V
Current into any A-port output in the low state, I_{O}	128 mA
Current into any B-port output in the low state, I_{O}	80 mA
Current into any A-port output in the high state, I_{O} (see Note 2)	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DGG package	1 W
DL package	1 W
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage, 3.3 V	3.15	3.3	3.45	V
	Supply voltage, 5 V	4.75	5	5.25	
V_{REF}	Supply voltage	0.8			V
V_I	Input voltage	B port	V_{CC}		V
		Except B port	5.5		
V_{IH}	High-level input voltage	B port	$V_{REF} + 50\text{ mV}$		V
		Except B port	2		
V_{IL}	Low-level input voltage	B port	$V_{REF} - 50\text{ mV}$		V
		Except B port	0.8		
I_{IK}	Input clamp current				-18 mA
I_{OH}	High-level output current	A port			-32 mA
I_{OL}	Low-level output current	A port‡			64 mA
		B port			40 mA
T_A	Operating free-air temperature	0			70 °C

‡ Current duty cycle $\leq 50\%$, $f \geq 1\text{ kHz}$

PRODUCT PREVIEW



SN74LVT16615
17-BIT GTL/LVT UNIVERSAL BUS TRANSCEIVER
WITH BUFFERED CLOCK OUTPUTS

MARCH 1993

electrical characteristics over recommended operating free-air temperature range, $V_{REF} = 0.8\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		$V_{CC} = 3.15\text{ V}$,	$I_I = -18\text{ mA}$			-1.2	V
V_{OH}	A port	$V_{CC} = \text{MIN to MAX}^\ddagger$,	$I_{OH} = -100\ \mu\text{A}$	$V_{CC} - 0.2$			V
		$V_{CC} = 3.15\text{ V}$	$I_{OH} = -8\text{ mA}$	2.4			
			$I_{OH} = -32\text{ mA}$	2			
V_{OL}	A port	$V_{CC} = 3.15\text{ V}$	$I_{OL} = 100\ \mu\text{A}$		0.2	V	
			$I_{OL} = 16\text{ mA}$		0.4		
			$I_{OL} = 32\text{ mA}$		0.5		
			$I_{OL} = 64\text{ mA}$		0.55		
	B port	$V_{CC} = 3.15\text{ V}$,	$I_{OL} = 40\text{ mA}$		0.4		
I_I	Control pins	$V_{CC} = 0\text{ or MAX}^\ddagger$,	$V_I = 5.5\text{ V}$			10	μA
	A port§	$V_{CC} = 3.45\text{ V}$	$V_I = 5.5\text{ V}$		20	μA	
			$V_I = V_{CC}$		1		
			$V_I = 0$		-5		
	B port	$V_{CC} = 3.45\text{ V}$	$V_I = V_{CC}$		5	μA	
$V_I = 0$				-5			
I_{off}	A port	$V_{CC} = 0$	$V_I\text{ or }V_O = 0\text{ to }4.5\text{ V}$		100	μA	
	B port		$V_I\text{ or }V_O = 0\text{ to }1.2\text{ V}$		100		
$I_I(\text{hold})$	A port	$V_{CC} = 3.15\text{ V}$	$V_I = 0.8\text{ V}$		75	μA	
			$V_I = 2\text{ V}$		-75		
I_{OZH}	A port	$V_{CC} = 3.45\text{ V}$	$V_O = 3\text{ V}$		1	μA	
	B port		$V_O = 1.2\text{ V}$		10		
I_{OZL}	A port	$V_{CC} = 3.45\text{ V}$	$V_O = 0.5\text{ V}$		-1	μA	
	B port		$V_O = 0.4\text{ V}$		-10		
I_{CC}	A port to B port	$V_{CC} = 3.45\text{ V}$, $V_I = V_{CC}\text{ or GND}$	$I_O = 0$,				mA
	B port to A port						
	Outputs disabled						
ΔI_{CC}^\ddagger		$V_{CC} = 3.45\text{ V}$, A or control inputs at V_{CC} or GND	One input at 2.7 V ,			1	mA
C_i	Control pins	$V_I = 3.15\text{ V or }0$			4		pF
C_{iO}	A port	$V_O = 3.15\text{ V or }0$			10		pF
C_{iO}	B port	Per IEEE1194.0-1991			5		pF

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ Unused pins at V_{CC} or GND

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

SN74LVT16615
 17-BIT GTL/LVT UNIVERSAL BUS TRANSCEIVER
 WITH BUFFERED CLOCK OUTPUTS
 MARCH 1993

timing requirements over recommended ranges of supply voltage and operating free-air temperature, $V_{REF} = 0.8\text{ V}$ (unless otherwise noted)

		MIN	MAX	UNIT
f_{clock}	Clock frequency	0	150	MHz
t_w	Pulse duration	LEAB or LEBA high		ns
		CLKAB or CLKBA high or low		
t_{su}	Setup time	A before CLKAB \uparrow	1.5	ns
		B before CLKAB \uparrow	3	
		A before LEAB \downarrow	0.5	
		B before LEBA \downarrow	1.5	
		\overline{CEAB} before CLKAB \uparrow		
		\overline{CEBA} before CLKBA \uparrow		
		\overline{CEAB} before LEAB \downarrow		
		\overline{CEBA} before LEBA \downarrow		
t_h	Hold time	A after CLKAB \uparrow	1	ns
		B after CLKAB \uparrow	0	
		A after LEAB \downarrow	2.5	
		B after LEBA \downarrow	2	
		\overline{CEAB} after CLKAB \uparrow		
		\overline{CEBA} after CLKBA \uparrow		
		\overline{CEAB} after LEAB \downarrow		
		\overline{CEBA} after LEBA \downarrow		

PRODUCT PREVIEW

SN74LVT16615
17-BIT GTL/LVT UNIVERSAL BUS TRANSCEIVER
WITH BUFFERED CLOCK OUTPUTS

MARCH 1993

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $V_{REF} = 0.8\text{ V}$ (see Figure 1)

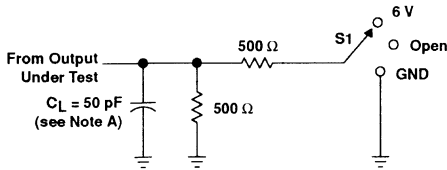
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT
t_{max}						MHz
t_{PLH}	A	B			3.2	ns
t_{PHL}					3.2	
t_{PLH}	LEAB	B			4	ns
t_{PHL}					4	
t_{PLH}	CLKAB	B			4.3	ns
t_{PHL}					4.3	
t_{PLH}	CLKAB	CLKOUT	2.3		6.5	ns
t_{PHL}					2.3	
t_{PLH}	OEAB	B			4.5	ns
t_{PHL}						
t_r	Transition time, B outputs (0.5 V to 1 V)				1.7	ns
t_f	Transition time, B outputs (1 V to 0.5 V)				0.6	ns
t_{PLH}	B	A			6.5	ns
t_{PHL}						
t_{PLH}	LEBA	A			6.3	ns
t_{PHL}						
t_{PLH}	CLKBA	A			6.3	ns
t_{PHL}						
t_{PLH}	CLKOUT	CLKIN	4		13.5	ns
t_{PHL}					4	
t_{en}	OE \bar{B} A	A			5.5	ns
t_{dis}						

PRODUCT PREVIEW

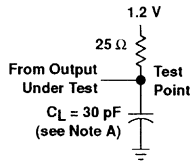
SN74LVT16615
17-BIT GTL/LVT UNIVERSAL BUS TRANSCEIVER
WITH BUFFERED CLOCK OUTPUTS

MARCH 1993

PARAMETER MEASUREMENT INFORMATION

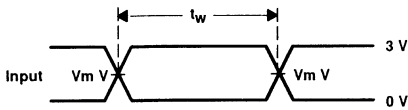


LOAD CIRCUIT FOR A OUTPUTS

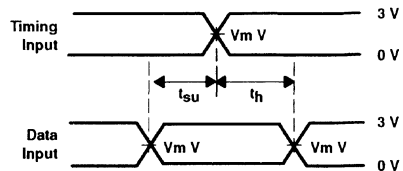


LOAD CIRCUIT FOR B OUTPUTS

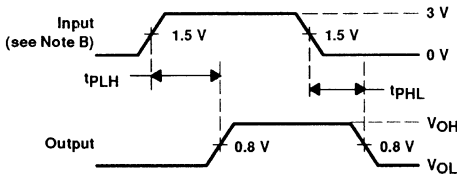
TEST	S1
t _{PLH} /t _{PHL}	Open
t _{PLZ} /t _{PZL}	6 V
t _{PHZ} /t _{PZH}	GND



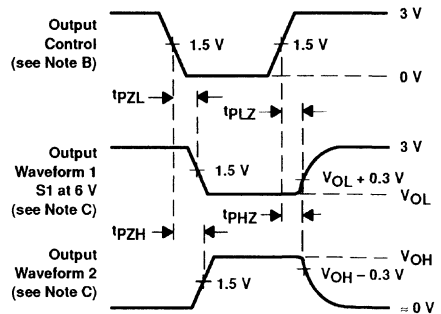
VOLTAGE WAVEFORMS
 PULSE DURATION
 (V_m = 1.5 V for A port and 0.8 V for B port)



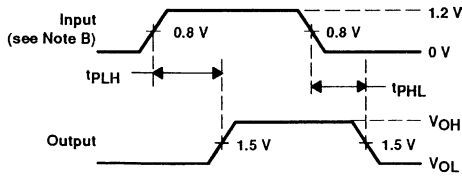
VOLTAGE WAVEFORMS
 SETUP AND HOLD TIMES
 (V_m = 1.5 V for A port and 0.8 V for B port)



VOLTAGE WAVEFORMS
 PROPAGATION DELAY TIMES
 (A port to B port)



VOLTAGE WAVEFORMS
 ENABLE AND DISABLE TIMES
 (A port)



VOLTAGE WAVEFORMS
 PROPAGATION DELAY TIMES
 (B port to A port)

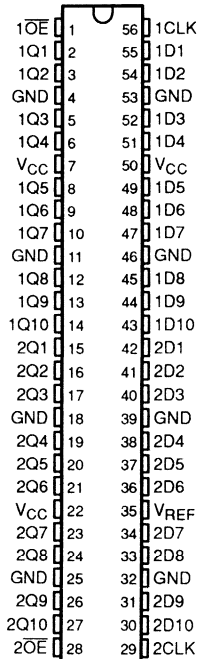
- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

- **EPIC-II B™** (Enhanced-Performance Implanted CMOS) Submicron Process
- Members of the Texas Instruments **Widebus™** Family
- Provides GTL Signals Levels on Both Inputs and Outputs
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages

DGG OR DL PACKAGE
(TOP VIEW)



description

The SN74GTL16821 has 20 single-bit flip-flops which are designed to provide terminated GTL logic levels.

The device can be used as two 10-bit flip-flops or one 20-bit flip-flop. The 20 flip-flops are edge-triggered D-type flip-flops. The SN74GTL16821 provides true data at the Q outputs on the positive transition of the clock (CLK) input.

The output-enable (\overline{OE}) input can be used to place the outputs in a high state. The output-enable input does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74GTL16821 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74GTL16821 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
\overline{OE}	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q ₀
H	X	X	Z

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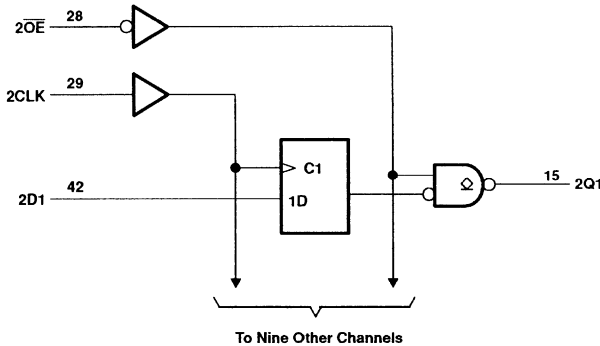
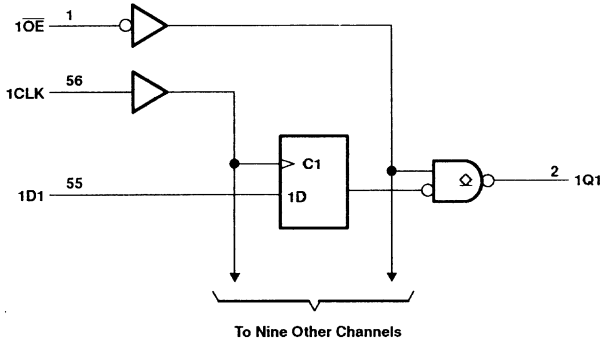


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PRODUCT PREVIEW

SN74GTL16821
20-BIT FLIP-FLOP
WITH GTL I/O LEVELS
 JULY 1993

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 4.6 V
Current into any output in the low state, I_O	80 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > 0$)	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DGG package	1 W
DL package	1 W
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.



recommended operating conditions

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage		3	3.6	V
V _{REF}	Supply voltage	2/3 V _{CC} - 2%	0.8	2/3 V _{CC} + 2%	V
V _I	Input voltage		0	V _{CC}	V
V _{OH}	High-level output voltage			3.6	V
V _{IH}	High-level input voltage		V _{REF} + 50 mV		V
V _{IL}	Low-level input voltage			V _{REF} - 50 mV	V
I _{IK}	Input clamp current			-18	mA
I _{OL}	Low-level output current			40	mA
T _A	Operating free-air temperature		0	70	°C

electrical characteristics over recommended operating free-air temperature range, V_{REF} = 0.8 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V _{IK}		V _{CC} = 3 V,	I _I = -18 mA			-1.2	V
V _{OL}		V _{CC} = 3 V,	I _{OL} = 40 mA			0.4	V
I _I		V _{CC} = 3 V	V _I = V _{CC}			5	μA
			V _I = 0			-5	
I _{OH}		V _{CC} = 3 V,	V _{OH} = 3.6 V				μA
I _{CC}	Outputs high	V _{CC} = 3 V, V _I = V _{CC} or GND	I _O = 0,				mA
	Outputs low						
C _i		Per IEEE1194.0-1991				4	pF
C _o		Per IEEE1194.0-1991				6	pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PRODUCT PREVIEW

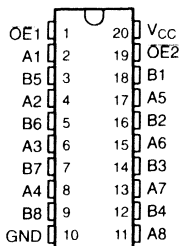
General Information	1
LVT Octals and Widebus™	2
LVC MSI, Octals and Widebus™	3
ALVC Widebus™	4
LV MSI and Octals	5
GTL Widebus™	6
CBT Bus Switches and 5-V/3-V Volt. Translators	7
Application Notes	8
LVT Characterization Information	9
Mechanical Data	10

SN74CBT3244 8-BIT CROSSBAR SWITCH

NOVEMBER 1992 – REVISED MARCH 1993

- **Space-Saving Package Option:**
Shrink Small-Outline Package (DB)
Features EIAJ 0.65-mm Lead Pitch
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input and Output Levels**
- **Standard '244-Type Pinout**
- **Package Options Include Plastic DIP Packages and Small-Outline and Thin Shrink Small-Outline Packages**

DW, DB, OR PW PACKAGE
(TOP VIEW)



description

The SN74CBT3244 provides 8 bits of high-speed TTL-compatible bus switching in a standard '244 device pinout. The low on resistance of the switch allows connections to be made without adding propagation delay.

The device is organized as two 4-bit switches with separate output-enable (OE) inputs. When OE is low, the switch is on and port A is connected to port B. When OE is high, the switch is open and a high-impedance state exists between the two ports.

The SN74CBT3244 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74CBT3244 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

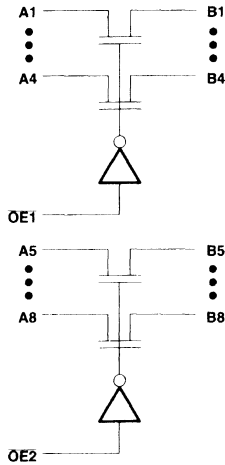
OE1	OE2	B1 – B4	B5 – B8	FUNCTION
L	L	A1 – A4	A5 – A8	Connect
L	H	A1 – A4	Z	Connect
H	L	Z	A5 – A8	Connect
H	H	Z	Z	Disconnect

PRODUCT PREVIEW

SN74CBT3244 8-BIT CROSSBAR SWITCH

NOVEMBER 1992 – REVISED MARCH 1993

function diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Current into any pin, I_O	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air):	
DB	0.5 W
DW	0.85 W
N	1.3 W
PW	0.5 W
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
T_A	Operating free-air temperature	-40	85	°C

SN74CBT3244 8-BIT CROSSBAR SWITCH

NOVEMBER 1992 – REVISED MARCH 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	$V_{CC} = 4.5 \text{ V}$,	$I_I = -18 \text{ mA}$				-1.2	V
I_I	$V_{CC} = 0$,	$V_I = 5.5 \text{ V}$				10	μA
	$V_{CC} = 5.5 \text{ V}$,	$V_I = 5.5 \text{ V or GND}$				± 1	
I_{OS}	$V_{CC} = 4.5 \text{ V}$,	$V_I(A) = 0$,	$V_I(B) = 4.5 \text{ V}$	100			mA
I_{CC}	$V_{CC} = 5.5 \text{ V}$,	$I_O = 0$, $V_I = V_{CC} \text{ or GND}$				1	mA
ΔI_{CC}^\ddagger	$V_{CC} = 3.6 \text{ V}$,	One input at 2.7 V,	Other inputs at V_{CC} or GND			0.2	mA
C_i Control pins	$V_I = 3 \text{ V or 0}$				4		pF
$C_{io(ON)}$	$V_O = 3 \text{ V or 0}$,	$\text{OE} = \text{GND}$			8		pF
$C_{io(OFF)}$	$V_O = 3 \text{ V or 0}$,	$\text{OE} = V_{CC}$			6		pF
r_{on}^\S	$V_{CC} = 4.5 \text{ V}$,	$V_I = 0$,	$I_I = 64 \text{ mA}$			6	Ω
	$V_{CC} = 4.5 \text{ V}$,	$V_I = 2.4 \text{ V}$,	$I_I = 15 \text{ mA}$			12	

† All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B pin at the indicated current through the switch. On resistance is determined by the lower of the voltages of the two (A or B) pins.

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = -40^\circ \text{ to } 85^\circ\text{C}$			$T_A = 0^\circ \text{ to } 70^\circ\text{C}$			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}^\P	A or B	B or A					0.25	ns	
t_{PHL}^\P						0.25			
t_{PZH}	OE	A or B				1.5	7.5	ns	
t_{PZL}						1.5	7.5		
t_{PHZ}	OE	Y				1.5	6.5	ns	
t_{PLZ}						1.5	6.5		

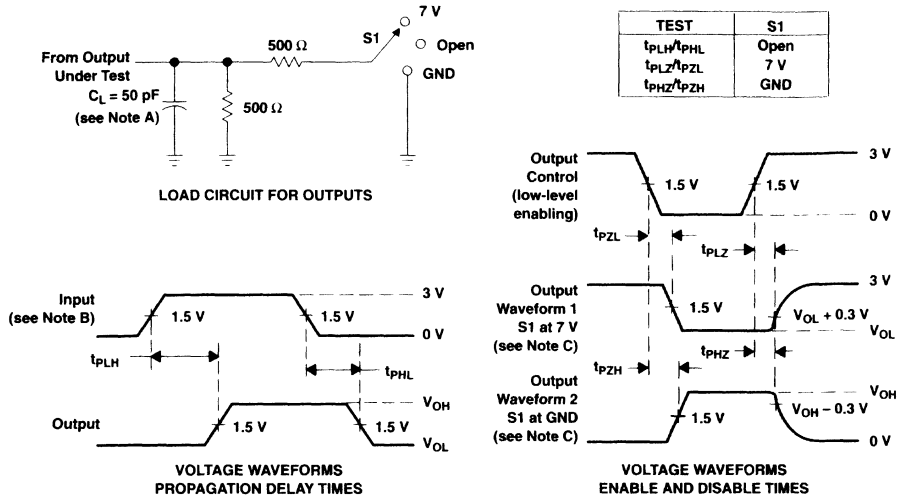
¶ This parameter is characterized but not tested. This propagation delay is due to the RC delay of the on resistance of the switch and the load capacitance.

PRODUCT PREVIEW

SN74CBT3244 8-BIT CROSSBAR SWITCH

NOVEMBER 1992 – REVISED MARCH 1993

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

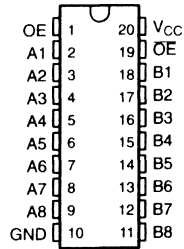
PRODUCT PREVIEW

SN74CBT3245 8-BIT CROSSBAR SWITCH

NOVEMBER 1992

- 5- Ω Switch Connection Between Two Ports
- TTL-Compatible Input and Output Levels
- Standard '245-Type Pinout
- Package Options Include Plastic DIP Packages and Small-Outline and Thin Shrink Small-Outline Packages

DW, DB, OR PW PACKAGE
(TOP VIEW)



description

The SN74CBT3245 provides 8 bits of high-speed TTL-compatible bus switching in a standard '245 device pinout. The low on resistance of the switch allows connections to be made without adding propagation delay.

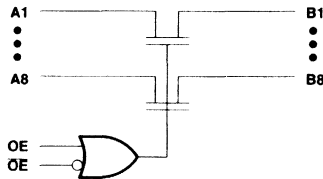
The device is organized as one 8-bit switch bank with dual output-enable (OE and $\overline{\text{OE}}$) inputs. When $\overline{\text{OE}}$ is low or OE is high, the switch is on and port A is connected to port B. When $\overline{\text{OE}}$ is high and OE is low, the switch is open and a high-impedance state exists between the two ports.

The SN74CBT3245 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

OE	$\overline{\text{OE}}$	B1-B8	FUNCTION
X	L	A1-A8	Connect
H	X	A1-A8	Connect
L	H	Z	Disconnect

function diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	$-0.5\text{ V to }7\text{ V}$	
Input voltage range, V_{I} (see Note 1)	$-0.5\text{ V to }7\text{ V}$	
Current into any pin, I_{O}	128 mA	
Input clamp current, $I_{\text{IK}} (V_{\text{I}} < 0)$	-50 mA	
Maximum power dissipation at $T_{\text{A}} = 55^{\circ}\text{C}$ (in still air):	DW	0.85 W
	N	1.3 W
	PW	0.5 W
Storage temperature range	$-65^{\circ}\text{C to }150^{\circ}\text{C}$	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

SN74CBT3245

8-BIT CROSSBAR SWITCH

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recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
T_A	Operating free-air temperature	-40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP [†]	MAX	UNIT
V_{IK}	$V_{CC} = 4.5$ V,	$I_I = -18$ mA			-1.2	V
I_I	$V_{CC} = 0$,	$V_I = 5.5$ V			10	μ A
	$V_{CC} = 5.5$ V,	$V_I = 5.5$ V or GND			± 1	
I_{OS}	$V_{CC} = 4.5$ V,	$V_I(A) = 0$,	$V_I(B) = 4.5$ V	100		mA
I_{CC}	$V_{CC} = 5.5$ V,	$I_O = 0$,	$V_I = V_{CC}$ or GND		1	mA
ΔI_{CC}^{\ddagger}	$V_{CC} = 3.6$ V,	One input at 2.7 V,	Other inputs at V_{CC} or GND		0.2	mA
C_i	Control pins	$V_I = 3$ V or 0			4	pF
$C_{iO(ON)}$		$V_O = 3$ V or 0,	$OE = GND$		8	pF
$C_{iO(OFF)}$		$V_O = 3$ V or 0,	$OE = V_{CC}$		6	pF
r_{on}^{\S}	$V_{CC} = 4.5$ V,	$V_I = 0$,	$I_I = 64$ mA		6	Ω
	$V_{CC} = 4.5$ V,	$V_I = 2.4$ V,	$I_I = 15$ mA		12	

[†] All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

[‡] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

[§] Measured by the voltage drop between the A and B pin at the indicated current through the switch. On resistance is determined by the lower of the voltages of the two (A or B) pins.

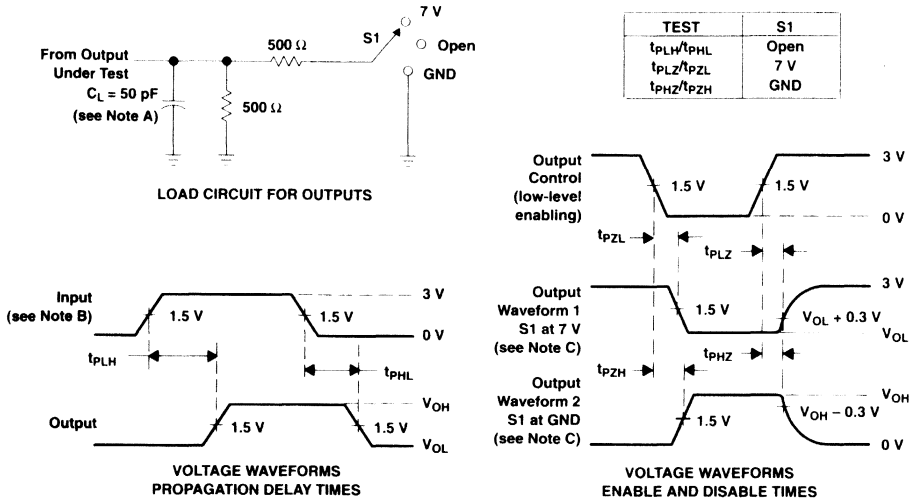
switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = -40^\circ$ to 85°C			$T_A = 0^\circ$ to 70°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}^{\parallel}	A or B	B or A						0.25	ns
t_{PHL}^{\parallel}							0.25		
t_{PZH}	OE or OE	A or B				1.5	7.5	ns	
t_{PZL}			1.5	7.5					
t_{PHZ}	OE or OE	Y				1.5	6.5	ns	
t_{PLZ}			1.5	6.5					

^{||} This parameter is characterized but not tested. This propagation delay is due to the RC delay of the on resistance of the switch and the load capacitance.

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one transition per measurement.

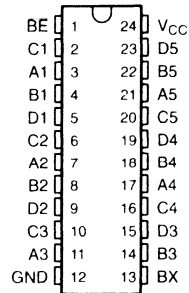
Figure 1. Load Circuit and Voltage Waveforms

SN74CBT3383 10-BIT BUS-EXCHANGE SWITCH

NOVEMBER 1992 - REVISED MARCH 1993

- **Space-Saving Package Option:
Shrink Small-Outline Package (DB)
Features EIAJ 0.65-mm Lead Pitch**
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input and Output Levels**
- **Package Options Include Plastic DIP
Packages and Small-Outline and Thin
Shrink Small-Outline Packages**

**DW, DB, OR PW PACKAGE
(TOP VIEW)**



description

The SN74CBT3383 provides 10 bits of high-speed TTL-compatible bus switching or exchanging. The low on resistance of the switch allows connections to be made without adding propagation delay.

The device operates as a 10-bit bus switch or a 5-bit bus exchanger, which provides swapping of the AB and CD pairs of signals. The bus-exchange function is selected when BX is high. The switches are connected when BE is low.

The SN74CBT3383 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74CBT3383 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

BE	BX	A1 - A5	B1 - B5	FUNCTION
L	L	C1 - C5	D1 - D5	Connect
L	H	D1 - D5	C1 - C5	Exchange
H	X	Z	Z	Disconnect

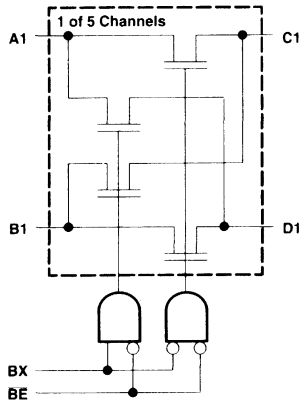
PRODUCT PREVIEW

SN74CBT3383

10-BIT BUS-EXCHANGE SWITCH

NOVEMBER 1992 – REVISED MARCH 1993

function diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Current into any pin, I_O	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air):	DB	0.5 W
	DW	0.85 W
	NT	1.3 W
	PW	0.5 W
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
T_A	Operating free-air temperature	-40	85	°C

PRODUCT PREVIEW

SN74CBT3383 10-BIT BUS-EXCHANGE SWITCH

NOVEMBER 1992 – REVISED MARCH 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	$V_{CC} = 4.5\text{ V}$,	$I_I = -18\text{ mA}$				-1.2	V
I_I	$V_{CC} = 0$,	$V_I = 5.5\text{ V}$				10	μA
	$V_{CC} = 5.5\text{ V}$,	$V_I = 5.5\text{ V or GND}$				± 1	
I_{OS}	$V_{CC} = 4.5\text{ V}$,	$V_I(A) = 0$,	$V_I(B) = 4.5\text{ V}$	100			mA
I_{CC}	$V_{CC} = 5.5\text{ V}$,	$I_O = 0$,	$V_I = V_{CC}\text{ or GND}$			1	mA
ΔI_{CC}^\ddagger	$V_{CC} = 3.6\text{ V}$,	One input at 2.7 V,	Other inputs at $V_{CC}\text{ or GND}$			0.2	mA
C_i	Control pins	$V_I = 3\text{ V or 0}$			4		pF
$C_{i(O)N}$	$V_O = 3\text{ V or 0}$,	$OE = \text{GND}$			8		pF
$C_{i(O)F}$	$V_O = 3\text{ V or 0}$,	$OE = V_{CC}$			6		pF
r_{on}^\S	$V_{CC} = 4.5\text{ V}$,	$V_I = 0$,	$I_I = 64\text{ mA}$			6	Ω
	$V_{CC} = 4.5\text{ V}$,	$V_I = 2.4\text{ V}$,	$I_I = 15\text{ mA}$			12	

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B pin at the indicated current through the switch. On resistance is determined by the lower of the voltages of the two (A or B) pins.

switching characteristics over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = -40^\circ\text{ to }85^\circ\text{C}$			$T_A = 0^\circ\text{ to }70^\circ\text{C}$			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}^\parallel	A or B	B or A						0.25	ns
t_{PHL}^\parallel								0.25	
t_{PLH}	BX	A or B				1.5	7.5	ns	
t_{PHL}						1.5	7.5		
t_{PZH}	BE	A or B				1.5	7.5	ns	
t_{PZL}						1.5	7.5		
t_{PHZ}	BE	Y				1.5	6.5	ns	
t_{PLZ}						1.5	6.5		

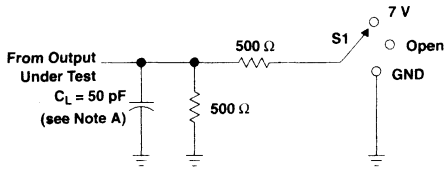
¶ This parameter is characterized but not tested. This propagation delay is due to the RC delay of the on resistance of the switch and the load capacitance.

PRODUCT PREVIEW

SN74CBT3383 10-BIT BUS-EXCHANGE SWITCH

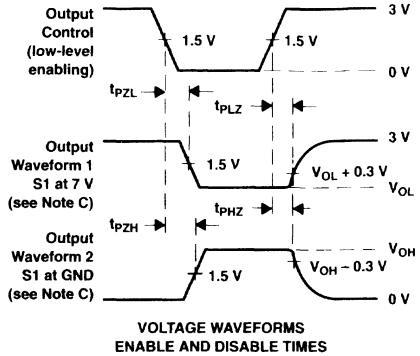
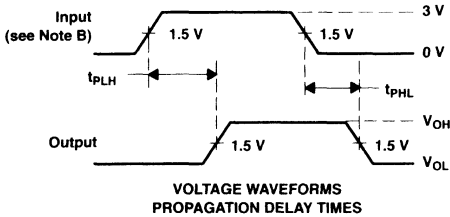
NOVEMBER 1992 – REVISED MARCH 1993

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR OUTPUTS

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	GND



NOTES: A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

SN74CBT3384 10-BIT CROSSBAR SWITCH

NOVEMBER 1992 – REVISED MARCH 1993

- **Space-Saving Package Option:
Shrink Small-Outline Package (DB)
Features EIAJ 0.65-mm Lead Pitch**
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input and Output Levels**
- **Package Options Include Plastic DIP
Packages and Small-Outline and Thin
Shrink Small-Outline Packages**

description

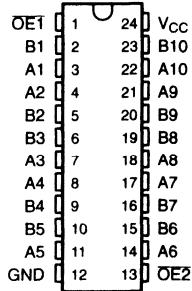
The SN74CBT3384 provides 10 bits of high-speed TTL-compatible bus switching. The low on resistance of the switch allows connections to be made without adding propagation delay.

The device is organized as two 5-bit switches with separate output-enable (OE) inputs. When OE is low, the switch is on and port A is connected to port B. When OE is high, the switch is open and a high-impedance state exists between the two ports.

The SN74CBT3384 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74CBT3384 is characterized for operation from -40°C to 85°C.

**DW, DB, OR PW PACKAGE
(TOP VIEW)**



FUNCTION TABLE

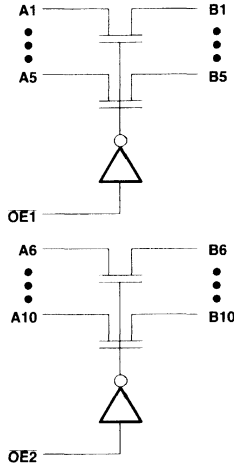
OE1	OE2	B1-B5	B6-B10	FUNCTION
L	L	A1-A5	A6-A10	Connect
L	H	A1-A5	Z	Connect
H	L	Z	A6-A10	Connect
H	H	Z	Z	Disconnect

PRODUCT PREVIEW

SN74CBT3384 10-BIT CROSSBAR SWITCH

NOVEMBER 1992 – REVISED MARCH 1993

function diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Current into any pin, I_O	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air):		
DB	0.5 W
DW	0.85 W
NT	1.3 W
PW	0.5 W
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
T_A	Operating free-air temperature	-40	85	°C

PRODUCT PREVIEW

SN74CBT3384 10-BIT CROSSBAR SWITCH

NOVEMBER 1992 – REVISED MARCH 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	$V_{CC} = 4.5\text{ V}$,	$I_I = -18\text{ mA}$				-1.2	V
I_I	$V_{CC} = 0$,	$V_I = 5.5\text{ V}$				10	μA
	$V_{CC} = 5.5\text{ V}$,	$V_I = 5.5\text{ V or GND}$				± 1	
I_{OS}	$V_{CC} = 4.5\text{ V}$,	$V_I(A) = 0$,	$V_I(B) = 4.5\text{ V}$	100			mA
I_{CC}	$V_{CC} = 5.5\text{ V}$,	$I_O = 0$,	$V_I = V_{CC}\text{ or GND}$			1	mA
ΔI_{CC}^\ddagger	$V_{CC} = 3.6\text{ V}$,	One input at 2.7 V,	Other inputs at V_{CC} or GND			0.2	mA
C_i	Control pins	$V_I = 3\text{ V or 0}$				4	pF
$C_{i(ON)}$	$V_O = 3\text{ V or 0}$,	$OE = \text{GND}$				8	pF
$C_{i(OFF)}$	$V_O = 3\text{ V or 0}$,	$OE = V_{CC}$				6	pF
r_{on}^\S	$V_{CC} = 4.5\text{ V}$,	$V_I = 0$,	$I_I = 64\text{ mA}$			6	Ω
	$V_{CC} = 4.5\text{ V}$,	$V_I = 2.4\text{ V}$,	$I_I = 15\text{ mA}$			12	

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B pin at the indicated current through the switch. On resistance is determined by the lower of the voltages of the two (A or B) pins.

switching characteristics over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = -40^\circ\text{ to }85^\circ\text{C}$			$T_A = 0^\circ\text{ to }70^\circ\text{C}$			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}^\parallel	A or B	B or A						0.25	ns
t_{PHL}^\parallel								0.25	
t_{PZH}	OE	A or B				1.5	7.5	ns	
t_{PZL}						1.5	7.5		
t_{PHZ}	OE	Y				1.5	6.5	ns	
t_{PLZ}						1.5	6.5		

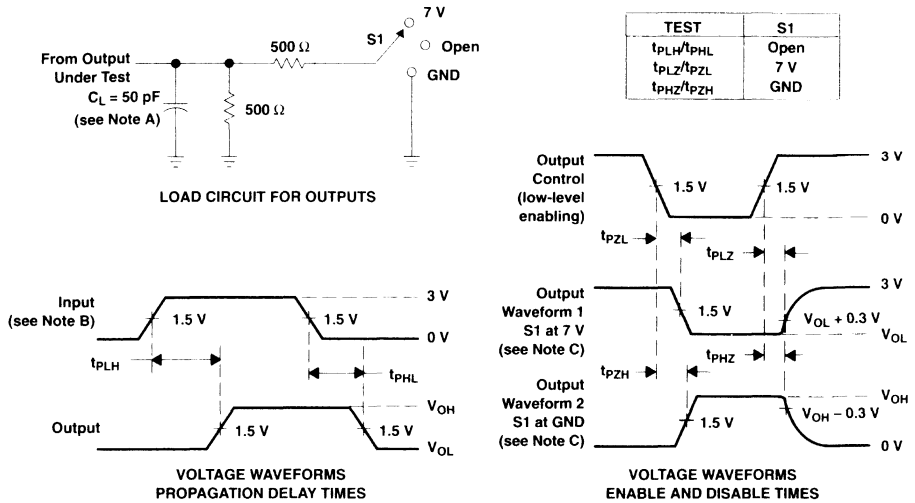
¶ This parameter is characterized but not tested. This propagation delay is due to the RC delay of the on resistance of the switch and the load capacitance.

PRODUCT PREVIEW

SN74CBT3384 10-BIT CROSSBAR SWITCH

NOVEMBER 1992 – REVISED MARCH 1993

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_0 = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

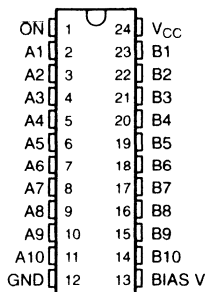
PRODUCT PREVIEW

SN74CBT6800 10-BIT CROSSBAR SWITCH WITH PRECHARGED OUTPUTS FOR LIVE INSERTION

MARCH 1993

- 5- Ω Switch Connection Between Two Ports
- TTL-Compatible Input and Output Levels
- Outputs Precharge Voltage to Minimize Signal Distortion During Live Insertion
- Package Options Include Plastic DIP Packages and Small-Outline and Thin Shrink Small-Outline Packages

DW, DB, OR PW PACKAGE
(TOP VIEW)



description

The SN74CBT6800 provides 10 bits of high-speed TTL-compatible bus switches. The low on resistance of the switch allows connections to be made without adding propagation delay. The device also precharges the B port to a user-selectable BIAS V to minimize live-insertion noise.

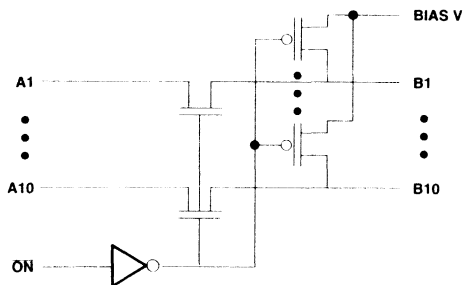
The SN74CBT6800 is organized as one 10-bit switch bank with a single enable (\overline{ON}) input. When \overline{ON} is low the switch is on and port A is connected to port B. When \overline{ON} is high the switch between port A and port B is open and the B port is precharged to the BIAS V voltage through the equivalent of a 10-k Ω resistor.

The SN74CBT6800 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

ON	B1-B8	FUNCTION
L	A1-A8	Connect
H	BIAS V	Precharge

function diagram



PRODUCT PREVIEW

SN74CBT6800
10-BIT CROSSBAR SWITCH
WITH PRECHARGED OUTPUTS FOR LIVE INSERTION
 MARCH 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	-0.5 V to 7 V
Bias voltage range, BIAS V	-0.5 V to V_{CC} V
Input voltage range, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Current into any pin, I_O	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DW	0.85 W
NT	1.3 W
PW	0.5 W
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
BIAS V	Supply voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
T_A	Operating free-air temperature	-40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP [‡]	MAX	UNIT
V_{IK}	$V_{CC} = 4.5$ V,	$I_I = -18$ mA				-1.2	V
I_I	$V_{CC} = 0$,	$V_I = 5.5$ V				10	μA
	$V_{CC} = 5.5$ V,	$V_I = 5.5$ V or GND				+1	
I_O	$V_{CC} = 4.5$ V,	BIAS V = 2.4 V,	$V_O = 0$	0.25			mA
I_{OS}	$V_{CC} = 4.5$ V,	$V_I(A) = 0$,	$V_I(B) = 4.5$ V	100			mA
I_{CC}	$V_{CC} = 5.5$ V,	$I_O = 0$,	$V_I = V_{CC}$ or GND			1	mA
ΔI_{CC} [§]	$V_{CC} = 3.6$ V,	One input at 2.7 V,	Other inputs at V_{CC} or GND			0.2	mA
C_i	Control pins	$V_I = 3$ V or 0			4		pF
$C_{iO(ON)}$		$V_O = 3$ V or 0,	OE = GND		8		pF
$C_{iO(OFF)}$		$V_O = 3$ V or 0,	OE = V_{CC}		6		pF
t_{on}	$V_{CC} = 4.5$ V,	$V_I = 0$,	$I_I = 64$ mA		6		Ω
	$V_{CC} = 4.5$ V,	$V_I = 2.4$ V,	$I_I = 15$ mA		12		
I_O	$V_{CC} = 4.5$ V,	BIAS V = 2.4 V,	$V_O = 0$	0.25			mA

[‡] All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

^{||} Measured by the voltage drop between the A and B pin at the indicated current through the switch. On resistance is determined by the lower of the voltages of the two (A or B) pins.

PRODUCT PREVIEW

SN74CBT6800
10-BIT CROSSBAR SWITCH
WITH PRECHARGED OUTPUTS FOR LIVE INSERTION
MARCH 1993

switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

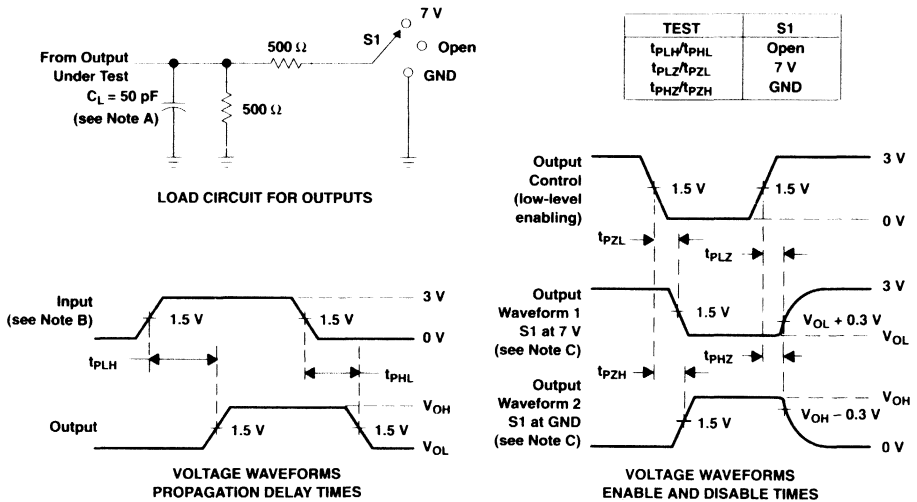
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = -40^\circ$ to 85°C			$T_A = 0^\circ$ to 70°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}^\dagger	A or B	B or A						0.25	ns
t_{PHL}^\dagger								0.25	
t_{PZH}^\ddagger	ON	A or B				1.5		7.5	ns
t_{PZL}^\S						1.5		7.5	
t_{PHZ}^\ddagger	ON	A or B				1.5		6.5	ns
t_{PLZ}^\S						1.5		6.5	

[†] This parameter is characterized but not tested. This propagation delay is due to the RC delay of the on resistance of the switch and the load capacitance.

[‡] BIAS V = GND

[§] BIAS V = 3 V

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SN74CBT16209 18-BIT BUS-EXCHANGE SWITCH

NOVEMBER 1992 – REVISED FEBRUARY 1993

- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input and Output Levels
- Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages

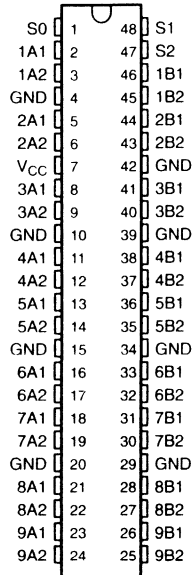
description

The SN74CBT16209 provides 18 bits of high-speed TTL-compatible bus switching or exchanging. The low on resistance of the switch allows connections to be made without adding propagation delay.

The device operates as an 18-bit bus switch or a 9-bit bus exchanger, which provides data exchanging between the four signal ports via the data-select pins (S0–S2).

The SN74CBT16209 is characterized for operation from –40°C to 85°C.

DGG OR DL PACKAGE
(TOP VIEW)



FUNCTION TABLE

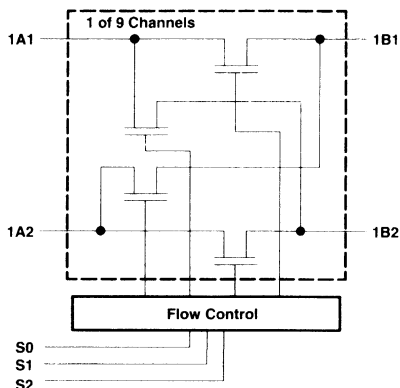
S0	S1	S2	A1	A2	FUNCTION
L	L	L	Z	Z	Disconnect
H	L	L	B1	Z	A1 and B1
L	H	L	B2	Z	A1 and B2
H	H	L	Z	B1	A2 and B1
L	L	H	Z	B2	A2 and B2
H	L	H	A2	A1	A1 and A2
L	H	H	B1	B2	A1 and B1, A2 and B2
H	H	H	B2	B1	A1 and B2, A2 and B1

PRODUCT PREVIEW

SN74CBT16209 18-BIT BUS-EXCHANGE SWITCH

NOVEMBER 1992 – REVISED FEBRUARY 1993

function diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Current into any pin, I_O	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air):	DGG	0.6 W
	DL	0.85 W
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
T_A	Operating free-air temperature	-40	85	°C

PRODUCT PREVIEW

SN74CBT16209 18-BIT BUS-EXCHANGE SWITCH

NOVEMBER 1992 - REVISED FEBRUARY 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		$V_{CC} = 4.5 \text{ V}$,	$I_I = -18 \text{ mA}$			-1.2	V
I_I		$V_{CC} = 0$,	$V_I = 5.5 \text{ V}$			10	μA
		$V_{CC} = 5.5 \text{ V}$,	$V_I = 5.5 \text{ V or GND}$			± 1	
I_{OS}		$V_{CC} = 4.5 \text{ V}$,	$V_I(A) = 0$,			100	mA
I_{CC}		$V_{CC} = 5.5 \text{ V}$,	$I_O = 0$,			1	mA
			$V_I = V_{CC} \text{ or GND}$				
I_{CC}^\ddagger		$V_{CC} = 3.6 \text{ V}$,	One input at 2.7 V ,			0.2	mA
			Other inputs at V_{CC} or GND				
C_i	Control pins	$V_I = 3 \text{ V or } 0$				4	pF
$C_{i(O\text{N})}$		$V_O = 3 \text{ V or } 0$,	$OE = \text{GND}$			8	pF
$C_{i(O\text{FF})}$		$V_O = 3 \text{ V or } 0$,	$OE = V_{CC}$			6	pF
r_{on}^\S		$V_{CC} = 4.5 \text{ V}$,	$V_I = 0$,			6	Ω
		$V_{CC} = 4.5 \text{ V}$,	$V_I = 2.4 \text{ V}$,			12	
			$I_I = 64 \text{ mA}$				
			$I_I = 15 \text{ mA}$				

† All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B pin at the indicated current through the switch. On resistance is determined by the lower of the voltages of the two (A or B) pins.

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = -40^\circ \text{ to } 85^\circ\text{C}$			$T_A = 0^\circ \text{ to } 70^\circ\text{C}$			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}^\P	A or B	B or A						0.25	ns
t_{PHL}^\P								0.25	
t_{PLH}	S0, S1, S2	A or B				1.5	7.5	ns	
t_{PHL}						1.5	7.5		
t_{PZH}	S0, S1, S2	A or B				1.5	7.5	ns	
t_{PZL}						1.5	7.5		
t_{PHZ}	S0, S1, S2	A or B				1.5	6.5	ns	
t_{PLZ}						1.5	6.5		

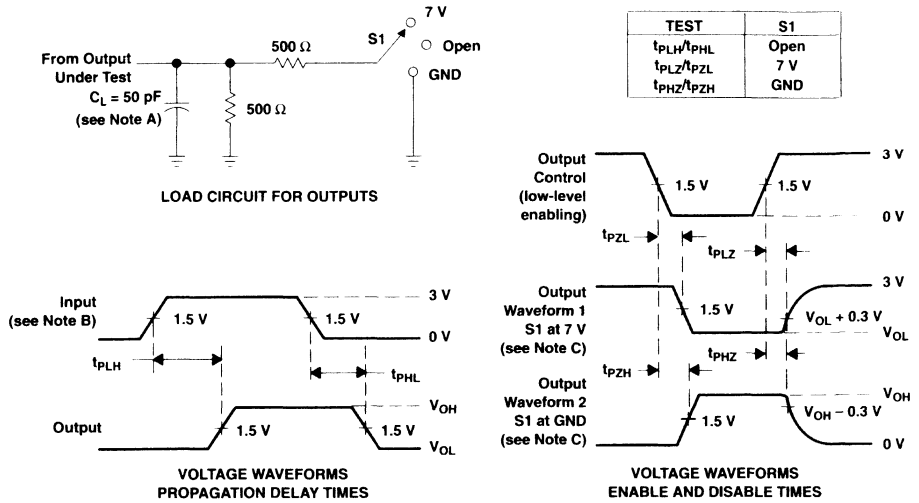
¶ This parameter is characterized but not tested. This propagation delay is due to the RC delay of the on resistance of the switch and the load capacitance.

PRODUCT PREVIEW

SN74CBT16209 18-BIT BUS-EXCHANGE SWITCH

NOVEMBER 1992 - REVISED FEBRUARY 1993

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

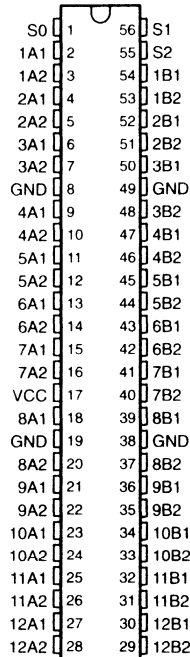
PRODUCT PREVIEW

SN74CBT16212 24-BIT BUS-EXCHANGE SWITCH

NOVEMBER 1992 - REVISED FEBRUARY 1993

- 5- Ω Switch Connection Between Two Ports
- TTL-Compatible Input and Output Levels
- Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages

DGG OR DL PACKAGE
(TOP VIEW)



description

The SN74CBT16212 provides 24 bits of high-speed TTL-compatible bus switching or exchanging. The low on resistance of the switch allows connections to be made without adding propagation delay.

The device operates as a 24-bit bus switch or a 12-bit bus exchanger, which provides data exchanging between the four signal ports via the data-select pins (S0–S2).

The SN74CBT16212 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

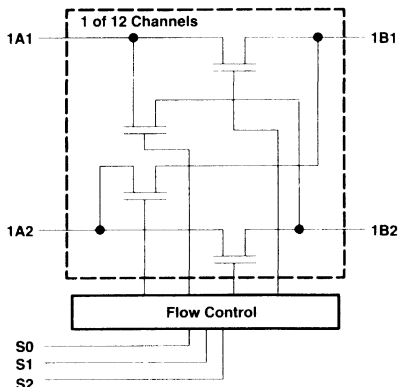
S0	S1	S2	A1	A2	FUNCTION
L	L	L	Z	Z	Disconnect
H	L	L	B1	Z	A1 and B1
L	H	L	B2	Z	A1 and B2
H	H	L	Z	B1	A2 and B1
L	L	H	Z	B2	A2 and B2
H	L	H	A2	A1	A1 and A2
L	H	H	B1	B2	A1 and B1, A2 and B2
H	H	H	B2	B1	A1 and B2, A2 and B1

PRODUCT PREVIEW

SN74CBT16212 24-BIT BUS-EXCHANGE SWITCH

NOVEMBER 1992 – REVISED FEBRUARY 1993

function diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Current into any pin, I_O	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DGG	0.7 W
DL	1 W
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
T_A	Operating free-air temperature	-40	85	$^\circ\text{C}$

PRODUCT PREVIEW

SN74CBT16212 24-BIT BUS-EXCHANGE SWITCH

NOVEMBER 1992 – REVISED FEBRUARY 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	$V_{CC} = 4.5 \text{ V}$	$I_I = -18 \text{ mA}$				-1.2	V
I_I	$V_{CC} = 0$	$V_I = 5.5 \text{ V}$				10	μA
	$V_{CC} = 5.5 \text{ V}$	$V_I = 5.5 \text{ V or GND}$				± 1	
I_{OS}	$V_{CC} = 4.5 \text{ V}$	$V_I(A) = 0$	$V_I(B) = 4.5 \text{ V}$	100			mA
I_{CC}	$V_{CC} = 5.5 \text{ V}$	$I_O = 0$	$V_I = V_{CC} \text{ or GND}$			1	mA
ΔI_{CC}^\ddagger	$V_{CC} = 3.6 \text{ V}$	One input at 2.7 V,	Other inputs at V_{CC} or GND			0.2	mA
C_i	Control pins	$V_I = 3 \text{ V or 0}$			4		pF
$C_{iO(ON)}$	$V_O = 3 \text{ V or 0}$,	$\text{OE} = \text{GND}$			8		pF
$C_{iO(OFF)}$	$V_O = 3 \text{ V or 0}$,	$\text{OE} = V_{CC}$			6		pF
r_{on}^\S	$V_{CC} = 4.5 \text{ V}$,	$V_I = 0$,	$I_I = 64 \text{ mA}$			6	Ω
	$V_{CC} = 4.5 \text{ V}$,	$V_I = 2.4 \text{ V}$,	$I_I = 15 \text{ mA}$			12	

† All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B pin at the indicated current through the switch. On resistance is determined by the lower of the voltages of the two (A or B) pins.

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = -40^\circ \text{ to } 85^\circ\text{C}$			$T_A = 0^\circ \text{ to } 70^\circ\text{C}$			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}^\parallel	A or B	B or A						0.25	ns
t_{PHL}^\parallel							0.25		
t_{PLH}	S0, S1, S2	A or B				1.5	7.5	ns	
t_{PHL}						1.5	7.5		
t_{PZH}	S0, S1, S2	A or B				1.5	7.5	ns	
t_{PZL}						1.5	7.5		
t_{PHZ}	S0, S1, S2	A or B				1.5	6.5	ns	
t_{PLZ}						1.5	6.5		

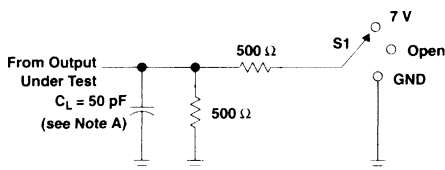
¶ This parameter is characterized but not tested. This propagation delay is due to the RC delay of the on resistance of the switch and the load capacitance.

PRODUCT PREVIEW

SN74CBT16212 24-BIT BUS-EXCHANGE SWITCH

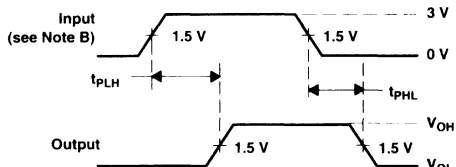
NOVEMBER 1992 – REVISED FEBRUARY 1993

PARAMETER MEASUREMENT INFORMATION

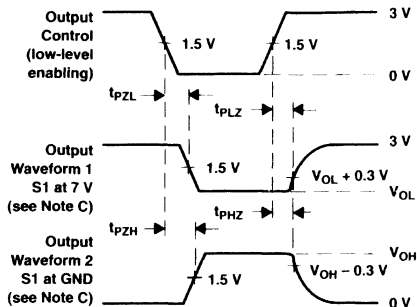


LOAD CIRCUIT FOR OUTPUTS

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_0 = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

5 Ω Switch Connection Between Two Ports

Zero propagation delay

TTL Compatible input and output levels

Packaged in Plastic 300-mil Shrink
Small-Outline (DL) and Thin Shrink
Small-Outline (DGG) Packages

description

The SN74CBT16214 provide 12 bits of high-speed TTL-compatible bus switching between three separate ports. The low on resistance of the switch allows connections to be made without adding propagation delay.

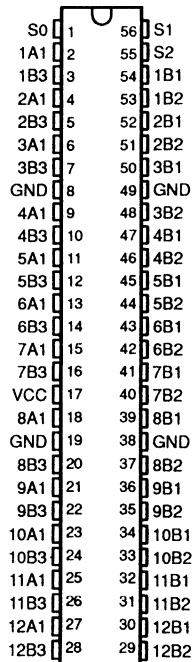
The SN74CBT16214 operates as a 12 bit bus switch via the data flow select pins (S0-S2).

The SN74CBT16214 is characterized for operation from -40°C to 85°C.

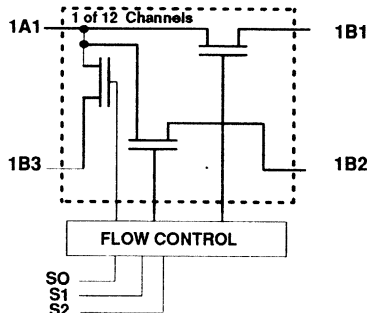
FUNCTION TABLE

S2	S1	S0	A1	Function
L	L	L	Z	DISCONNECT
L	L	H	B1	A1 AND B1
L	H	L	B2	A1 AND B2
L	H	H	Z	DISCONNECT
H	L	L	Z	DISCONNECT
H	L	H	B3	A1 AND B3
H	H	L	B1	A1 AND B1,
H	H	H	B2	A1 AND B2,

DL or DGG PACKAGE
(TOP VIEW)



Function diagram



SN74CBT16214

3 TO 1 BUS SELECT SWITCH

MAY 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_i (see Note 1)	-0.5 V to 7 V
Current into any pin, I_O	128 mA
Input clamp current, I_{IK} ($V_i < 0$)	-50 mA
Maximum power package dissipation at $T_A = 55^\circ\text{C}$ (in still air): DL	0.85 W
DGG	W
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

	MIN	NOM	MAX	UNIT
V_{CC} Supply voltage	4.5		5.5	V
V_{IH} High-level input voltage	2			V
V_{IL} Low-level input voltage			0.8	V
T_A Operating free-air temperature	-40		85	$^\circ\text{C}$

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_{IK}	$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$			-1.2	V
I_I	$V_{CC} = 0$, $V_i = 5.5\text{ V}$			10	μA
	$V_{CC} = 5.5\text{ V}$, $V_i = 5.5\text{ or GND}$			± 1	μA
I_{OS}	$V_{CC} = 4.5$, $V_i(\text{A}) = 0\text{ V}$, $V_i(\text{B}) = 4.5\text{ V}$	100			mA
I_{CC}	$V_{CC} = 5.5\text{ V}$, $I_O = 0$, $V_i = V_{CC}$ or GND			1	mA
ΔI_{CC} †	$V_{CC} = 3.6\text{ V}$, One input at 2.7 V, Other inputs at V_{CC} or GND			0.2	mA
C_i Control pins	$V_i = 3\text{ V or } 0$		4		pF
C_{ON}	$V_O = 3\text{ V or } 0$, $OE = \text{GND}$		10		pF
C_{OFF}	$V_O = 3\text{ V or } 0$, $OE = V_{CC}$		6		pF
R_{ON} §	$V_{CC} = 4.5$, $V_i = 0\text{ V}$, $I_I = 64\text{ mA}$			6	Ω
	$V_{CC} = 4.5$, $V_i = 2.4\text{ V}$, $I_I = 15\text{ mA}$			12	

‡ All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

§ Measured by the voltage drop between A and B pin at the indicated current through the switch. On resistance is determined by the lower of the voltages of the two (A, B) pins.

† This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

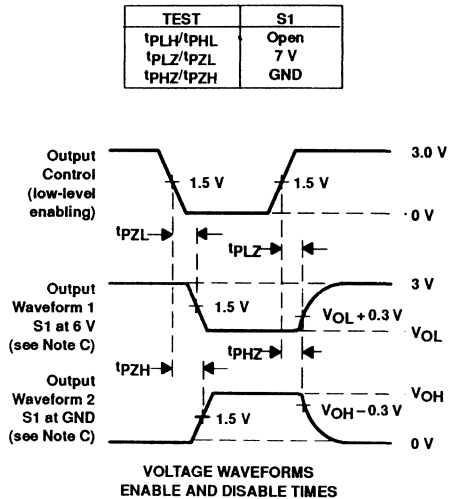
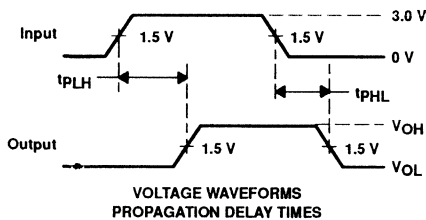
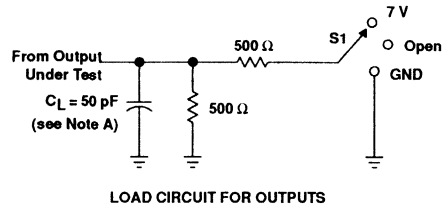
SN74CBT16214 3 TO 1 BUS SELECT SWITCH

MAY 1993

switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_a = -40$ to 85 °C			$T_a = 0$ to 70 °C			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
$t_{PLH}†$	A	B							ns
$t_{PHL}†$									
t_{PZH}	S0, S1, S2	A							ns
t_{PZL}									
t_{PHZ}	S0, S1, S2	A							ns
t_{PLZ}									
t_{PLH}	S0, S1, S2	A							ns
t_{PHL}									

† This parameter is characterized but not tested. This propagation delay is due to the RC delay of the on resistance of the switch and the load capacitance.



- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_0 = 50$ Ω , $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

General Information

1

LVT Octals and Widebus™

2

LVC MSI, Octals and Widebus™

3

ALVC Widebus™

4

LV MSI and Octals

5

GTL Widebus™

6

CBT Bus Switches and 5-V/3-V Volt. Translators

7

Application Notes

8

LVT Characterization Information

9

Mechanical Data

10

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Texas Instruments Crossbar Switches (CBT)	8-13

Mixing It Up With 3.3 Volts

Ken Ristow

Steve Perna

**General Purpose Logic – Semiconductor Group
Texas Instruments Incorporated**

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Introduction

The evolution to a 3.3-V supply voltage is being driven by a complex matrix of requirements. Leading the way are the characteristics of advanced semiconductor processing and the need to reduce system power without a corresponding tradeoff in system performance. Reduction of the horizontal and vertical feature sizes of transistors is the most common method of increasing the density of cells that can be contained in an integrated circuit. These feature sizes or geometries are typically represented as minimum process dimensions for advanced products such as dynamic random access memories (DRAMs).

DRAM manufacturers have forecasted that all 64M-bit versions will be developed for operation from a supply voltage of 3.3 ± 0.3 V. For 16M-bit DRAM products there is no such rule of thumb as certain vendors expect to operate from 3.3 V, while others will offer different product versions with differing voltage levels. An approach used by several manufacturers is to provide 5-V power supply operation externally with internal step-down conversion to 3.3 V. For static random access memories (SRAMs), manufacturers have announced that most 16M versions will operate at 3.3 V or lower (down to 2.7 V).

Typical 1M-bit DRAM geometries are on the order of $1.2 \mu\text{m}$, and it is not a problem to apply a 5-V power supply to this type of product. However, as the feature sizes of DRAMs shrink, the stresses of 5-V operation can preclude their reliable operation due to high field-effect failures. One such effect is hot-carrier injection which over time increases the transistor's threshold, leading to eventual nonoperation. Another field-effect concern is the breakdown of the transistor's gate oxide causing internal shorts. Therefore, reducing the supply voltage is one way to ensure reliable operation of devices fabricated in state-of-the-art processes.

The reduction of V_{CC} from 5 V to 3.3 V reduces the power consumed by the device which increases system reliability while reducing costs associated with the removal of the heat. The power consumption of a device is primarily a function of its capacitive load, frequency of operation, and supply voltage. However, capacitive load and frequency have a linear effect on a device's power consumption while supply voltage has a square relationship. Because of this square relationship a small reduction in voltage significantly reduces the power consumed, as illustrated in Figure 1, and is a driving factor towards 3.3-V operation.

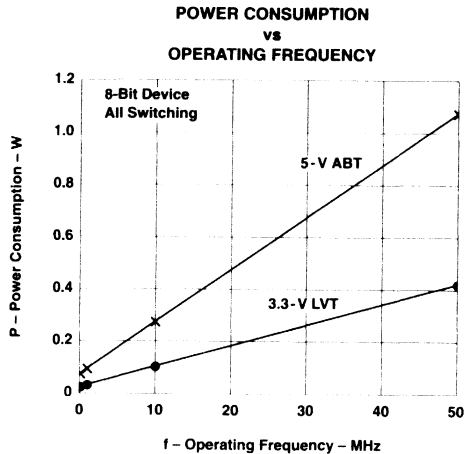


Figure 1. 3-V to 5-V Power vs Frequency Comparison

The Market for Low Voltage

User demand for low-voltage products can be grouped into specific brackets depending on their performance-power priorities. End equipments such as multiuser servers, engineering workstations, high-end desktop PCs, and other high-performance motherboards favor high performance over low power, but are interested in 3.3-V products to reduce or eliminate bulky, noisy cooling fans in the attempt to shrink external case size for better desktop fit. Some end equipments favor low power at the expense of high performance such as battery-powered notebooks and palmtop computers, portable test equipment, and point-of-sale terminals. A few end equipments require equal priority for high performance and low power such as laptop computers, automotive and air/space products.

The universal benefits to users of low-voltage products are higher reliability and lower cost. The higher reliability is relative to standard 5-V solutions and results from lower stress gradients on device junctions and oxides, lower buildup of heat due to lower power consumption, and improved signal integrity from the reduction in ground bounce and signal noise. Lower power consumption usually yields lower costs since power costs money to generate and heat costs money to dissipate. All things considered, it is desirable to use inexpensive plastic packages instead of metal or ceramic to dissipate heat. For battery users, an added benefit of the lower power consumption of low-voltage products is one of increased battery lifetime.

Of all the end-equipment groups which can benefit from the use of low-voltage products, it appears that demand will be initially driven by battery-operated computers. This market segment is defined by notebook and palmtop computers, as well as point-of-sale terminals which are designed to capture data at remote field sites and either store it for downloading later or transmit it real time via an on-board transmitter. The goal for these systems is to have a battery life of 8 to 10 hours, roughly the equivalent of one work day or the time to complete a transcontinental airplane trip.

The unregulated battery market is itself quite varied, however, because different batteries exhibit very different voltage characteristics between fully charged and discharged states. Two AA batteries provide for 3-V supply when charged, decreasing to about 2.7 V after use. Three NiCad batteries provide for a baseline 3.6-V supply fully charged but the spread actually runs from about 3.3 V up to 3.9 V. For now the unregulated battery market demands low-voltage products which are optimized to run from 2.7 V up as high as 3.9 V. Since performance is directly related to supply voltage, it is more important for device optimization to be extended down to 2.7 V, where devices will slow down appreciably.

There are some barriers for low-voltage acceptance in the short term. Specification standardization remains an issue. Also, the access to adequate supplies of 3.3-V devices can be a problem. Generally, DRAM memories are leading the way into 3.3-V operation with SRAM memories close behind. Coupled with the low-voltage microprocessors now available, systems are being implemented with the core components operating at 3.3 V, with volume requirements not beginning until the '94-'95 time frame. Hindering the migration to a full 3.3-V system is the availability of support products such as: disk drives, LCDs, A/D converters, RF transmitters, and EPROMS.

Migration to 3.3 V

The need to migrate to power supplies with supply voltages less than 3.3 V has been an issue since 1984 when two JEDEC standards were adopted. Standard 8.0 was intended to address both regulated (3-V to 3.6-V) and unregulated (2-V to 3.6-V) battery applications. Standard 8.1 was intended to address higher-performance applications operating from a regulated power supply that could interface to a standard 5-V TTL device as well as a low-voltage device. Essentially Standard 8.0 established regulated low-voltage CMOS (LVCMOS) and unregulated low-voltage battery-operated (LVBO) interfaces, and Standard 8.1 established the low-voltage TTL (LVTTL) interface.

Committee members have since determined that the original two standards are inadequate. Since most systems currently require a TTL interface, Standard 8.1 LVTTL is the most critical one being reviewed now. When ratified, the new LVTTL standard will present methods for interfacing with 5-V systems and contain a provision for battery-operated systems. Until this happens, a generic lack of compatibility will exist between the various 3.3-V and 5-V interfaces.

Existing solutions for 3.3-V operation have historically been 5-V products and processes characterized for 3.3-V operation. A CMOS process is typically chosen because of the scaling effect of the inverter thresholds with respect to the supply voltage. HCMOS and Advanced CMOS devices support both 5-V and 3.3-V operation by this method. One drawback is slower propagation delay when compared to parts specifically designed for 3-V operation. A limitation of many of these devices is their inability to directly interface to a 5-V system when running off a 3.3-V supply, due to diodes from the input and input/output (I/O) pins to V_{CC} . This limits input voltages to $V_{CC} + 0.5$ V and limits direct connection to a 5-V system.

Mixed-Mode Operation

This dilemma of device incompatibility between the large installed base of 5-V systems with the newly emerging 3.3-V systems is a serious industry concern. Mixed-mode operation allows for direct communication between the two systems. Devices which support this mode must be designed for maximum input voltages of 5.5 V without any long-term reliability issues. Another concern is that the output drive must be capable of driving a standard-TTL backplane, while still providing for rail-to-rail switching for compatibility with 3-V CMOS systems.

Figure 2 compares the standard-TTL dc interface levels with two of the emerging low-voltage standards. Low-voltage CMOS (LVCMOS) is a pure CMOS specification that specifies low current rail-to-rail output drive along with input voltage levels, V_{IH} and V_{IL} , which are ratios of V_{CC} . Low-voltage TTL (LVTTTL) utilizes the standard-TTL input levels of 0.8 and 2 V as well as specifying a higher dc output drive than LVCMOS. To ensure interoperability between these three varied standards, a multipurposed low-voltage interface device must meet all of the requirements of the three different specifications.

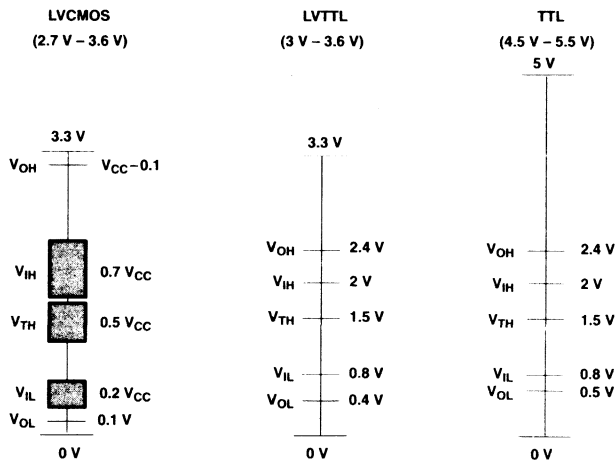


Figure 2. Comparison of 3.3-V and 5-V Interfaces

LVT Family Characteristics

To address the need for a complete low-voltage interface solution, Texas Instruments has developed a new generation of logic parts capable of mixed-mode operation. The LVT series of parts rely on a state-of-the-art submicron BiCMOS process to provide up to a 90% reduction in static power dissipation over ABT devices, and provides the following family characteristics:

5.5-V maximum input voltage

Specified 2.7- to 3.6-V supply voltage

I/O structures that support power-on (live) insertion

Standard TTL output drives of:

$V_{OH} = 2 \text{ V}$ at $I_{OH} = -32 \text{ mA}$

$V_{OL} = 0.55 \text{ V}$ at $I_{OL} = 64 \text{ mA}$

Rail-to-rail switching for driving CMOS

Maximum supply currents of:

$I_{CC(L)} = 15 \text{ mA}$

$I_{CC(H)} = 250 \text{ } \mu\text{A}$

$I_{CC(Z)} = 250 \text{ } \mu\text{A}$

Propagation delays of:

$t_{pd} < 4.6 \text{ ns}$

$t_{pd} \text{ (LE to Q)} < 5.1 \text{ ns}$

$t_{pd} \text{ (CLK to Q)} < 6.3 \text{ ns}$

Surface-mount packaging support including fine-pitch packages:

48- and 56-pin SSOP for LVT Widebus™

20- and 24-pin TSSOP for standard LVT

LVT input/output characteristics

Figure 3 shows a simplified LVT output and illustrates the mixed-mode signal drive designed into the output stage. This combination of a high-drive TTL stage along with the rail-to-rail CMOS switching gives the LVT series of product extreme application flexibility. These parts have the same drive characteristics as 5-V ABT devices, as shown in Figure 4, providing the dc drive needed for existing 5-V backplanes and allowing for a simple solution to reduce system power via the migration to 3.3-V operation.

Not only can LVT devices operate as 3-V-to-5-V level translators by supporting input or I/O voltages of 5.5 V with $V_{CC} = 2.7$ to 3.6 V, the inputs can withstand 5.5 V even when $V_{CC} = 0$ V. This allows for the devices to be used under partial system power-down applications or when live insertion is required.

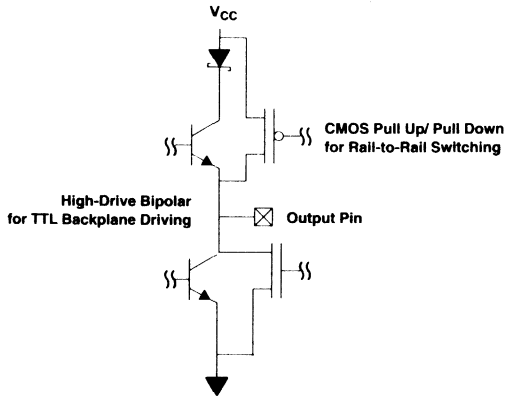


Figure 3. Simplified LVT Output Structure

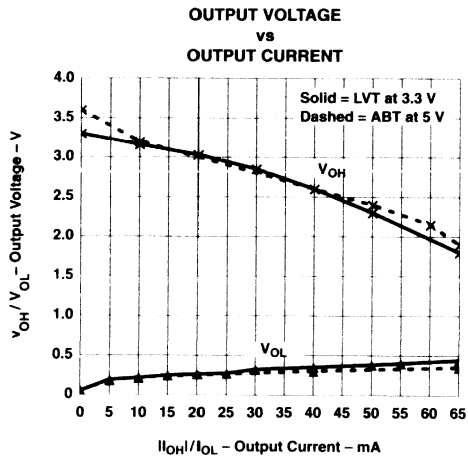


Figure 4. ABT vs LVT Output Drive Comparison

Bus Hold

Many times devices are used in applications that do not provide a pullup or pulldown voltage to the input or I/O pin when the driving device goes into a high-impedance state, as in the case of CMOS buses or nonbused lines. To prevent application problems or oscillations, a large pullup resistor is typically used, but this consumes board area and contributes to driver loading. The LVT series of devices incorporate active circuitry that holds unused or floating inputs or I/Os at a valid logic level. This circuitry provides for a typical holding current, $\pm 100 \mu\text{A}$, that is sufficient enough to overcome any CMOS-type leakages. Since this is an active circuit, it does take current, approximately $\pm 500 \mu\text{A}$, to toggle the state of the input. This current is negligible when compared to the magnitude of current that is needed to charge a capacitive load, and does not affect the propagation delay of the driving output.

Conclusion

LVT devices solve the system need for a transparent interface between the low-voltage and 5-V sections by providing for mixed-signal operation. The devices support live insertion or partial-power applications while providing low-input leakage currents. The outputs are capable of driving today's 5-V backplanes with a considerable reduction in the device's power consumption and are packaged in state-of-the-art fine-pitch surface-mount packages.

Texas Instruments Crossbar Switches (CBT)

**Ramzi Ammar
General Purpose Logic – Semiconductor Group
Texas Instruments Incorporated**

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What Are Texas Instruments Crossbar Switches (CBT)?

Crossbar switches are high-speed bus-connect devices. Each switch consists of an N-channel MOS transistor driven by a CMOS gate. When enabled, the N-channel transistor gate is pulled to V_{CC} and the switch is on. These devices have an on resistance of approximately $5\ \Omega$ and a propagation delay of 250 ps. They are capable of conducting a current of 64 mA each. The transistor clamps the output at $\approx 1\text{ V}$ less than the gate potential regardless of the level at the input pin. This is one of the N-channel transistor characteristics (see Figures 1 and 2). Note the $\approx 1\text{ V}$ difference between the gate (V_{CC}) and the source (V_O) at any point on the graph.

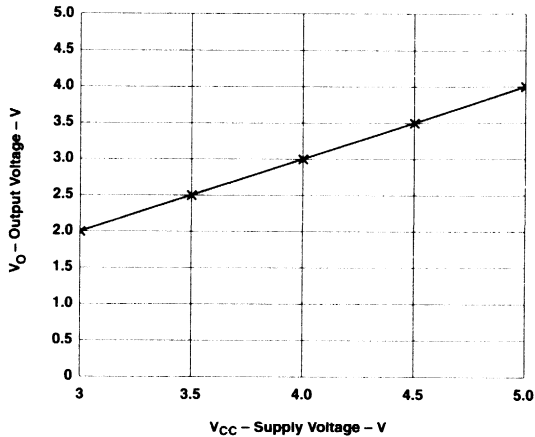


Figure 1. Output Voltage vs Supply Voltage

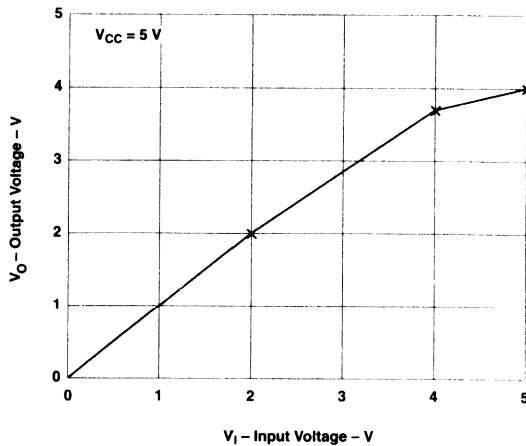


Figure 2. Output Voltage vs Input Voltage

r_{on} increases gradually with V_I until V_I approaches $V_{CC} - 1$ V, where r_{on} rapidly increases clamping V_O at $V_{CC} - 1$ V (see Figure 3). Also, by the nature of the N-channel transistor design, the input and output pins are fully isolated when the transistor is off. Leakage and capacitance is to ground and not between input and output which minimizes feedthrough when the transistor is off.

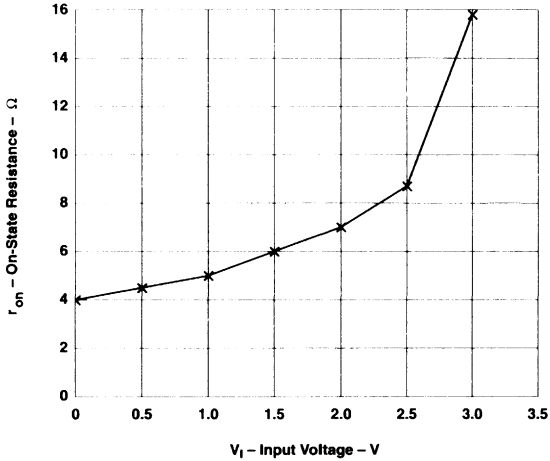


Figure 3. On-State Resistance vs Input Voltage

What Does Texas Instruments Offer in the CBT Family?

Here is a sampling of CBT switches that will be offered by Texas Instruments followed by an application note that helps designers understand and identify areas where these devices can be useful.

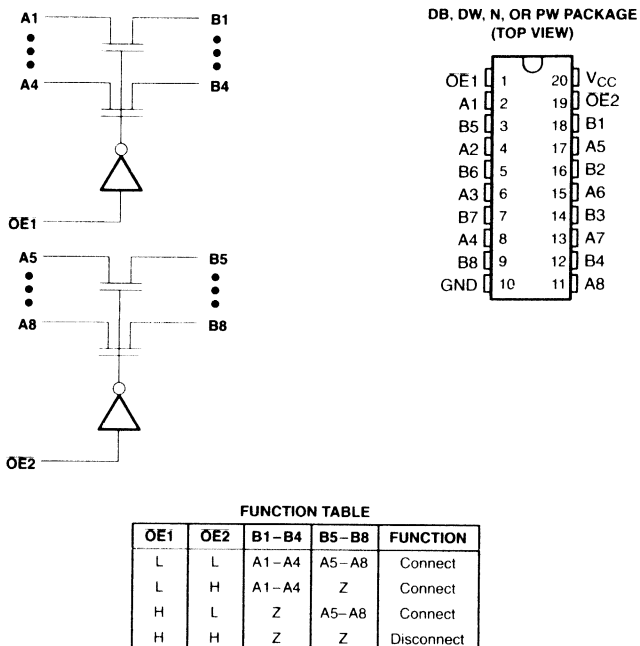
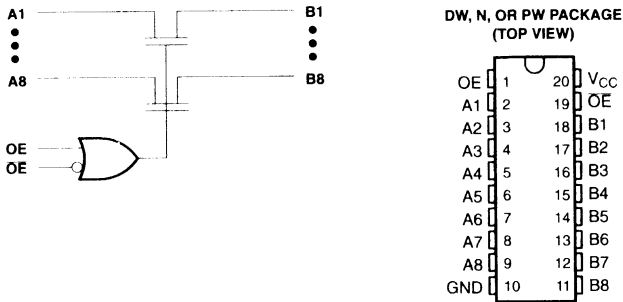


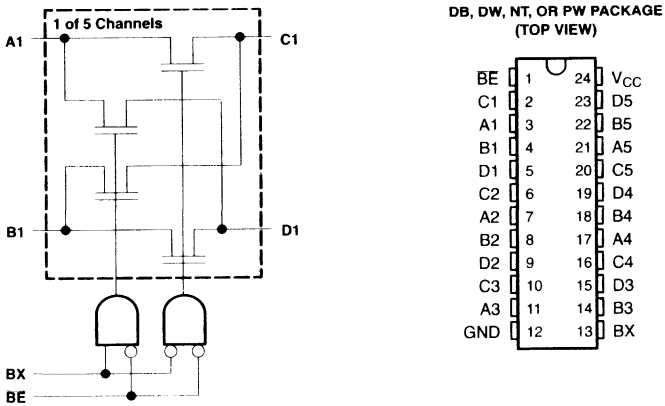
Figure 4. SN74CBT3244 – 8-Bit Crossbar Switch



FUNCTION TABLE

OE	OE	B1-B8	FUNCTION
X	L	A1-A8	Connect
H	X	A1-A8	Connect
L	H	Z	Disconnect

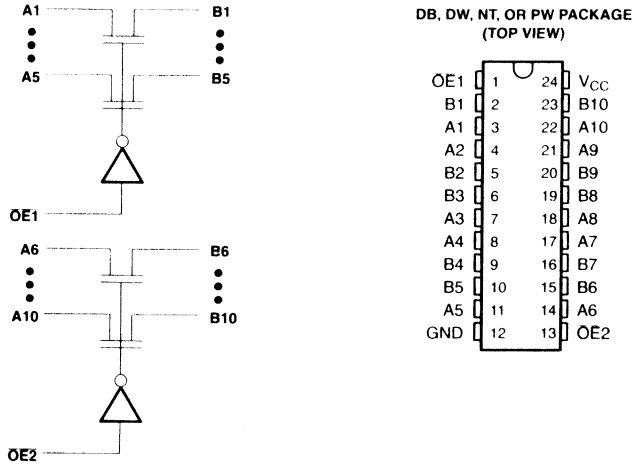
Figure 5. SN74CBT3245 – 8-Bit Crossbar Switch



FUNCTION TABLE

BE	BX	A1-A5	B1-B5	FUNCTION
L	L	C1-C5	D1-D5	Connect
L	H	D1-D5	C1-C5	Exchange
H	X	Z	Z	Disconnect

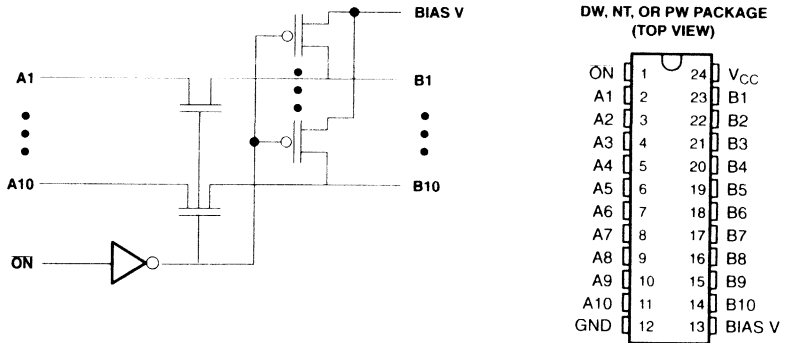
Figure 6. SN74CBT3383 – 10-Bit Bus-Exchange Switch



FUNCTION TABLE

OE1	OE2	B1-B5	B6-B10	FUNCTION
L	L	A1-A5	A6-A10	Connect
L	H	A1-A5	Z	Connect
H	L	Z	A6-A10	Connect
H	H	Z	Z	Disconnect

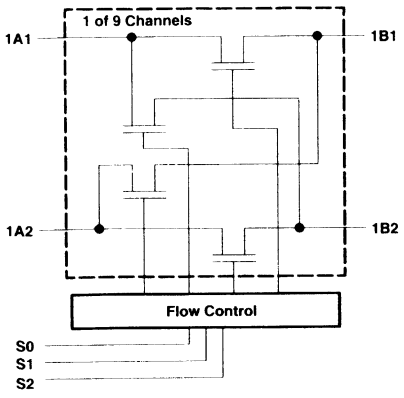
Figure 7. SN74CBT3384 – 10-Bit Crossbar Switch



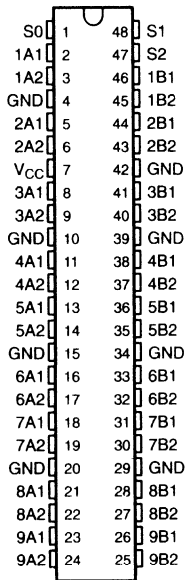
FUNCTION TABLE

ON	B1-B8	FUNCTION
L	A1-A8	Connect
H	BIAS V	Precharge

Figure 8. SN74CBT6800 – 10-Bit Crossbar Switch With Precharged Outputs for Live Insertion



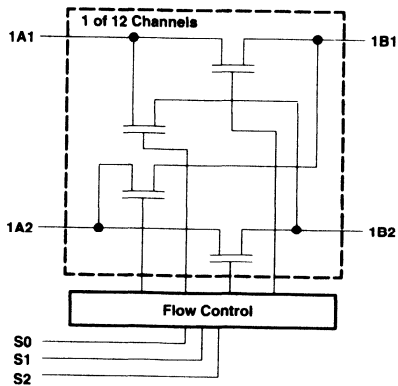
DGG OR DL PACKAGE
(TOP VIEW)



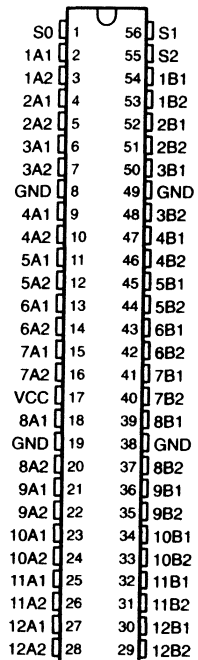
FUNCTION TABLE

S0	S1	S2	A1	A2	FUNCTION
L	L	L	Z	Z	Disconnect
H	L	L	B1	Z	A1 and B1
L	H	L	B2	Z	A1 and B2
H	H	L	Z	B1	A2 and B1
L	L	H	Z	B2	A2 and B2
H	L	H	A2	A1	A1 and A2
L	H	H	B1	B2	A1 and B1, A2 and B2
H	H	H	B2	B1	A1 and B2, A2 and B1

Figure 9. SN74CBT16209 – 18-Bit Bus-Exchange Switch



DGG OR DL PACKAGE
(TOP VIEW)



FUNCTION TABLE

S0	S1	S2	A1	A2	FUNCTION
L	L	L	Z	Z	Disconnect
H	L	L	B1	Z	A1 and B1
L	H	L	B2	Z	A1 and B2
H	H	L	Z	B1	A2 and B1
L	L	H	Z	B2	A2 and B2
H	L	H	A2	A1	A1 and A2
L	H	H	B1	B2	A1 and B1, A2 and B2
H	H	H	Z	B1	A1 and B2, A2 and B1

Figure 10. SN74CBT16212 – 24-Bit Bus-Exchange Switch

Bus Switches Provide 5-V to 3-V Translation When a 3-V Supply Line Is Not Provided

These devices can also provide bidirectional 5-V to 3-V translation with no added propagation delay or direction control using only a 5-V supply line and a diode. Figure 4 illustrates this application. A 4.3-V V_{CC} can be created by placing a diode between V_{CC} and the switch. This causes the gate to drop to 4.3 V due to the diode drop of approximately 0.7 V. This drop, coupled with the gate-to-source voltage drop of 1 V, brings V_O to a maximum 3.3-V level that can be used to drive a signal in a 3-V environment.

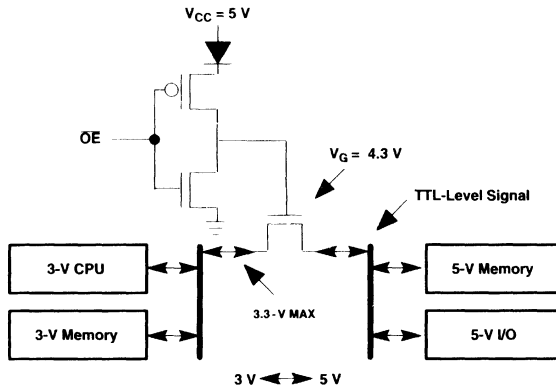


Figure 11. 5-V TTL to 3-V TTL Translator System

Bus Switches Can Be Used to Replace Drivers and Transceivers in Bus Applications

Bus switches introduce near-zero propagation delay. They can replace drivers and transceivers in systems where signal buffering is not required. They can be used in a multiprocessor system as a fast bus connect, or they can be used as a bus-exchange switch for crossbar systems, ping-pong memory connect, or bus-byte swap. These devices can also replace relays that are used in automated test equipment (ATE) to connect or disconnect load resistors in negligible time with the same low on resistance and without the reliability problem that relays provide.

Bus Switches Convert TTL Logic to Hot-Card Insertion Capability

This application is most used in systems that require hot-card insertion or removal of cards without disturbing or loading down the bus. These systems are designed to run continuously and cannot be shut down for any reason, such as telephone switches, manufacturing controls, real-time transaction systems, and airline-reservation networks. These systems/cards use some logic families like ACL, HCMOS, etc., that do not provide isolation from the bus when power is partially removed, causing system error. Also, connectors are designed so that the ground pins are connected first followed by the signal pins then V_{CC} last. In this condition, the existing logic must ensure that the I/O signals do not disturb or load down the bus. This assurance cannot be achieved using CMOS logic since it contains P-channel transistors that provide an inherent diode between the I/O pins and V_{CC} that is forward biased when driven above V_{CC} (see Figure 5). In a situation where V_{CC} is disconnected, these diodes are capable of pulling the system bus to approximately one diode drop above ground leaving the bus disturbed.

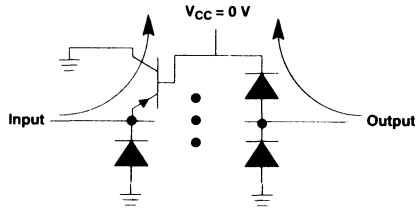


Figure 12. ACL Direction of Current Flow When $V_{CC} = 0\text{ V}$

Another issue to consider is that, when V_{CC} is rising but still below the device operating voltage, the logic should ensure that the outputs are in the high-impedance state and that the bus is totally isolated until the card is ready for operation. Finally, the capacitance of the card must be seen by the system bus as low as possible so that when the card is inserted and the capacitance is charged up, disturbance or bus error will not occur.

There are two solutions to this problem. One is to use Texas Instruments BCT or ABT families, since both allow the input and output to be off when V_{CC} is removed due to the absence of the clamping diodes to V_{CC} (see Figure 6). They also provide an active circuit that ensures the output to be in the high-impedance state during part of the V_{CC} power up or power down.

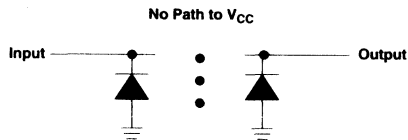


Figure 13. No ABT Current Flow When $V_{CC} = 0\text{ V}$

The second choice is to use the Texas Instruments crossbar technology (CBT) family. This can be done by placing the switch between the card logic and the connector to serve as an isolator when power is removed (see Figure 7). Note that the switch uses an N-doped channel that prevents the current from flowing into the switch when powered down. One device in particular, the SN74CBT6800, is designed specifically for hot-card insertion. It has a built-in P-channel pullup tied to a bias voltage (BIAS V) that is provided to ensure power up such that the buses are not connected. Other devices can be used in the same manner, however, to ensure the high-impedance state during power up or power down. The enable pins of the switch should be tied to V_{CC} through a pullup resistor. The minimum value of the resistor is determined by the current-sinking capability of the driver (see Figure 8).

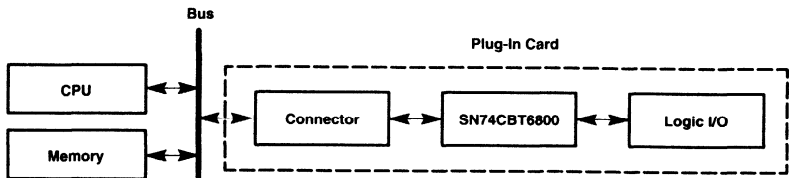
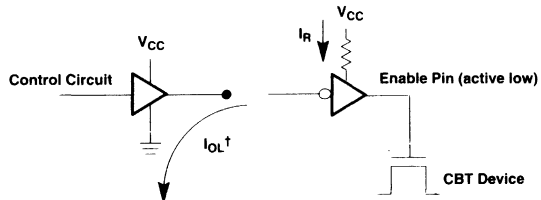


Figure 14. Hot-Card Insertion Application



$^\dagger I_{OL} > I_R$, so the control signal can override the pullup resistor.

Figure 15. Power-Up High-Impedance State With CBT

Conclusion

Texas Instruments crossbar switches can be used in several applications. Although they are simple N-channel transistors, they are capable of providing several important bus functions, such as hot-card insertion, near-zero-delay communication, 5-V to 3-V translation and memory management in multiprocessor environments.

General Information	1
LVT Octals and Widebus™	2
LVC MSI, Octals and Widebus™	3
ALVC Widebus™	4
LV MSI and Octals	5
GTL Widebus™	6
CBT Bus Switches and 5-V/3-V Volt. Translators	7
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LVT Characterization Information	9
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LVT Family Characteristics

Ken Ristow
General Purpose Logic – Semiconductor Group
Texas Instruments Incorporated

Introduction

To address the need for a complete low-voltage interface solution, Texas Instruments has developed a new generation of logic parts capable of mixed-mode operation. The LVT series of parts rely on a state-of-the-art submicron BiCMOS process to provide up to a 90% reduction in static power dissipation over ABT, as well as the following family characteristics:

5.5-V maximum input voltage

Specified 2.7-V to 3.6-V supply voltage

I/O structures which support live insertion

Standard TTL output drives of:

$V_{OH} = 2\text{ V}$ at $I_{OH} = -32\text{ mA}$

$V_{OL} = 0.55\text{ V}$ at $I_{OL} = 64\text{ mA}$

Rail-to-rail switching for driving CMOS

Maximum supply currents of:

$I_{CCL} \leq 15\text{ mA}$

$I_{CCH} \leq 200\text{ }\mu\text{A}$

$I_{CCZ} \leq 200\text{ }\mu\text{A}$

Propagation delays of:

$t_{pd} < 4.6\text{ ns}$

$t_{pd}(\text{LE to Q}) < 5.1\text{ ns}$

$t_{pd}(\text{CLK to Q}) < 6.3\text{ ns}$

Surface mount packaging support including fine-pitch packages:

48-/56-pin SSOP and TSSOP for LVT Widebus™

20-/24-pin SOIC and TSSOP for standard LVT

LVT Input/Output Characteristics

Figure 1 shows a simplified LVT output and illustrates the mixed-mode-signal drive designed into the output stage. This combination of a high-drive TTL stage along with the rail-to-rail CMOS switching gives the LVT series of product extreme application flexibility. These parts have the same drive characteristics as 5-V ABT devices (see Figure 2), and provide the dc drive needed for existing 5-V backplanes. This allows for a simple solution to reduce system power via the migration to 3.3-V operation.

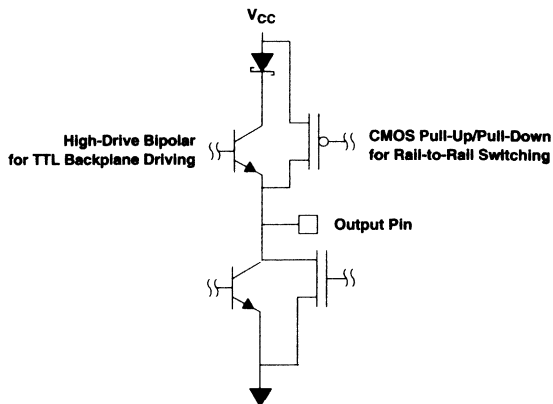


Figure 1. Simplified LVT Output Structure

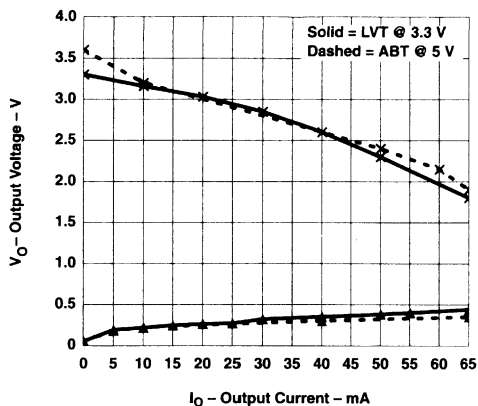


Figure 2. ABT vs LVT Output-Drive Comparison

Not only can LVT devices operate as 3-V to 5-V level translators by supporting input or I/O voltages of 5.5 V with $V_{CC} = 2.7$ V to 3.6 V, the inputs can withstand 5.5 V even when $V_{CC} = 0$ V. This allows for the devices to be used under partial system power-down applications or those which require live insertion.

Bus Hold

Many times, devices are used in applications that do not provide a pullup or pulldown voltage to the input or I/O pin when the driving device goes into a high-impedance state, as in the case of CMOS buses or nonbused lines. To prevent application problems or oscillations, a large pullup resistor is typically used, but this consumes board area and contributes to driver loading. The LVT series of devices incorporate active circuitry that holds unused or floating inputs or I/Os at a valid logic level. This circuitry provides for a typical holding current, ± 100 μ A, that is sufficient enough to overcome any CMOS-type leakages. Since this is an active circuit, it does take current, approximately ± 500 μ A, to toggle the state of the input. This current is trivial when compared to the tens of mA of current that is needed to charge a capacitive load, thereby not affecting the propagation delay of the driving output.

Conclusion

LVT devices solve the system need for a transparent seam between the low-voltage and 5-V sections by providing for mixed-signal operation. The devices support live-insertion or partial-power applications, while providing for low-input leakage currents. The outputs are capable of driving today's 5-V backplanes, with a considerable reduction in device power consumption, as well as being packaged in state-of-the-art fine-pitch surface-mount packages.

LVT244 Characteristics

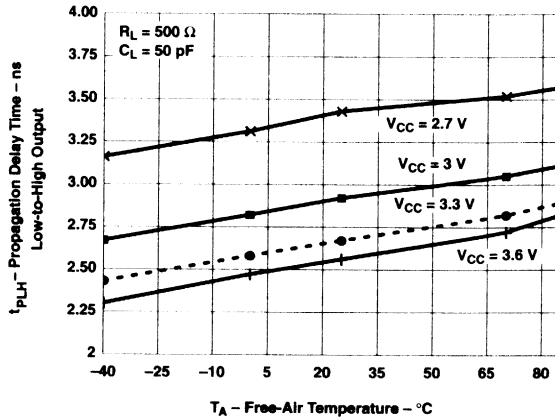


Figure 3. Propagation Delay vs Free-Air Temperature

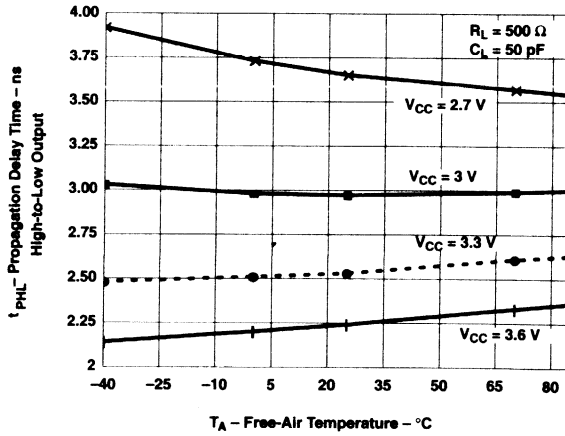


Figure 4. Propagation Delay vs Free-Air Temperature

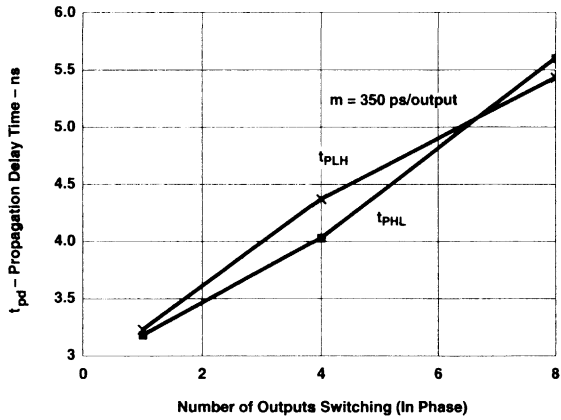


Figure 5. Propagation Delay vs Outputs Switching

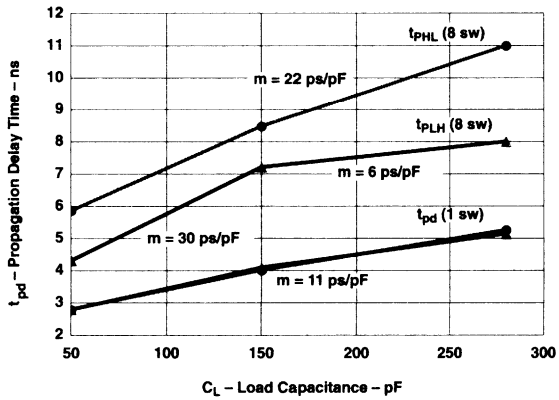


Figure 6. Propagation Delay vs Load Capacitance

'LVT244 Typical dc Characteristics

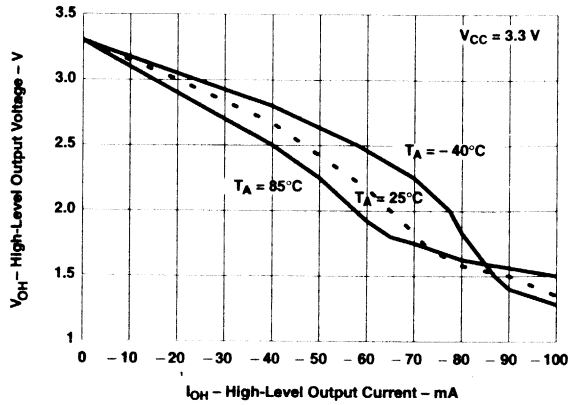


Figure 7. High-Level Output Voltage vs High-Level Output Current

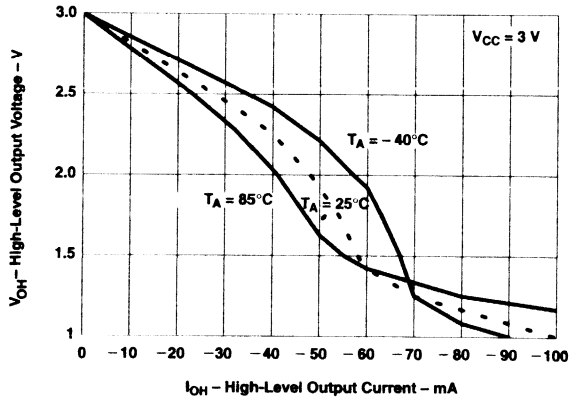


Figure 8. High-Level Output Voltage vs High-Level Output Current

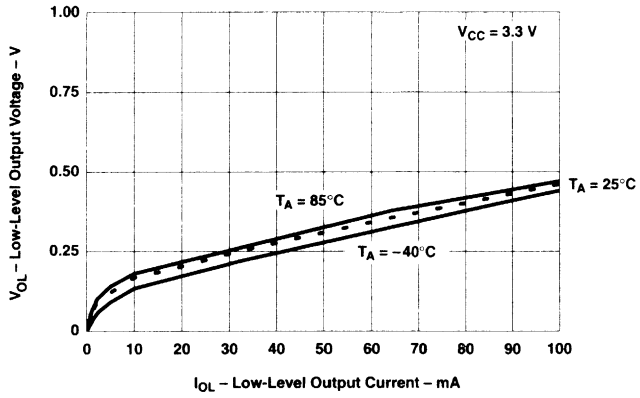


Figure 9. Low-Level Output Voltage vs Low-Level Output Current

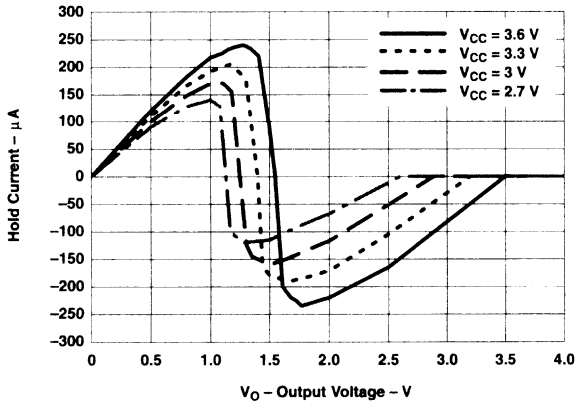


Figure 10. Hold Current vs Output Voltage

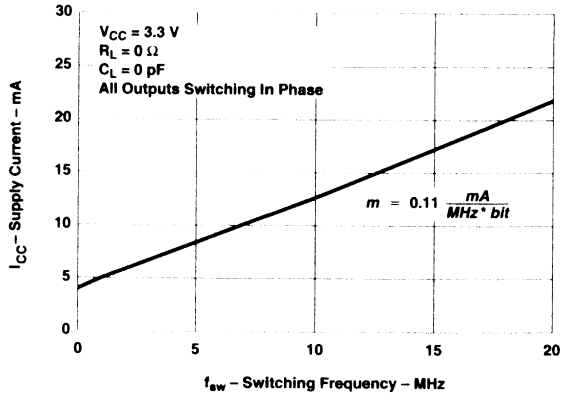


Figure 11. Supply Current vs Switching Frequency

Unloaded t_r and t_f Rates

The circuit shown below was used to measure the unloaded transition rates of the output.

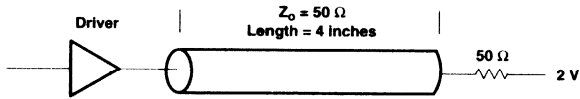


Figure 12. Load Circuit

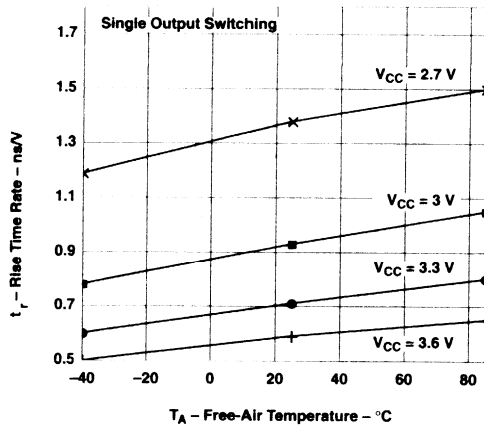


Figure 13. Rise Time Rate vs Free-Air Temperature

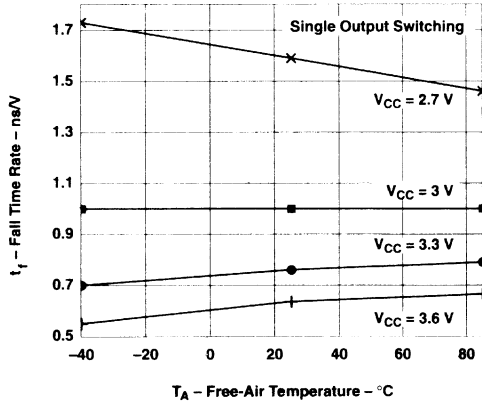


Figure 14. Fall Time Rate vs Free-Air Temperature

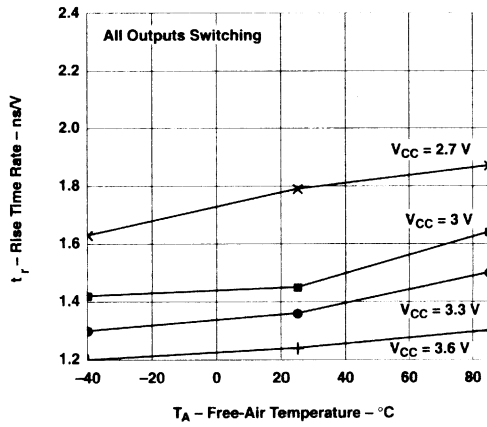


Figure 15. Rise Time Rate vs Free-Air Temperature

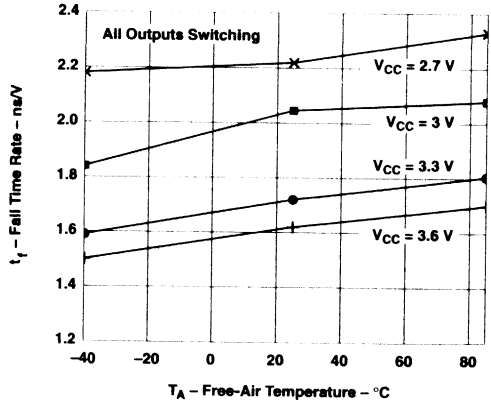


Figure 16. Fall Time Rate vs Free-Air Temperature

'LVT646 Characteristics

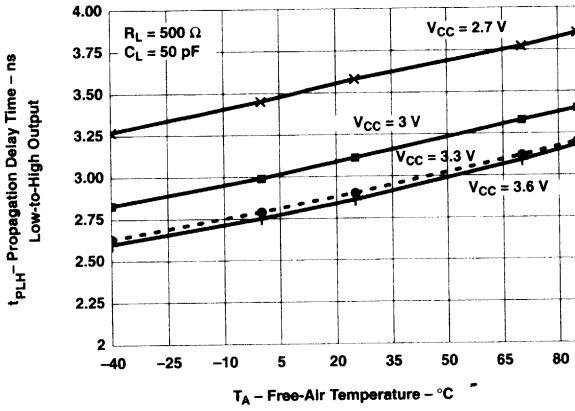


Figure 17. Thru-Mode Propagation Delay vs Free-Air Temperature

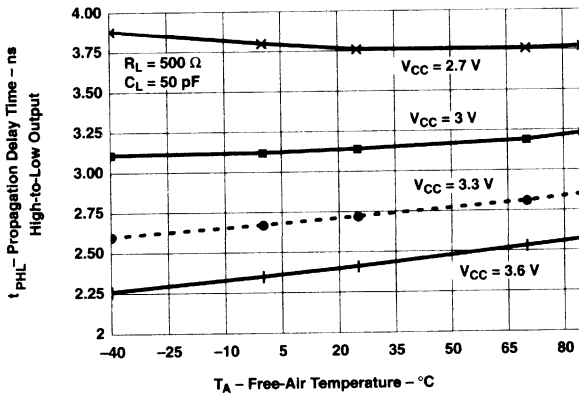


Figure 18. Thru-Mode Propagation Delay vs Free-Air Temperature

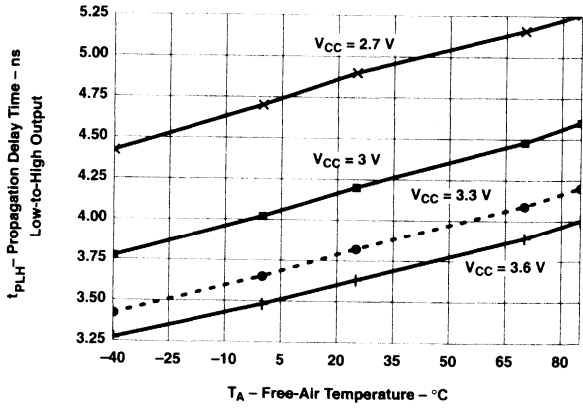


Figure 19. Clock-to-Q Propagation Delay vs Free-Air Temperature

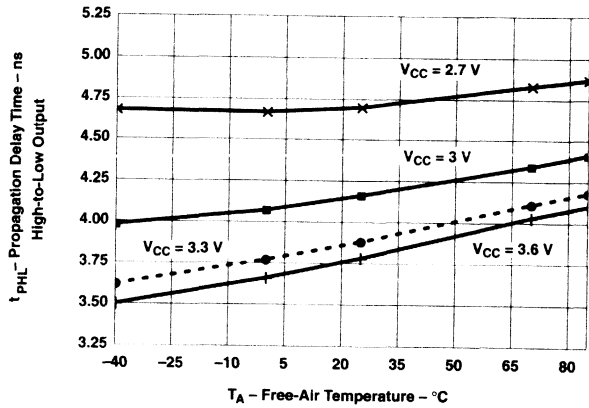


Figure 20. Clock-to-Q Propagation Delay vs Free-Air Temperature

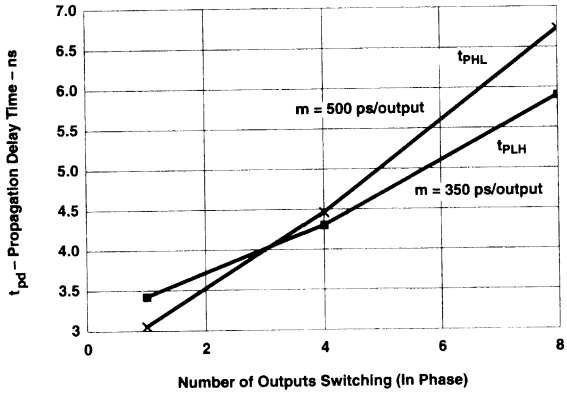


Figure 21. Propagation Delay vs Outputs Switching

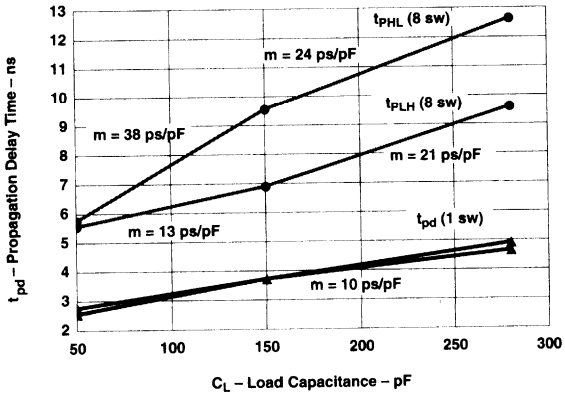
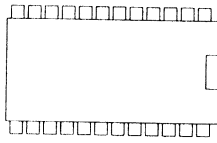
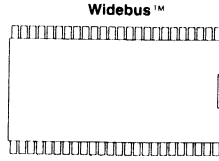


Figure 22. Propagation Delay vs Load Capacitance

Packaging Options



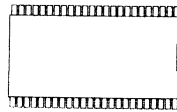
24-Pin SOIC (DW)†
 Area = 165 mm²
 Height = 2.65 mm
 Lead pitch = 1.27 mm



Widebus™
48-Pin SSOP (DL)†
 Area = 171 mm²
 Height = 2.74 mm
 Lead pitch = 0.635 mm



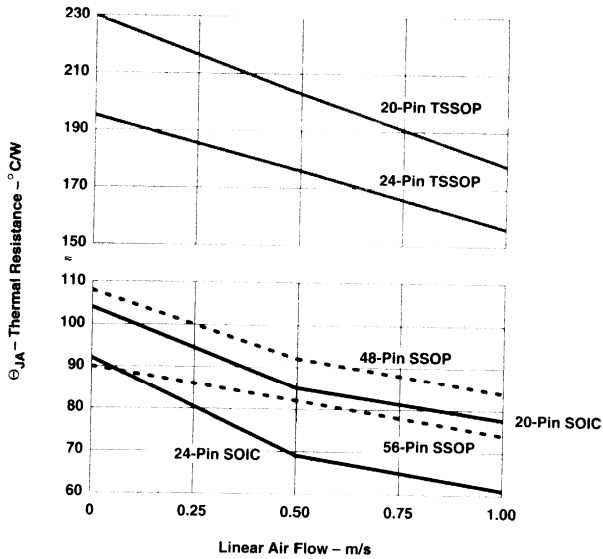
24-Pin TSSOP (PW)†
 Area = 54 mm²
 Height = 1.1 mm
 Lead Pitch = 0.65 mm



Shrink Widebus™
48-Pin TSSOP (DGG)†
 Area = 108 mm²
 Height = 1.1 mm
 Lead Pitch = 0.5 mm

† TI package designators

Thermal Characteristics



Widebus and Shrink Widebus are trademarks of Texas Instruments Incorporated.

General Information

1

LVT Octals and Widebus™

2

LVC MSI, Octals and Widebus™

3

ALVC Widebus™

4

LV MSI and Octals

5

GTL Widebus™

6

CBT Bus Switches and 5-V/3-V Volt. Translators

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LVT Characterization Information

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ORDERING INSTRUCTIONS

Electrical characteristics presented in this data book, unless otherwise noted, apply for the circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this catalog should include a four-part type number as explained in the following example.

EXAMPLE: SN 74LVT16245 DL R

Prefix

- Blank = (Standard product)
- SN = Standard prefix
- SNJ = Mil-Std-883, Class B

Unique Circuit Description

MUST CONTAIN FIVE TO NINE CHARACTERS
(from individual data sheet)

Package

MUST CONTAIN ONE TO THREE LETTERS

- D, DW = plastic small-outline package (SOIC)
- DB = plastic shrink small-outline package (SSOP)
- DGG = plastic Shrink Widebus™ package
- DL = plastic small-outline Widebus™ package
- FK = ceramic chip carrier
- HV = ceramic quad flat package
- J, JT = ceramic dual-in-line package
- N, NT = plastic dual-in-line package (DIP)
- PCA, PM, PN, PZ = plastic thin quad flat package (TQFP)
- PW = plastic thin shrink small-outline package (TSSOP)
- RC = plastic quad flat package
- W = ceramic flat package
- WD = ceramic Widebus™ flat package

Tape and Reel Packaging

Valid for surface-mount packages only. All orders for tape and reel must be for whole reels.

MUST CONTAIN ONE OR TWO LETTERS

- LE = Left embossed tape and reel (required for DB and PW packages)
- R = Standard tape and reel (required for DGG; optional for D, DW, and DL packages)

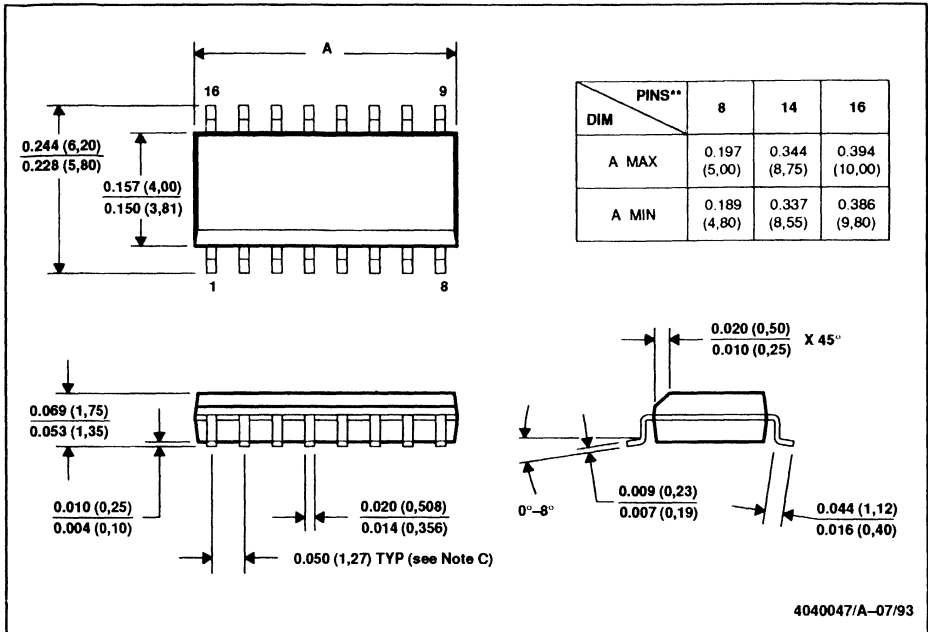
Widebus and Shrink Widebus are trademarks of Texas Instruments Incorporated.





D/R-PDSO-G**
16-PIN SHOWN

PLASTIC NARROW-BODY SMALL-OUTLINE PACKAGE



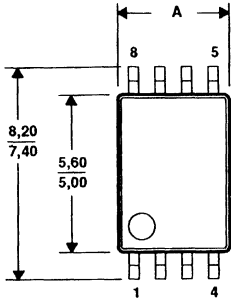
- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Leads are within 0.005 (0,127) radius of true position at maximum material condition.
 D. Body dimensions do not include mold flash or protrusion.
 E. Mold protrusion shall not exceed 0.006 (0,15).
 F. Maximum deviation from coplanarity is 0.004 (0,10).

MECHANICAL DATA

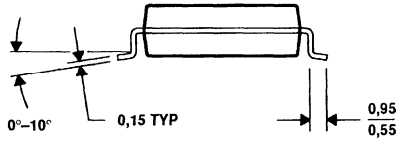
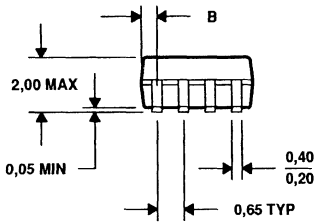
DB/R-PDSO-G**

PLASTIC SMALL-OUTLINE PACKAGE

8-PIN SHOWN



DIM \ PINS**	8	14	16	20	24	28	30	38
A MAX	3,30	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	2,70	5,90	5,90	6,90	7,90	9,90	9,90	12,30
B MAX	0,68	1,30	0,98	0,83	0,68	1,03	0,70	0,60

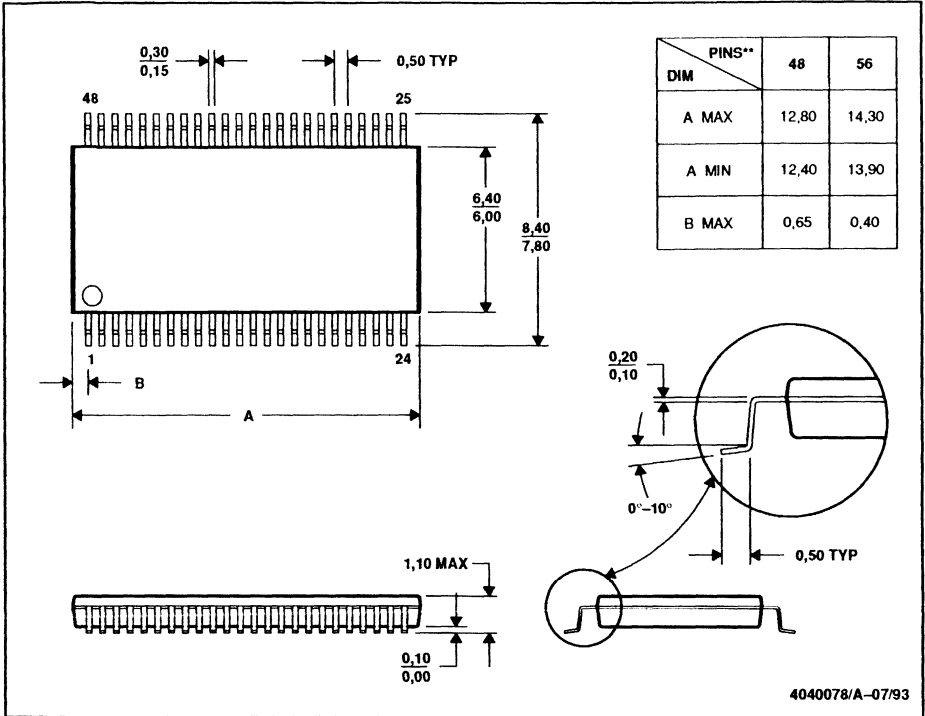


4040065/A-07/93

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions include mold flash or protrusion.

DGG/R-PDSO-G**

300-MIL THIN SHRINK SMALL-OUTLINE PACKAGE



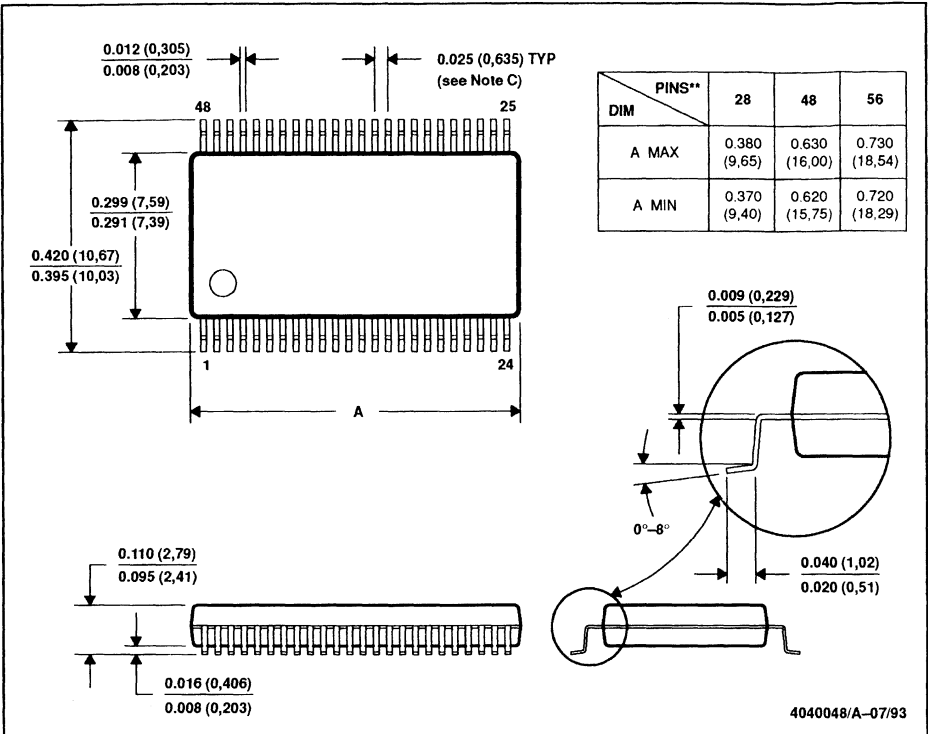
- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions include mold flash or protrusion.

MECHANICAL DATA

DL/R-PDSO-G**

PLASTIC SHRINK SMALL-OUTLINE PACKAGE

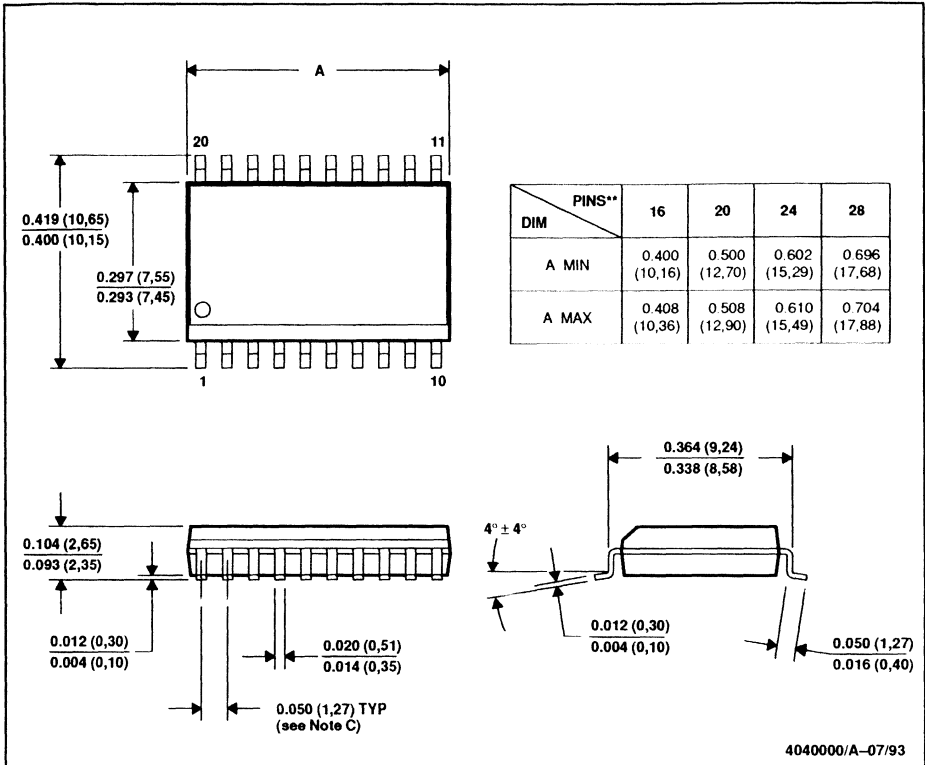
48-PIN SHOWN



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Leads are within 0.0035 (0,089) radius of true position at maximum material condition.
 - Body dimensions do not include mold flash, protrusion or gate burr.
 - Mold flash or protrusion or gate burr shall not exceed 0.015 (0,381).
 - Lead tips coplanar within 0.004 (0,102).
 - Lead length measured from lead top to point 0.010 (0,254) above seating plane.

DW/R-PDSO-G**
20-PIN SHOWN

PLASTIC WIDE-BODY SMALL-OUTLINE PACKAGE

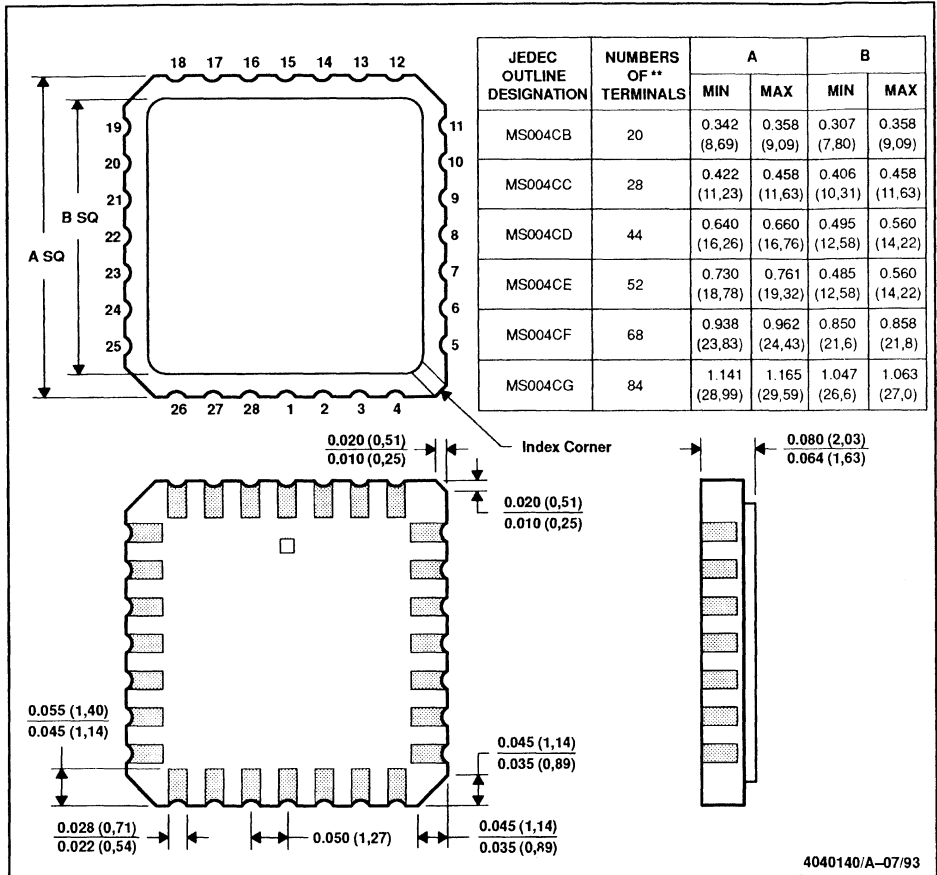


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Leads are within 0.10 (0,25) radius of true position at maximum material condition.
 D. Body dimensions do not include mold flash or protrusion.
 E. Mold flash or protrusion shall not exceed 0.006 (0,15).
 F. Lead tips coplanar within ±0.004 (±0,10) exclusive of solder.

MECHANICAL DATA

FK/S-CQCC-N**
28-TERMINAL SHOWN

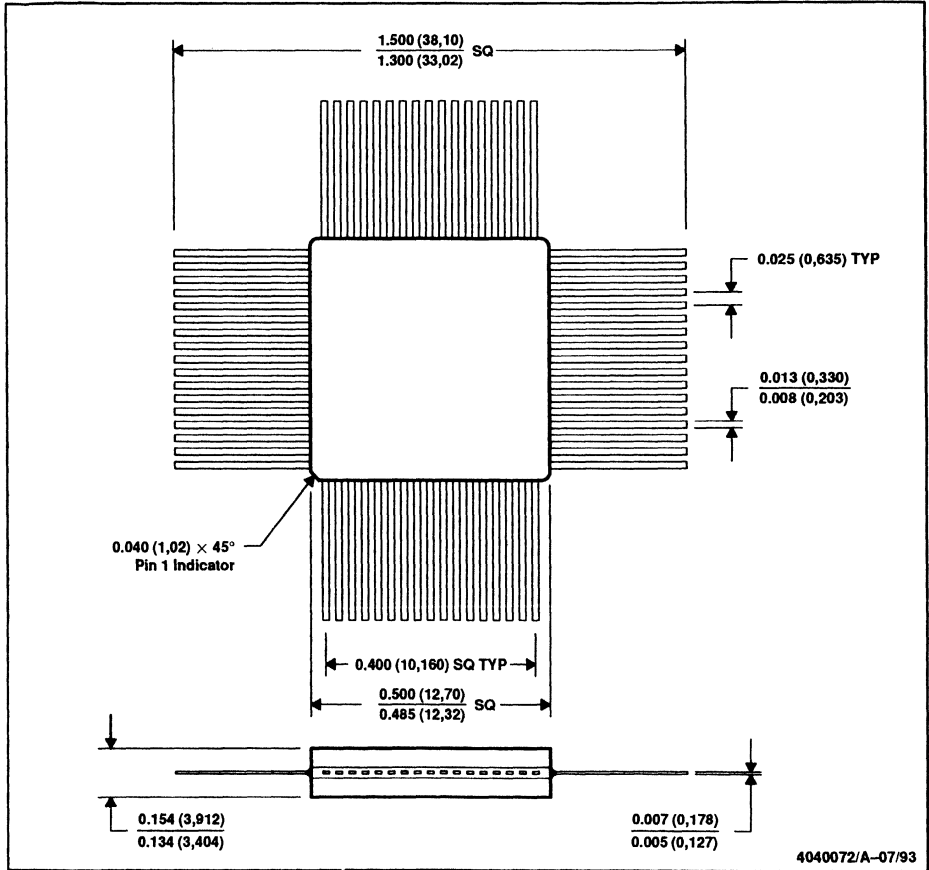
CERAMIC CHIP CARRIER



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Three-layer ceramic base with a metal lid and braze seal.
 D. FK package terminal assignments conform to JEDEC Standards 1,2 and 11.
 E. The packages are intended for surface mounting on solder lands on 0.050 (1,27) centers.

HV/S-GQFP-F68

CERAMIC QUAD FLAT PACKAGE



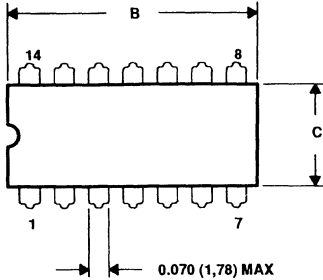
- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.

MECHANICAL DATA

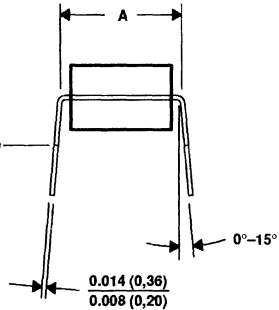
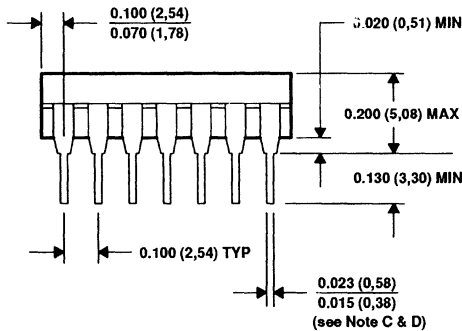
J/R-GDIP-T**

CERAMIC DUAL-IN-LINE PACKAGE

14-PIN SHOWN



DIM	PINS**				
	14	16	18	20	22
A MAX	0.310 (7,87)	0.310 (7,87)	0.310 (7,87)	0.310 (7,87)	0.410 (10,41)
A MIN	0.290 (7,37)	0.290 (7,37)	0.290 (7,37)	0.290 (7,37)	0.390 (9,91)
B MAX	0.785 (19,94)	0.785 (19,94)	0.910 (23,10)	0.975 (24,77)	1.100 (28,00)
B MIN	0.755 (19,18)	0.755 (19,18)	—	0.930 (23,62)	—
C MAX	0.280 (7,11)	0.300 (7,62)	0.300 (7,62)	0.300 (7,62)	0.388 (9,65)
C MIN	0.245 (6,22)	0.245 (6,22)	0.245 (6,22)	0.245 (6,22)	—



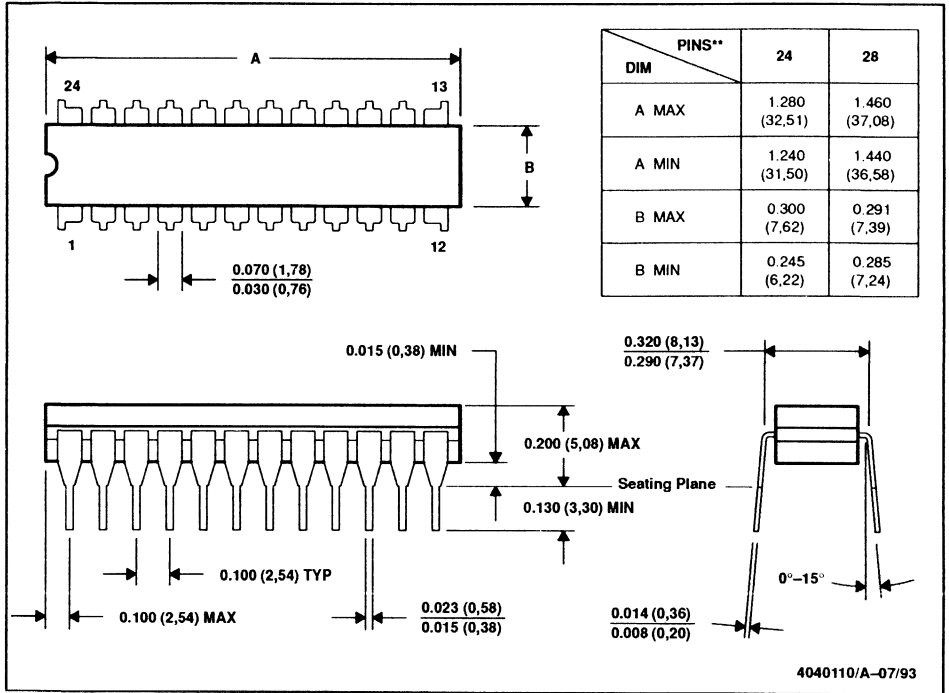
4040083/A-07/93

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This dimension does not apply for solder dipped leads.
 - For solder dipped leads, dipping area of the leads extends from the lead tip to at least 0.020 (0.51) above seating plane.

JT/R-GDIP-T**

CERAMIC DUAL-IN-LINE PACKAGE

24-PIN SHOWN



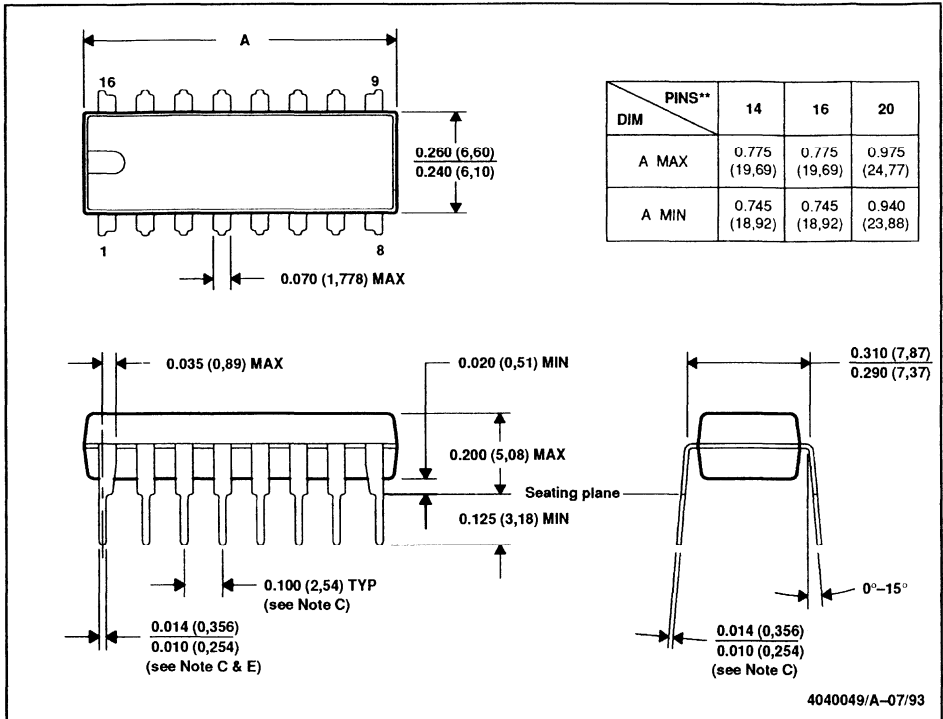
- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package is glass seal.

MECHANICAL DATA

N/R-PDIP-T**

PLASTIC DUAL-IN-LINE PACKAGE

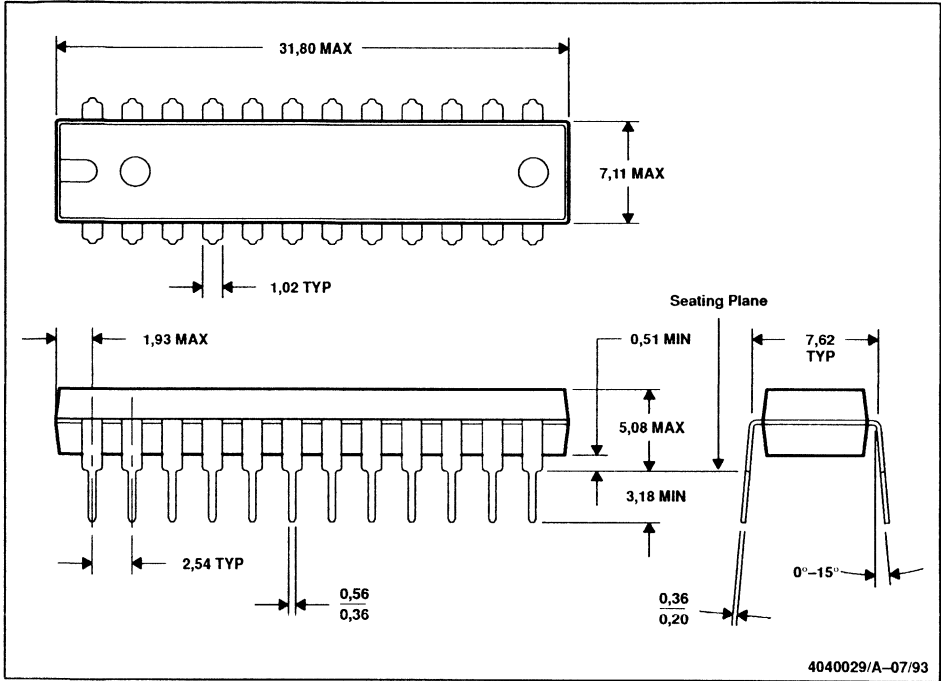
16-PIN SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Each pin centerline is located within 0.010 (0,254) of its true longitudinal position.
 - D. This dimension does not apply for solder dipped leads.
 - E. For solder dipped leads, dipping area of the leads extends from the lead tip to at least 0.020 (0,51) above seating plane.

NT/R-PDIP-T24

PLASTIC DUAL-IN-LINE PACKAGE

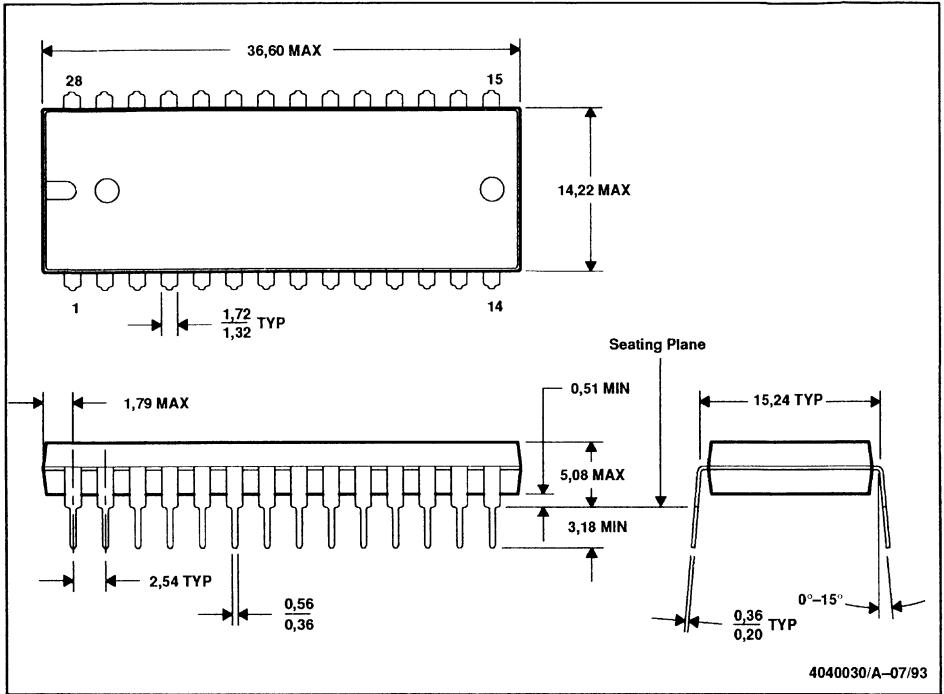


- NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Drawing source: SCJ Package handbook, 1990

MECHANICAL DATA

N/R-PDIP-T28

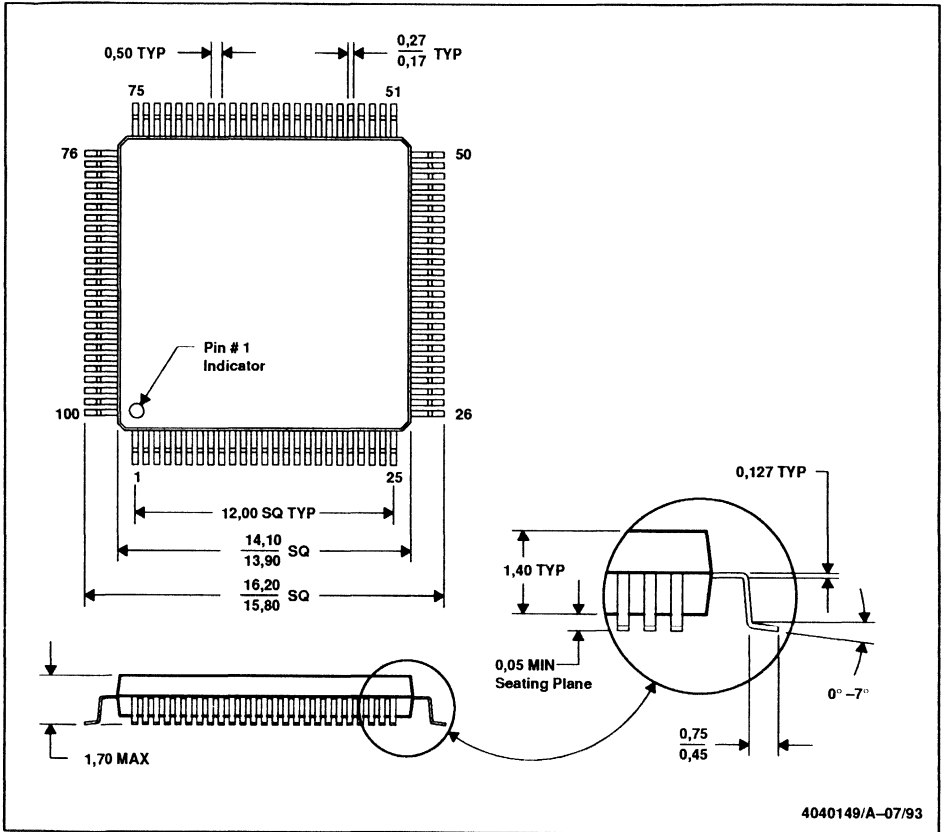
PLASTIC DUAL-IN-LINE PACKAGE



- NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Drawing source: SCJ Package handbook, 1990

PZ/S-PQFP-G100

PLASTIC QUAD FLAT PACKAGE

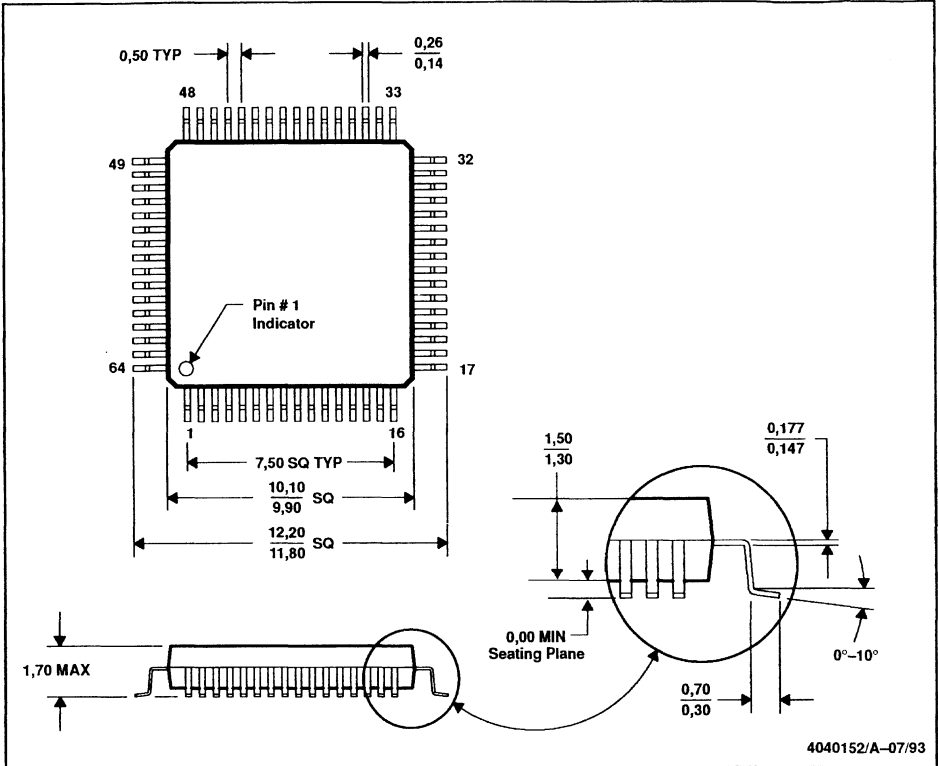


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Maximum deviation from caplanarity is 0,08 mm.

MECHANICAL DATA

PM/S-PQFP-G64

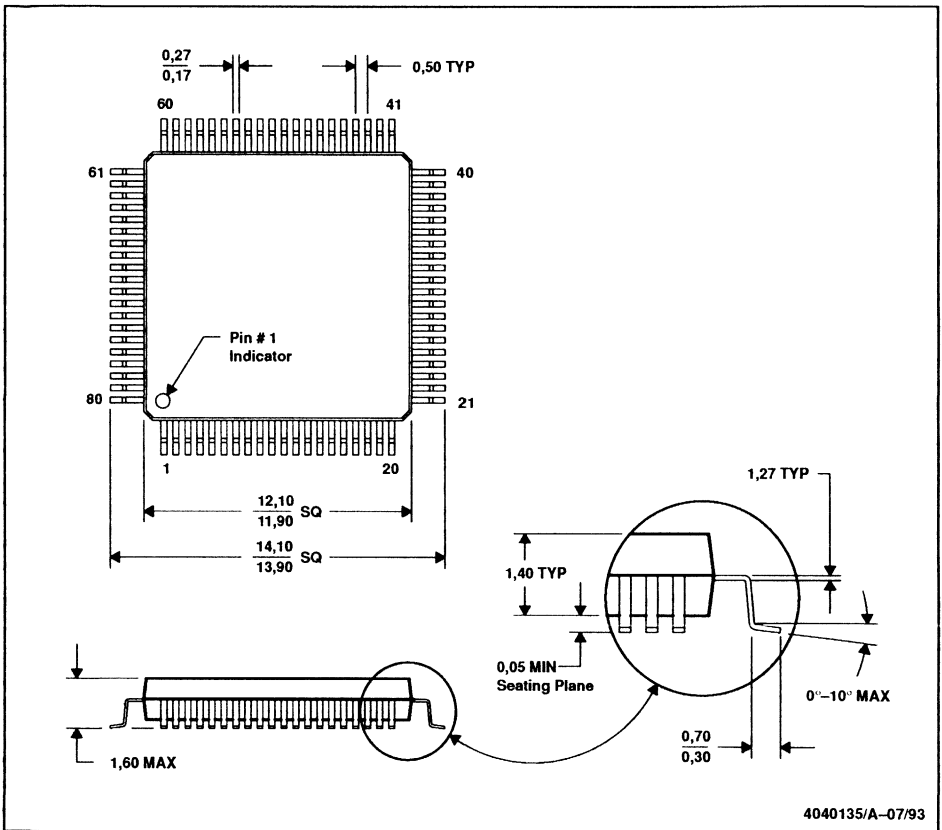
PLASTIC QUAD FLAT PACKAGE



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Maximum deviation from coplanarity is 0,08 mm.
 D. Body dimensions do not include mold flash or protrusion.

PN/S-PQFP-G80

PLASTIC QUAD FLAT PACKAGE



4040135/A-07/93

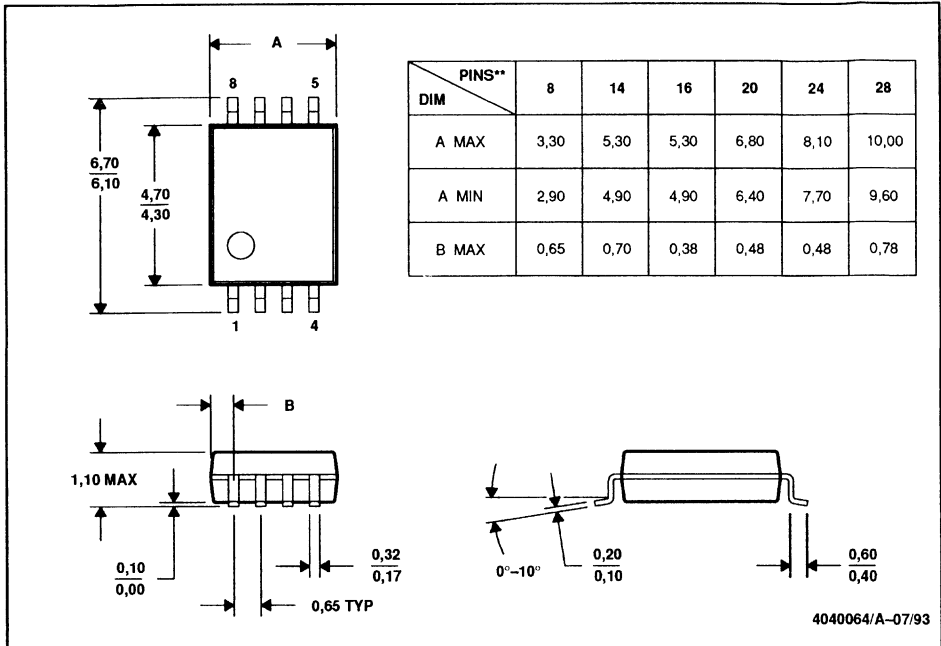
- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Maximum deviation from coplanarity is 0,08 mm.

MECHANICAL DATA

PW/R-PDSO-G**

PLASTIC SMALL-OUTLINE PACKAGE

8-PIN SHOWN

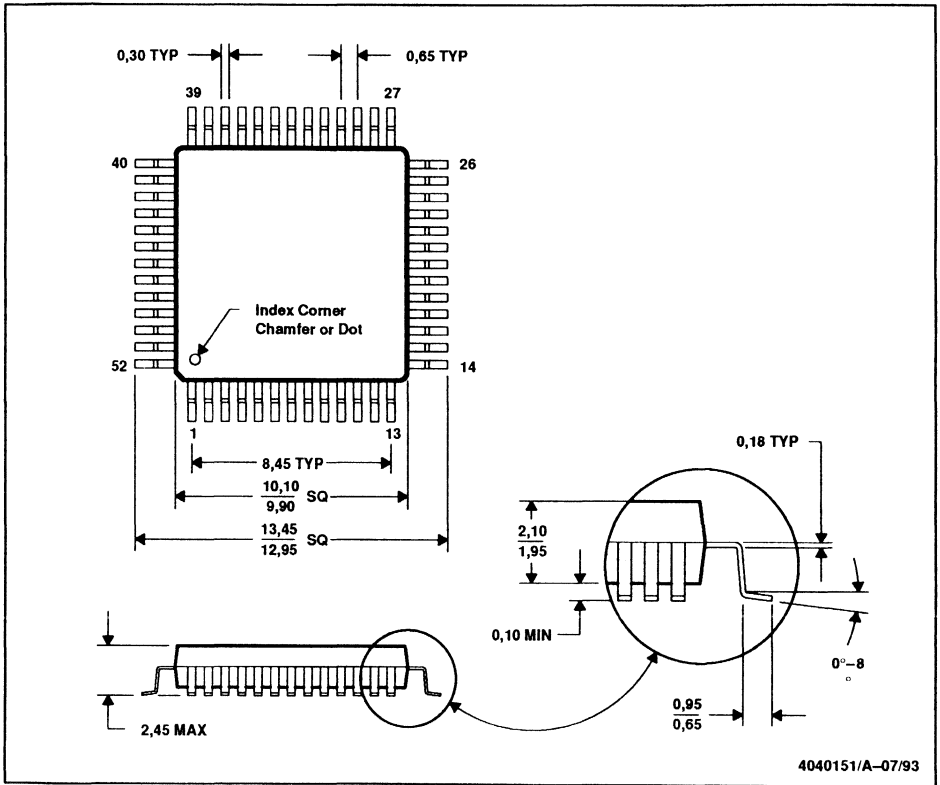


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Drawing source: SCJ Package handbook, 1990

4040064/A-07/93

RC/S-PQFP-G52

PLASTIC QUAD FLAT PACKAGE

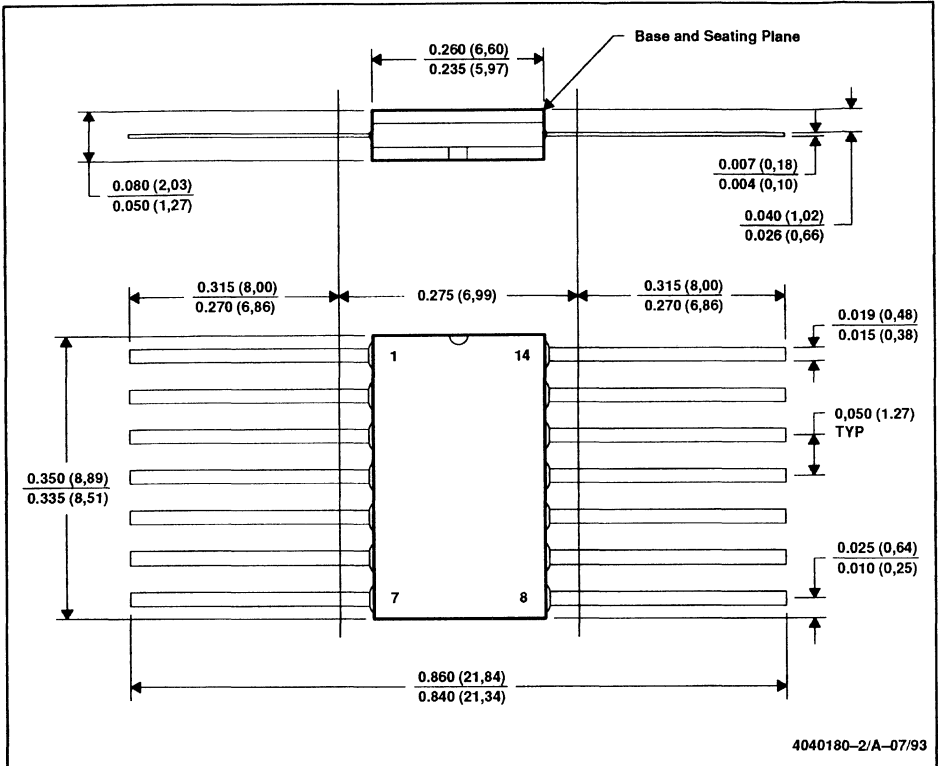


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.

MECHANICAL DATA

W/R-GDFP-F14

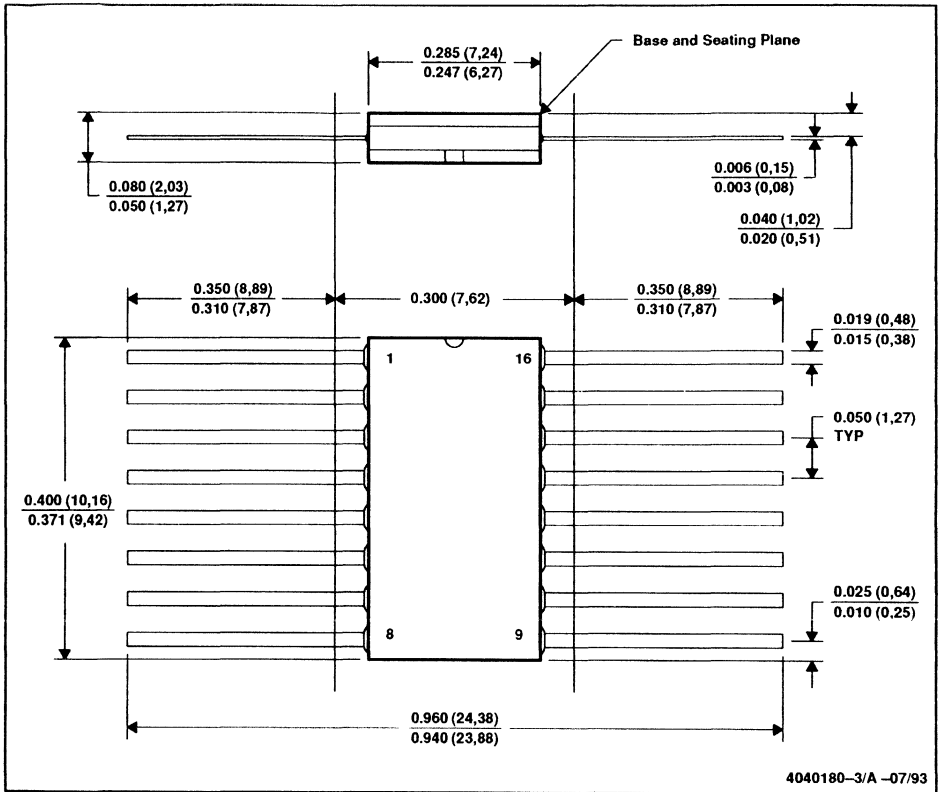
CERAMIC FLAT PACKAGE



- NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Leads are within 0.005 (0,13) radius of true position (T.P.) at maximum material condition.
D. Falls within JEDEC MO-004AA dimensions.

W/R-GDFP-F16

CERAMIC FLAT PACKAGE

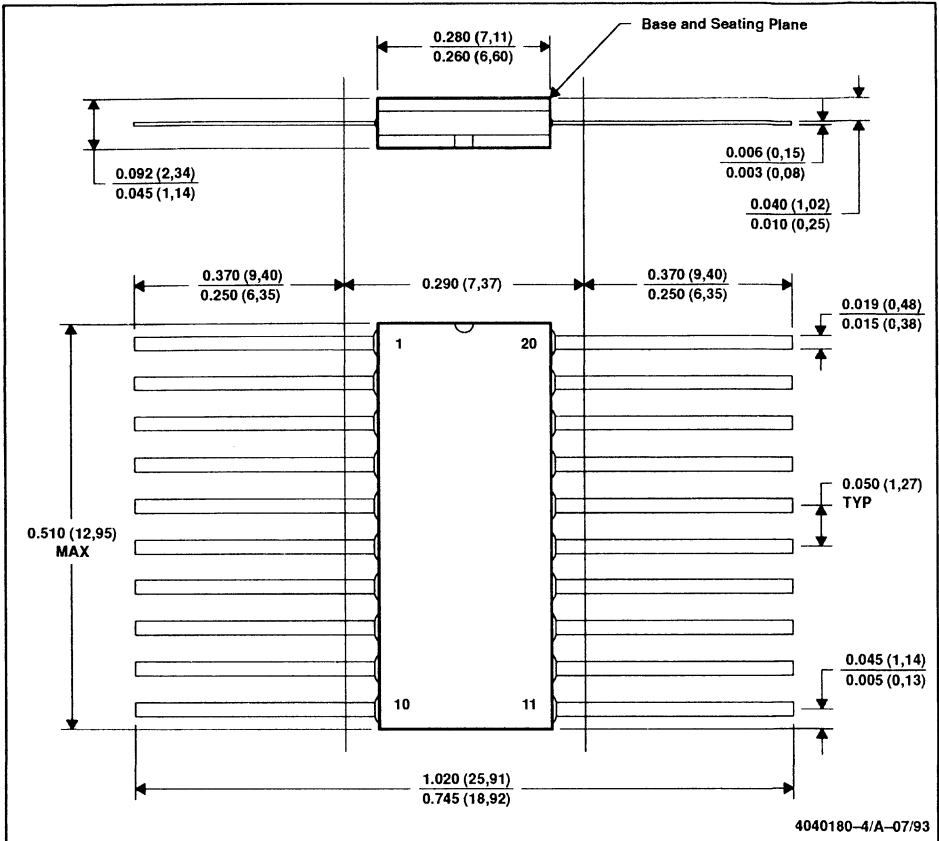


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Leads are within 0.005 (0,13) radius of true position (T.P.) at maximum material condition.
 - D. Falls within JEDEC MO-004AA dimensions.
 - E. Index point is provided on cap for terminal identification only.

MECHANICAL DATA

W/R-GDFP-F20

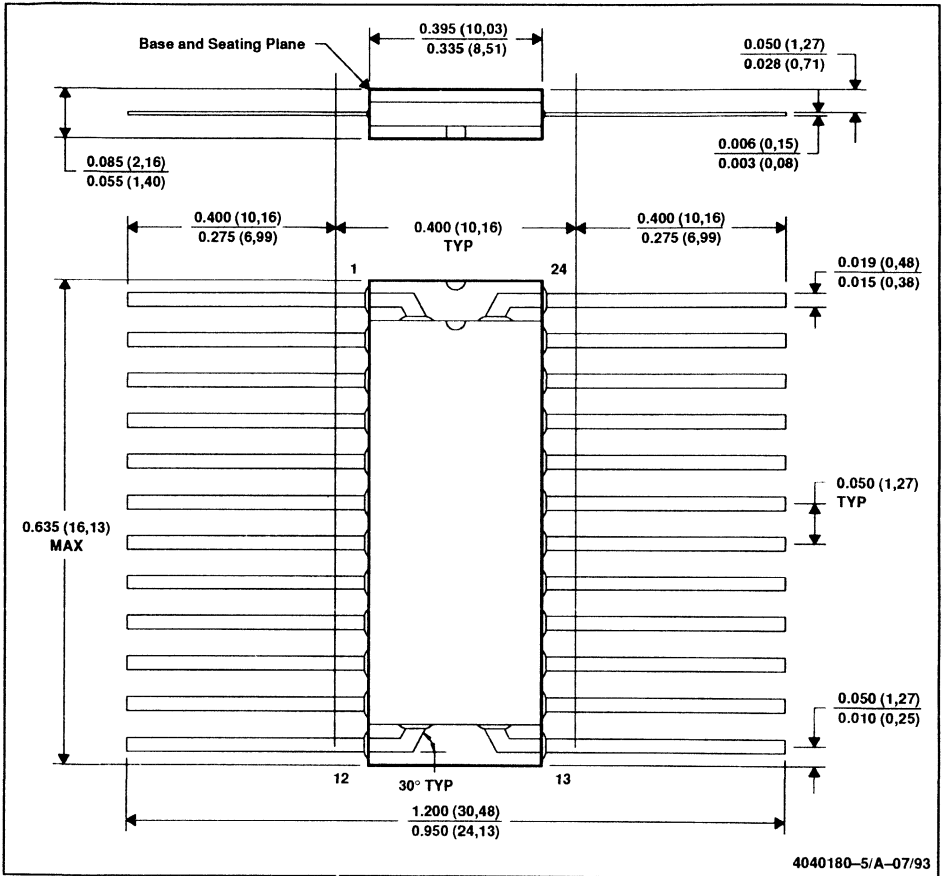
CERAMIC FLAT PACKAGE



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Leads are within 0.005 (0,13) radius of true position (T.P.) at maximum material condition.
 D. Index point is provided on cap for terminal identification only.

W/R-GDFP-F24

CERAMIC FLAT PACKAGE



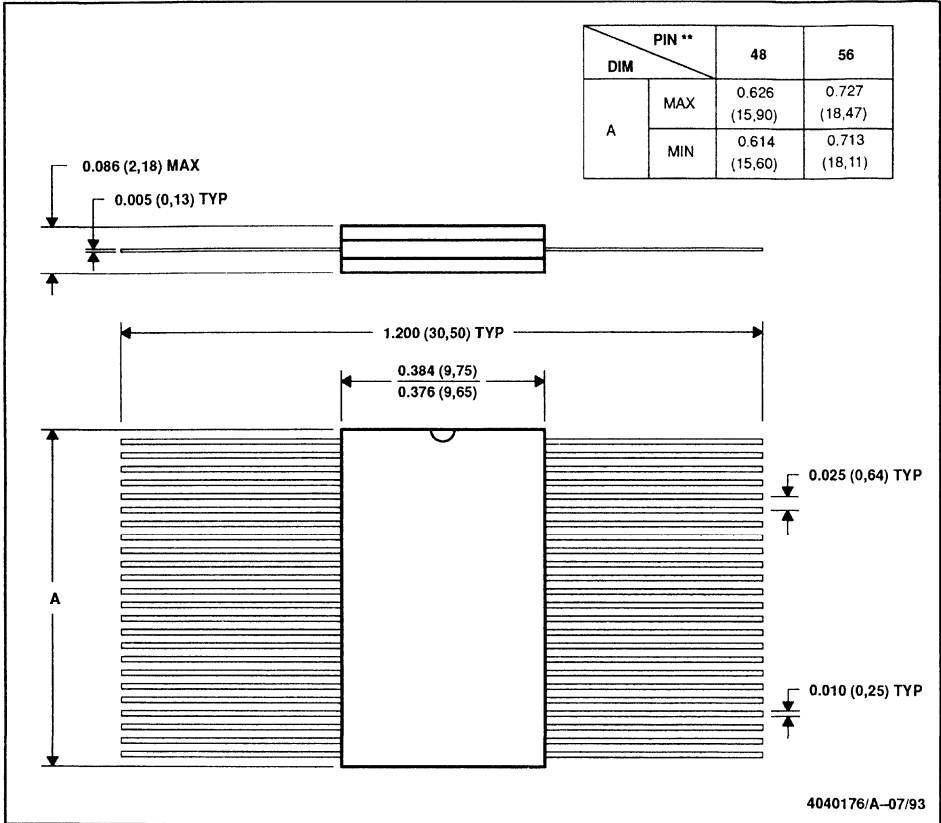
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Leads are within 0.005 (0,13) radius of true position (T.P.) at maximum material condition.
 - D. Falls within JEDEC MO-019AA dimensions.
 - E. Index point is provided on cap for terminal identification only.
 - F. End configuration of 24-pin package is at the option of TI.
 - G. Not applicable for solder-dipped leads. When solder-dipped leads are specified, dipped area extends from lead tip to within 0.050 (1,27) of the package body.

MECHANICAL DATA

WD/R-GDFP-F**

CERAMIC FLAT PACKAGE

48-PIN SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.

Notes

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